A Roadmap to 65nm for EDA

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Semiconductor Process Flow

Market size for 2002 Sources: VLSI, Dataquest, Synopsys Estimates

Main Drivers for IC Design

- Technology
  - Physics
  - Complexity

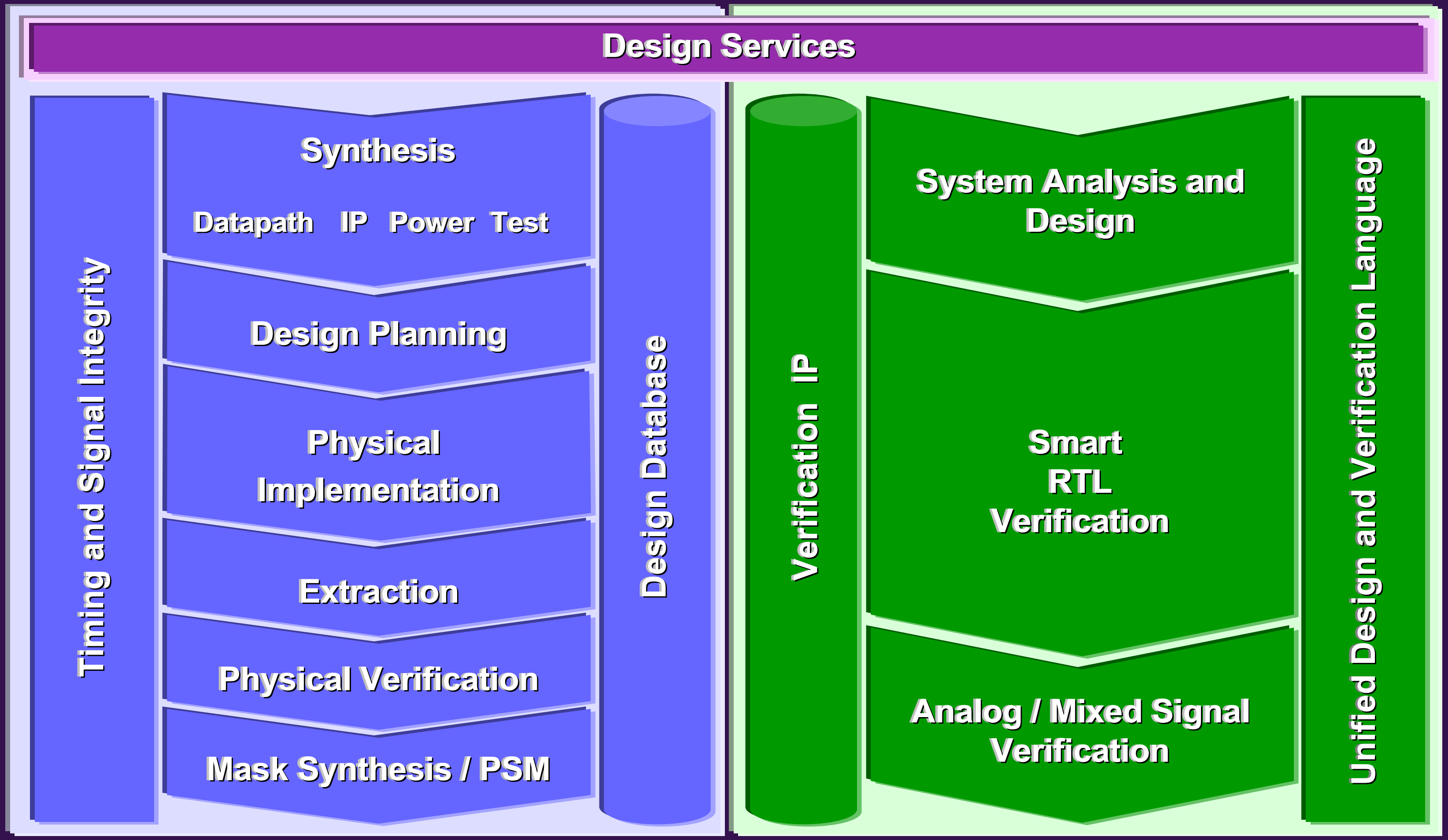
- Application
  - All
  - Communications (56%)
  - Computer (24%)
  - Consumer (21%)
  - Other Environment

– Power
– Heterogeneity
– Speed
– Size (cost)
– Reliability,

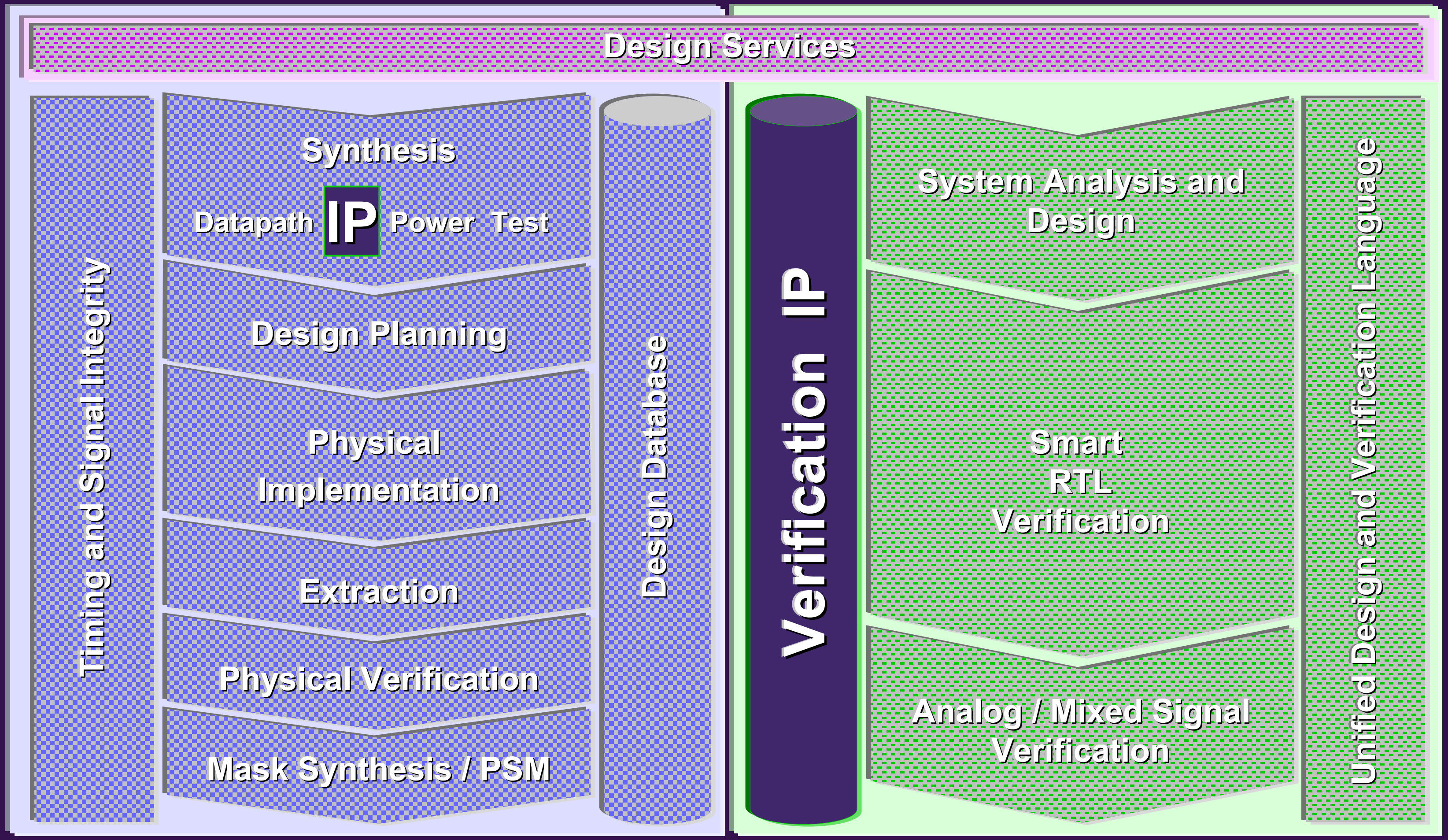
What Is Needed for 65nm and Below

- IP-based methodology
- Central data base
- Hierarchy
- Integrated verification environment
- Timing closure and signal integrity
- Low power design flow
- Analog design flow
- Build in chip-level self test
- Design for manufacturability
- Chip / package design

SoC Design

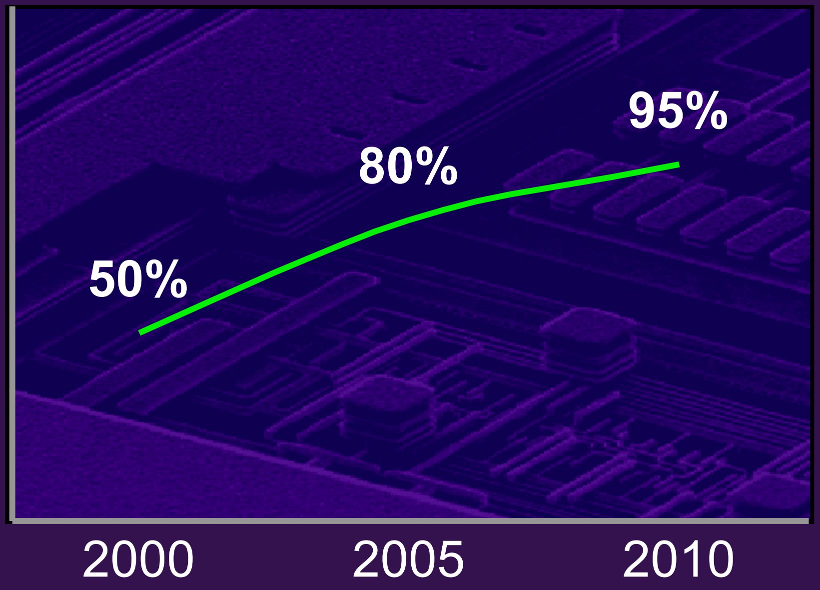

Design Services
Timing and Signal Integrity
Synthesis
Datapath IP Power Test
Design Planning
Physical Implementation
Extraction
Physical Verification
Mask Synthesis / PSM
Design Database
Verification IP
System Analysis and Design
Smart RTL Verification
Analog / Mixed Signal Verification
Unified Design and Verification Language

IP Based Methodology

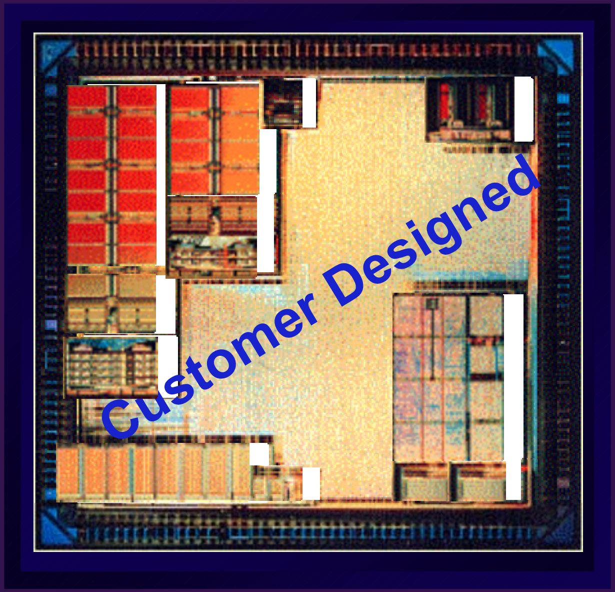


IP Reuse

Pre-designed Blocks as % of an SoC

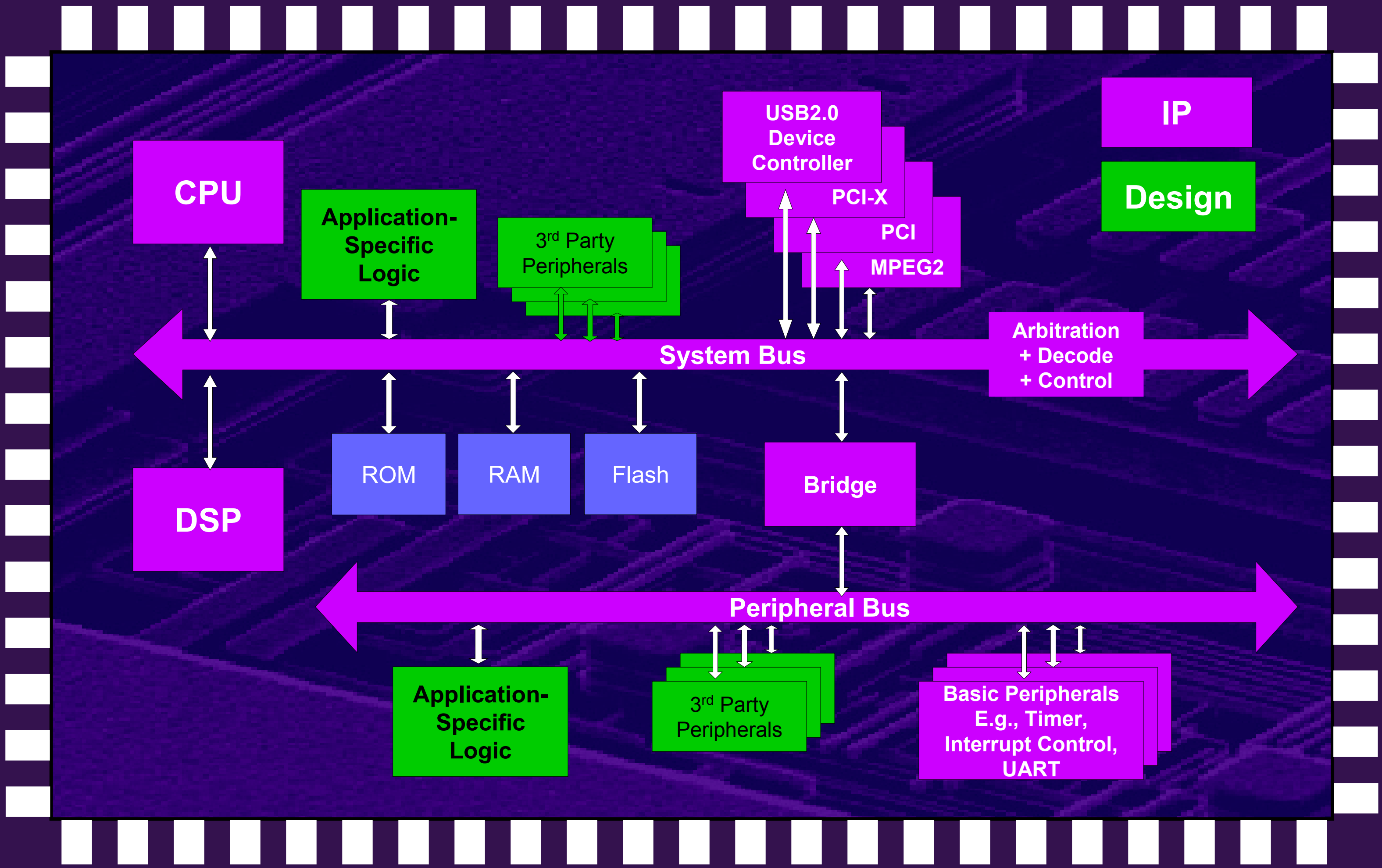


IP, Memory and SW Increasing

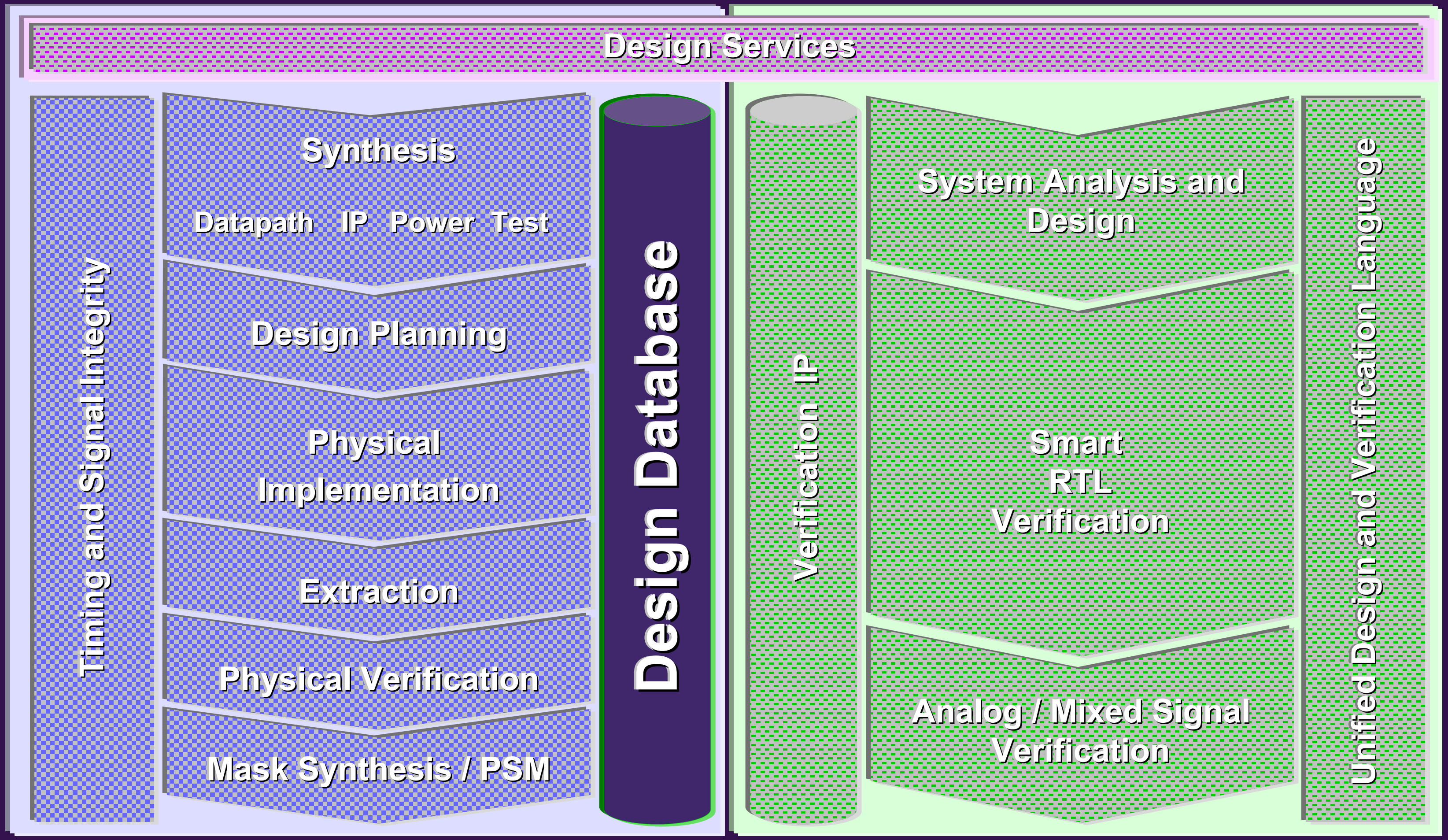


Source: Dataquest, 2000

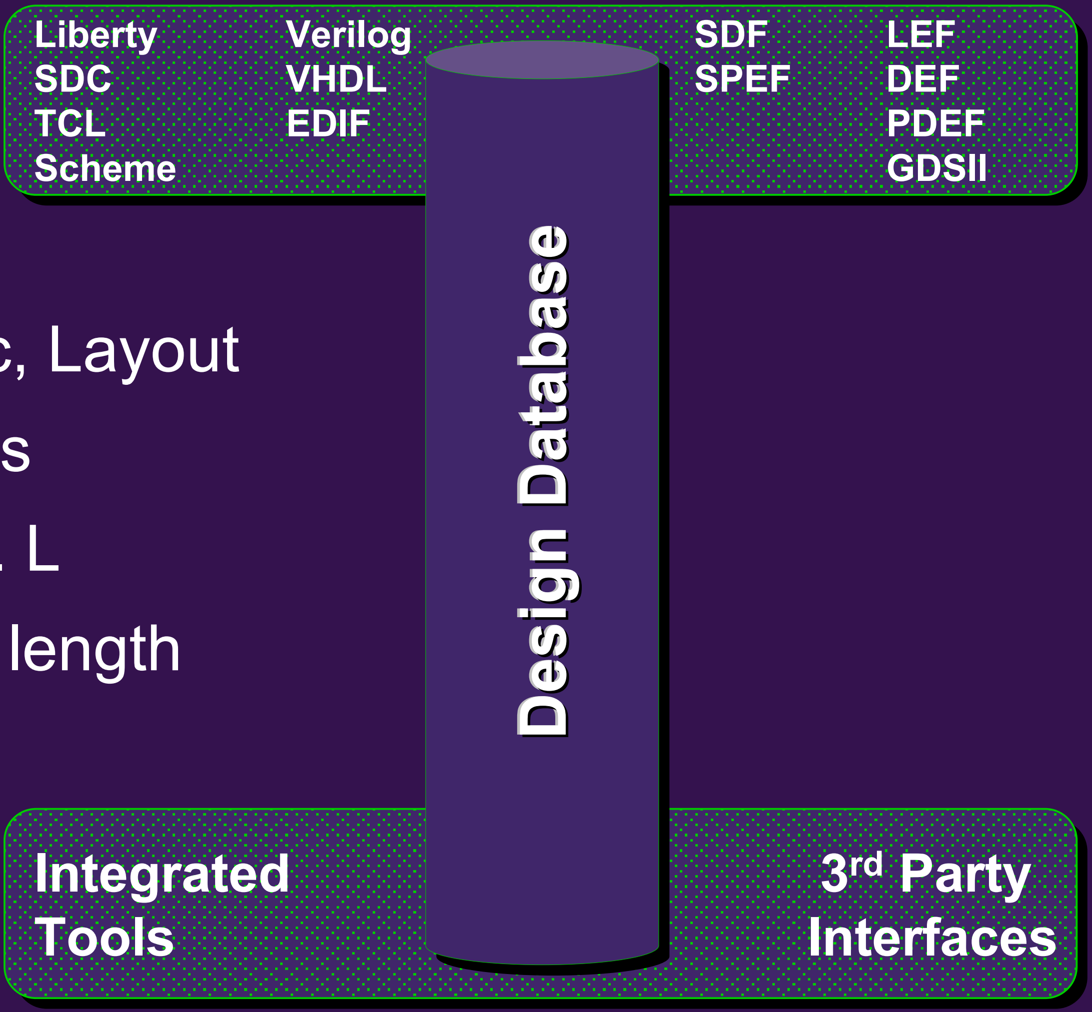
From IP to Platform-Based Design



Central Data Base



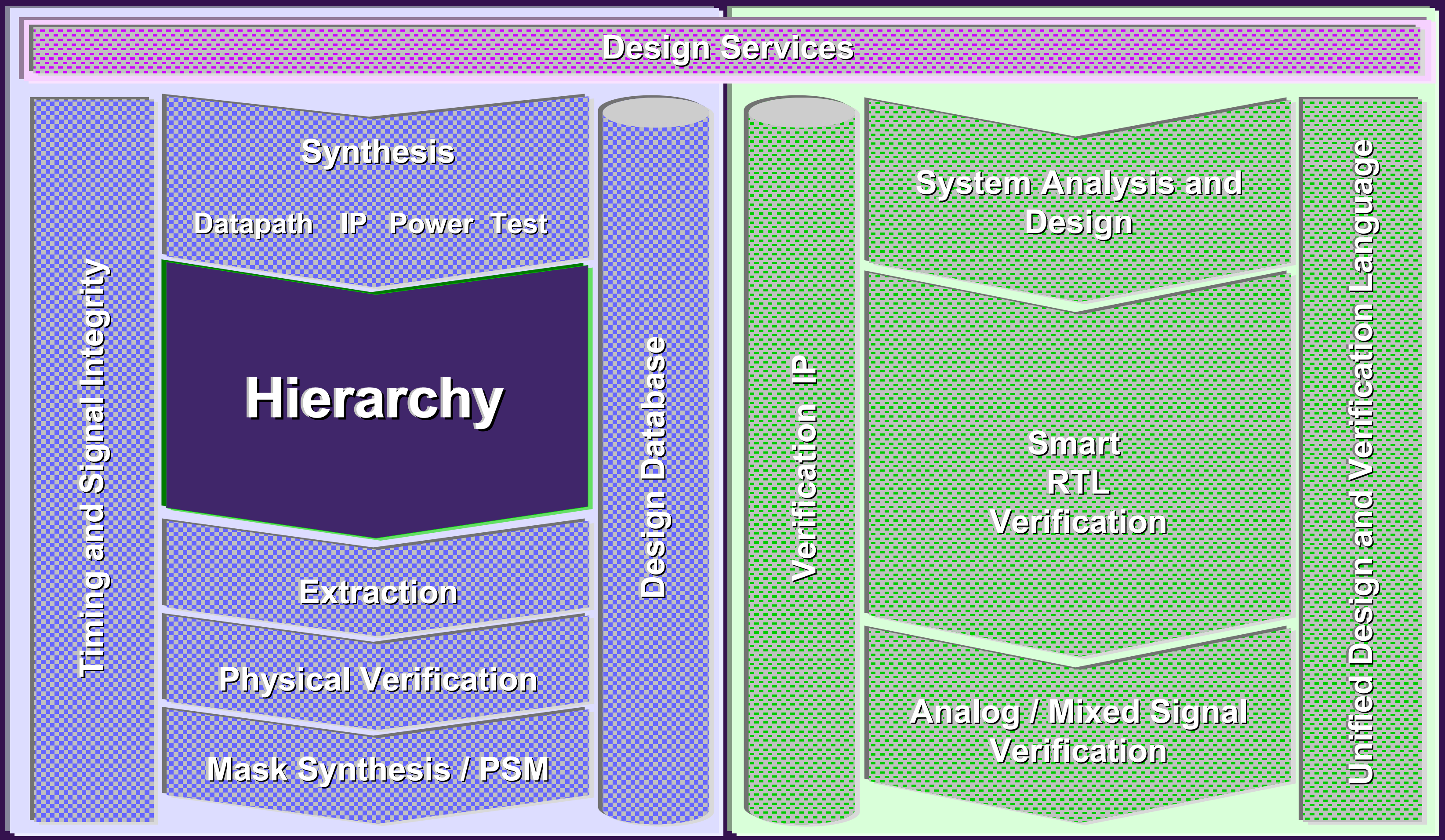
Integrated Data



Examples

Libraries:	Logic, Layout
Logic:	Loads
Parasitic:	C, R. L
Physical:	Wire length

Hierarchy



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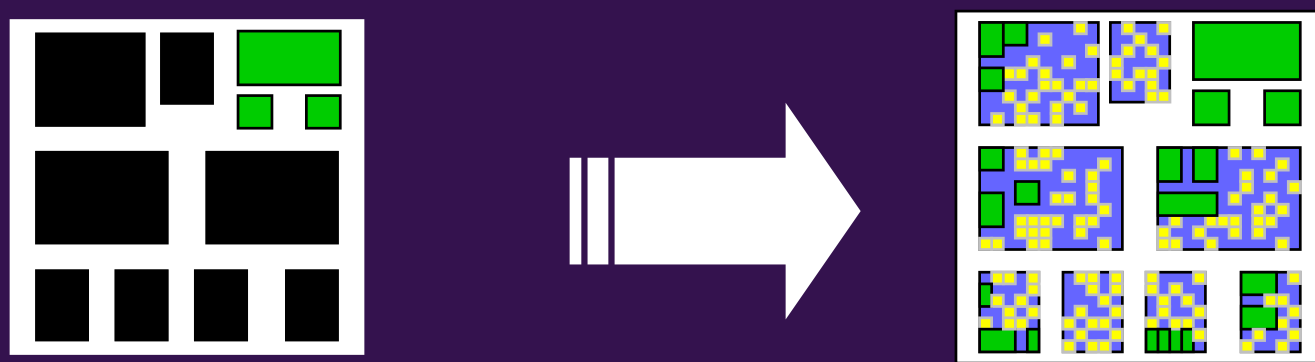
Approaches to Hierarchy

Top Down / Bottom Up

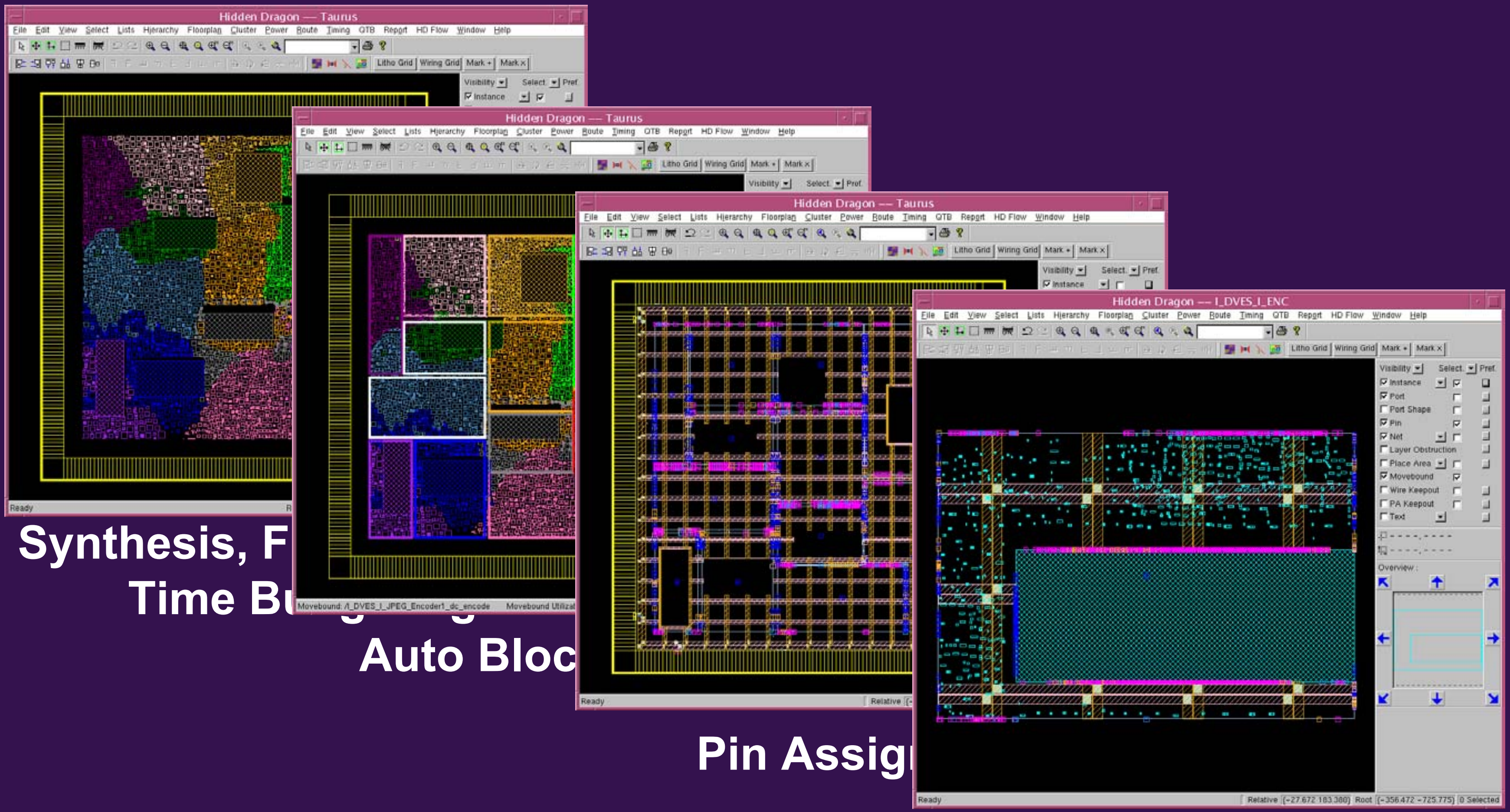
Virtually Flat



- Only top level is visible
- Block, macro and pin assignment quality poor without chip context

- All key operations use virtual flat view of chip
- Chip timing, routability and power can be analyzed and optimized

Main Tasks in Hierarchical Design



Synthesis, F

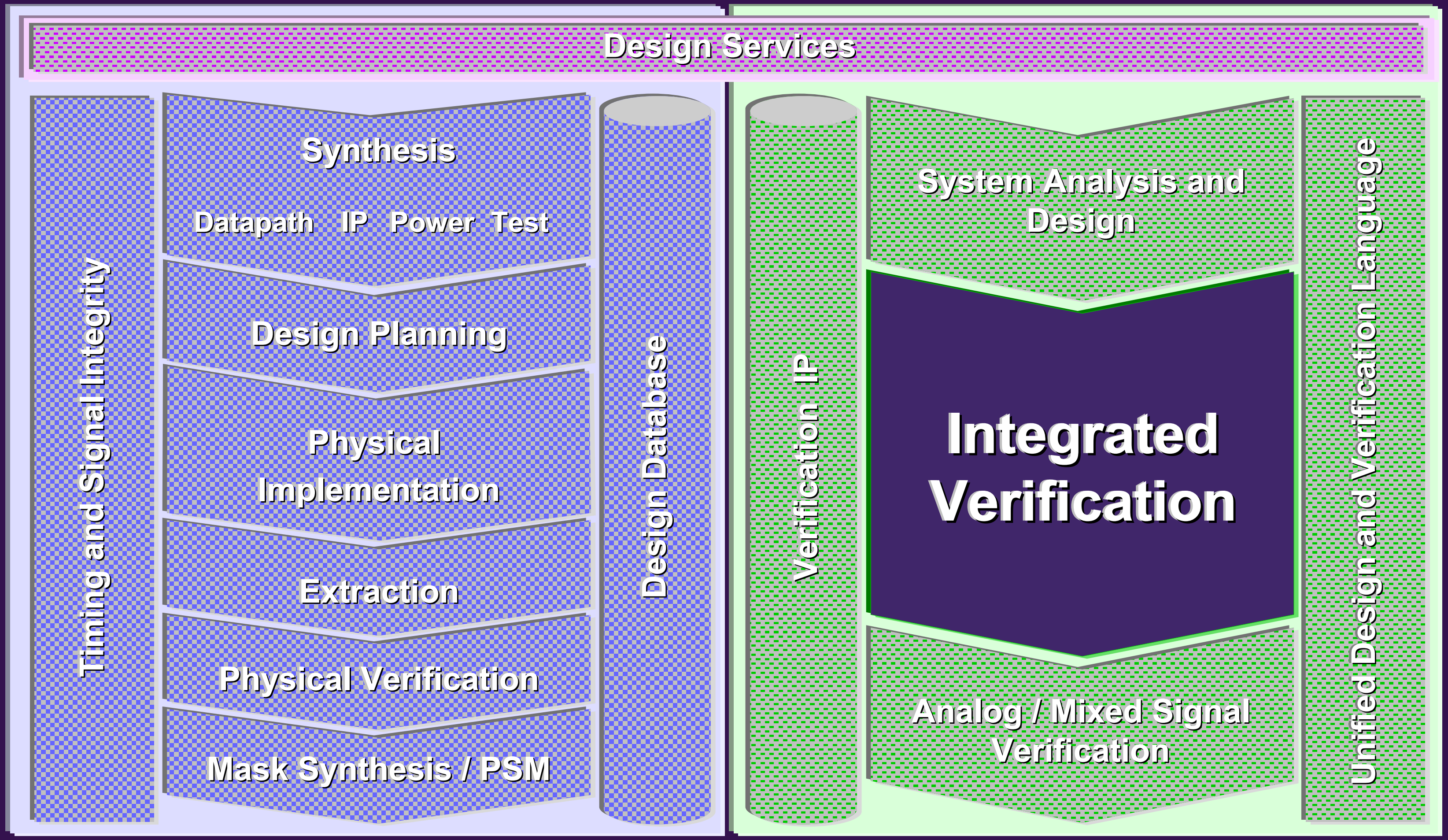
Time Bu

Auto Bloc

Pin Assig

Ready For Physical Design

Integrated Verification Environment



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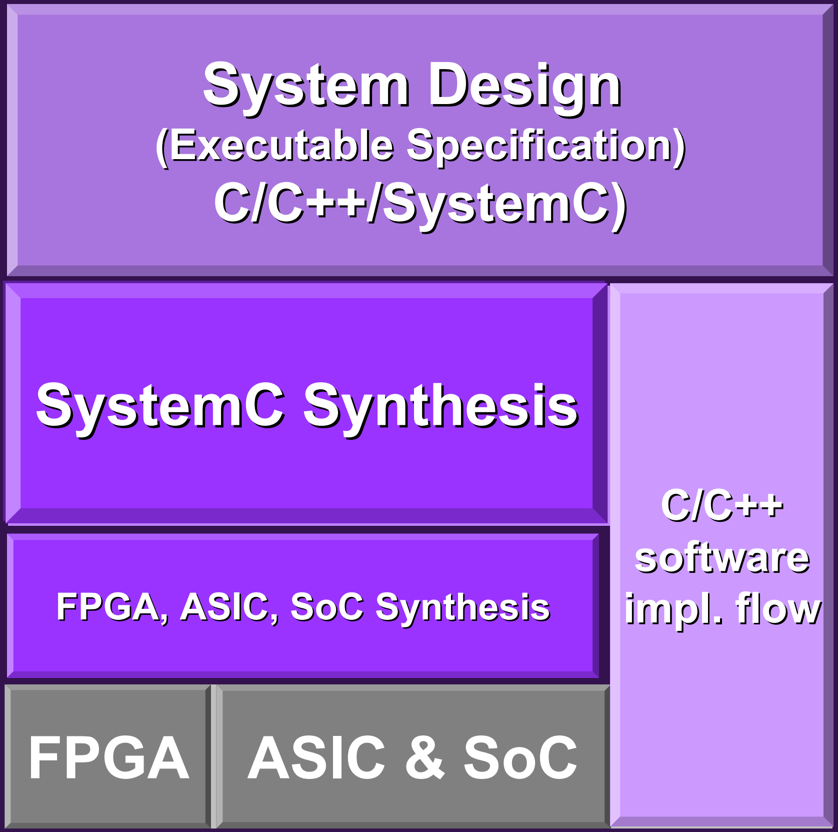
System Level Design and Verification

- Bringing hardware and software together early in the design process
- Hardware synthesis from SystemC
  - RTL and behavioral
  - ASIC, SoC, FPGA

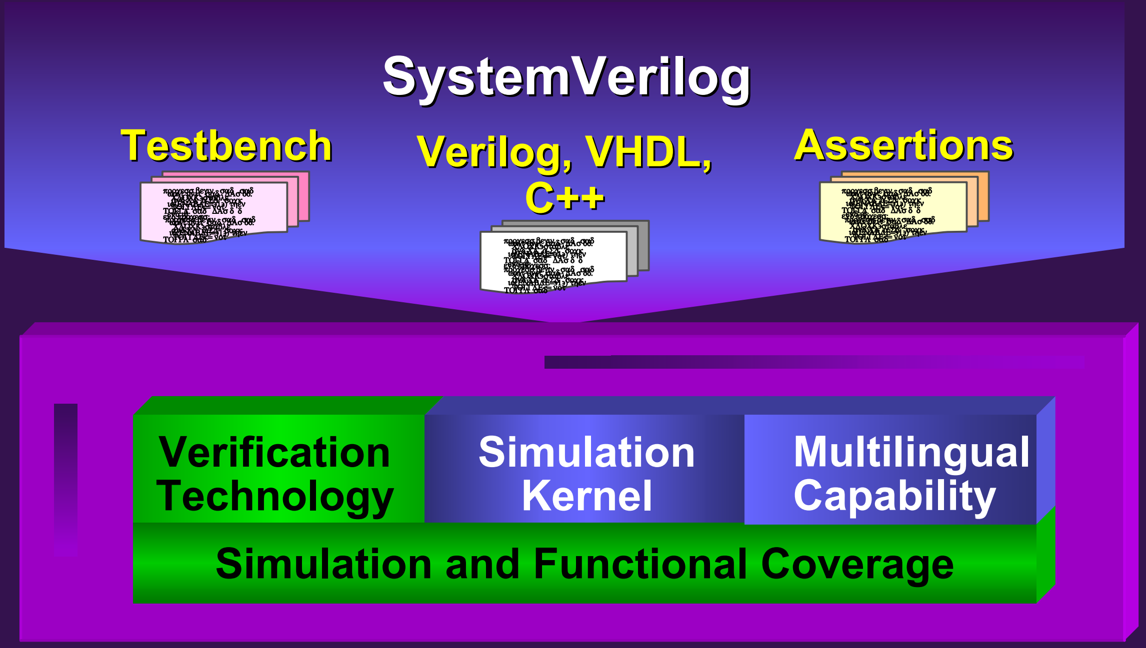


SystemVerilog
Next Generation Verilog

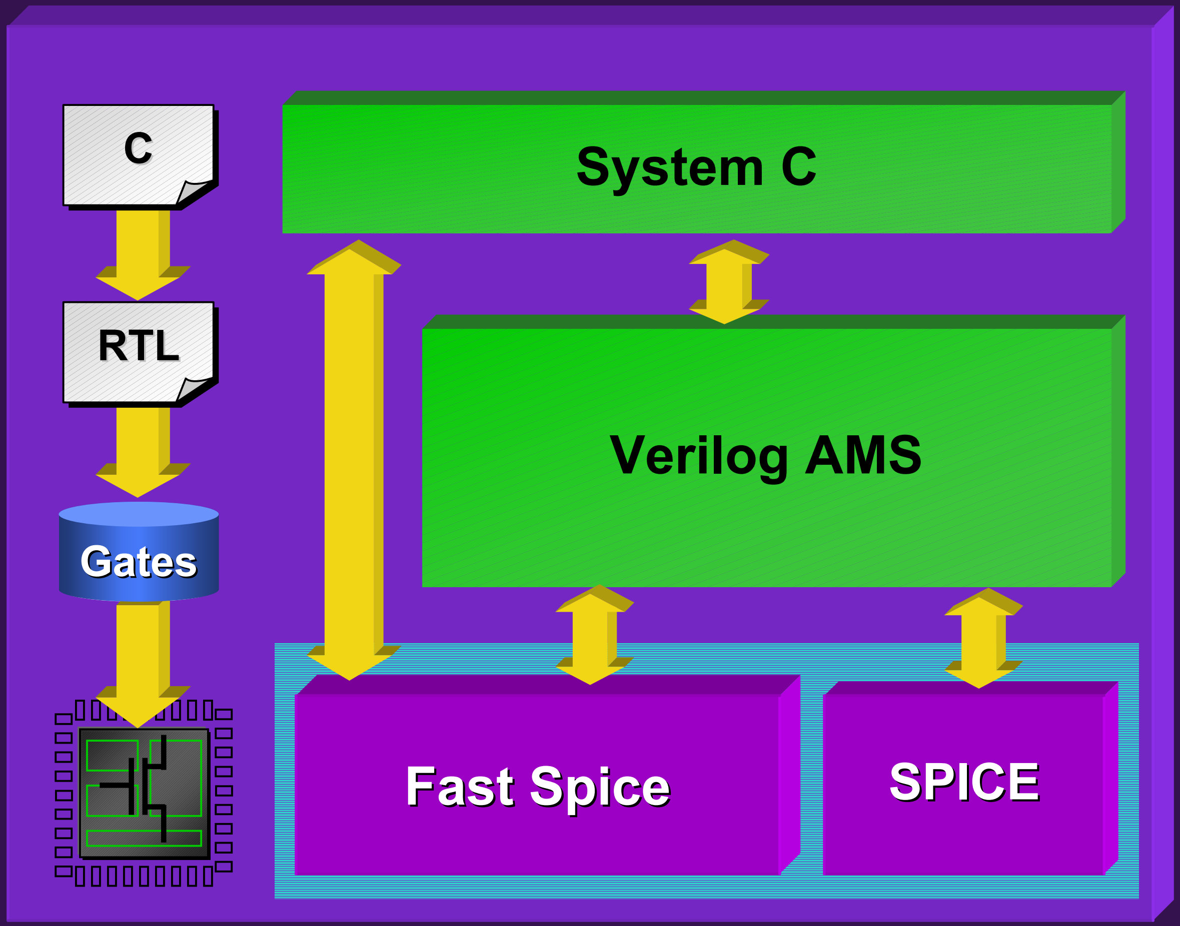
- Concise design features
- C++ extensions
- Unified assertions
- Testbench capabilities
- Advanced APIs

RTL Design
Simulation Evolving Into DFV Platform

- Newer technologies attach to simulator
  - Testbenches
    Assertions
    Coverage
    Formal
    C++
- Verification technologies being native to simulator offers best performance
- Ease of adoption



Analog Mixed-Signal Verification

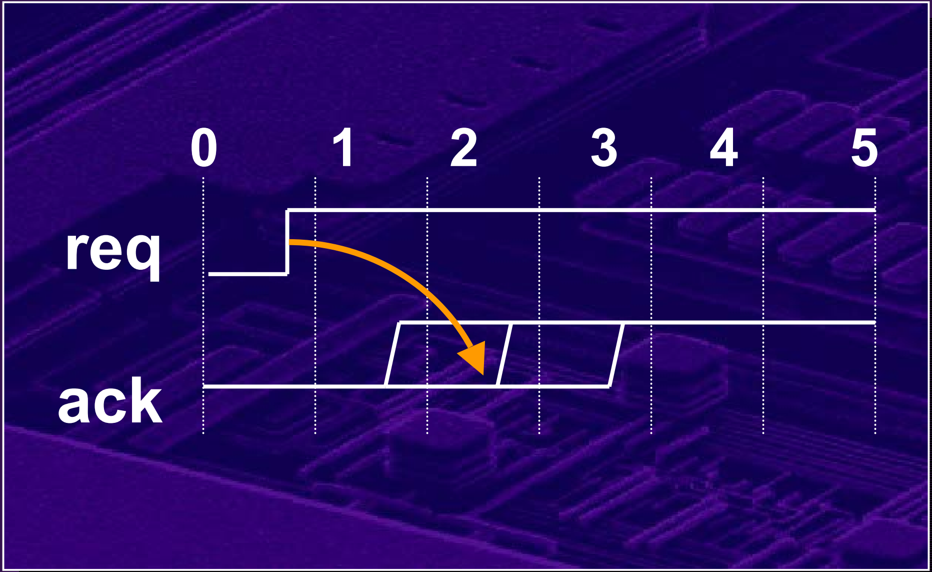


Formal Verification

- Equivalence Checking
- Property Checking
  - Assertions
  - Constraints

What is an Assertion (Constraint)?

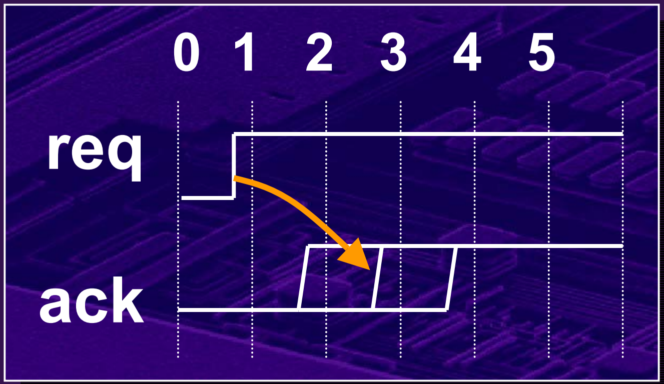
Example



"After request is asserted, acknowledge will come 1 to 3 cycles later"

Assertions (constraints) capture designer assumptions and intent

Assertion Languages Are Very Efficient



Traditional HDL

```
always @(posedge req)
  begin
     repeat (1) @(posedge clk);
     fork: pos_pos
        begin
           @(posedge ack)
           $display("Assertion Success",$time);
                disable pos_pos;
        end
       begin
          repeat (2) @(posedge clk);
          $display("Assertion Failure",$time);
          disable pos_pos;
       end
     join
  end // always
```

Assertion-based HVL

```
clock posedge clk {
   event req_cycle: posedge req #[1..3] posedge
ack;
 }
```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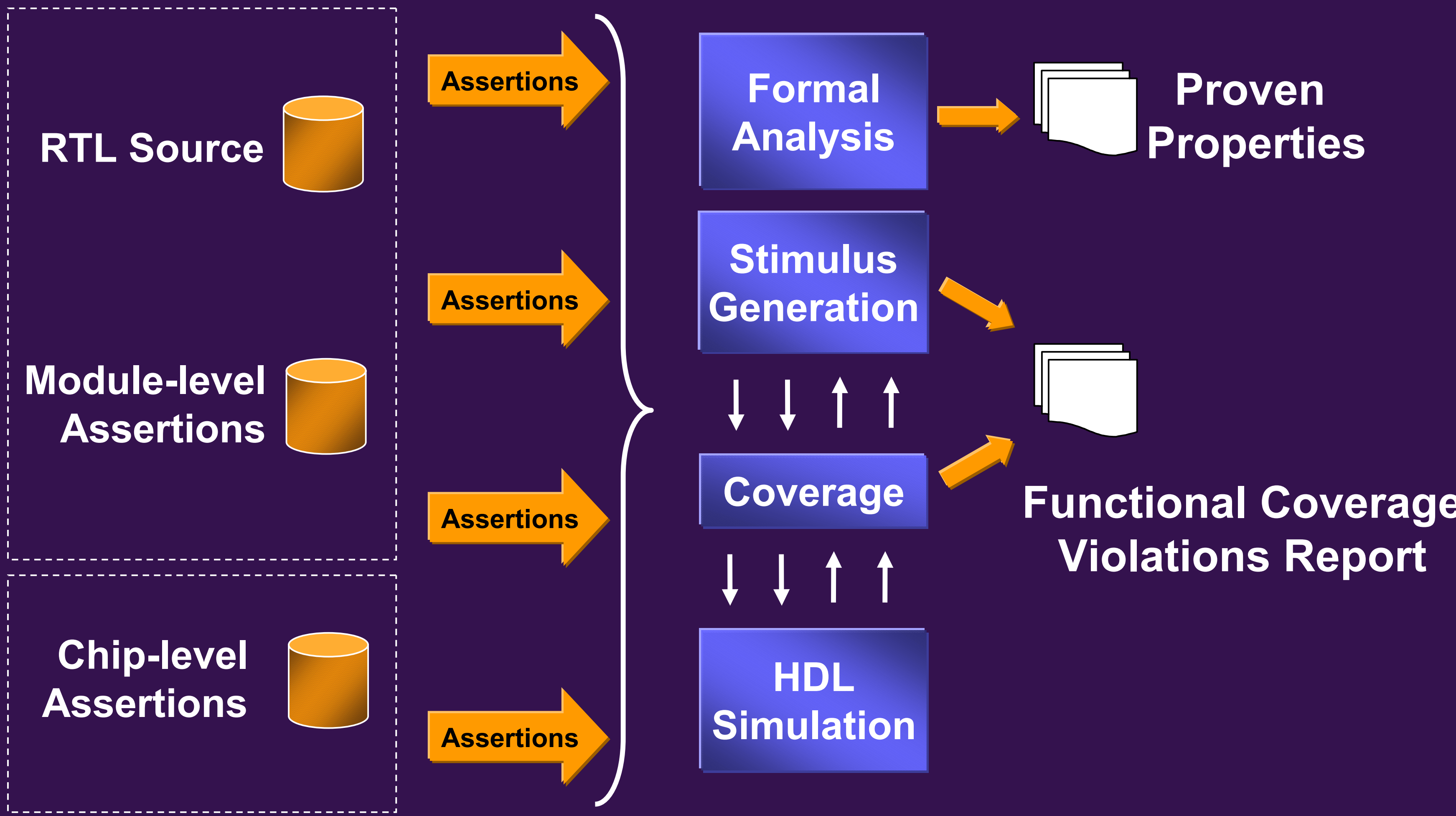
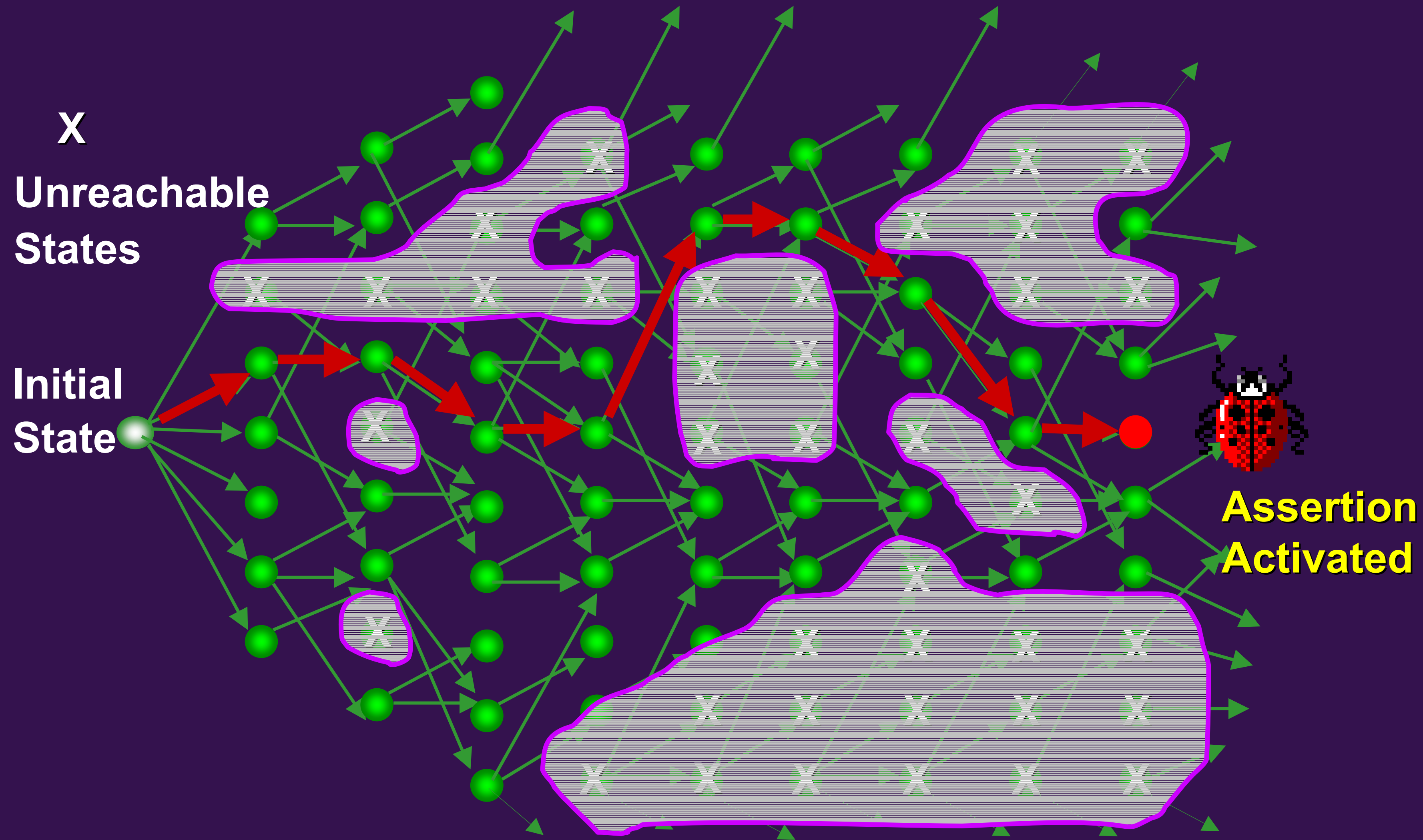
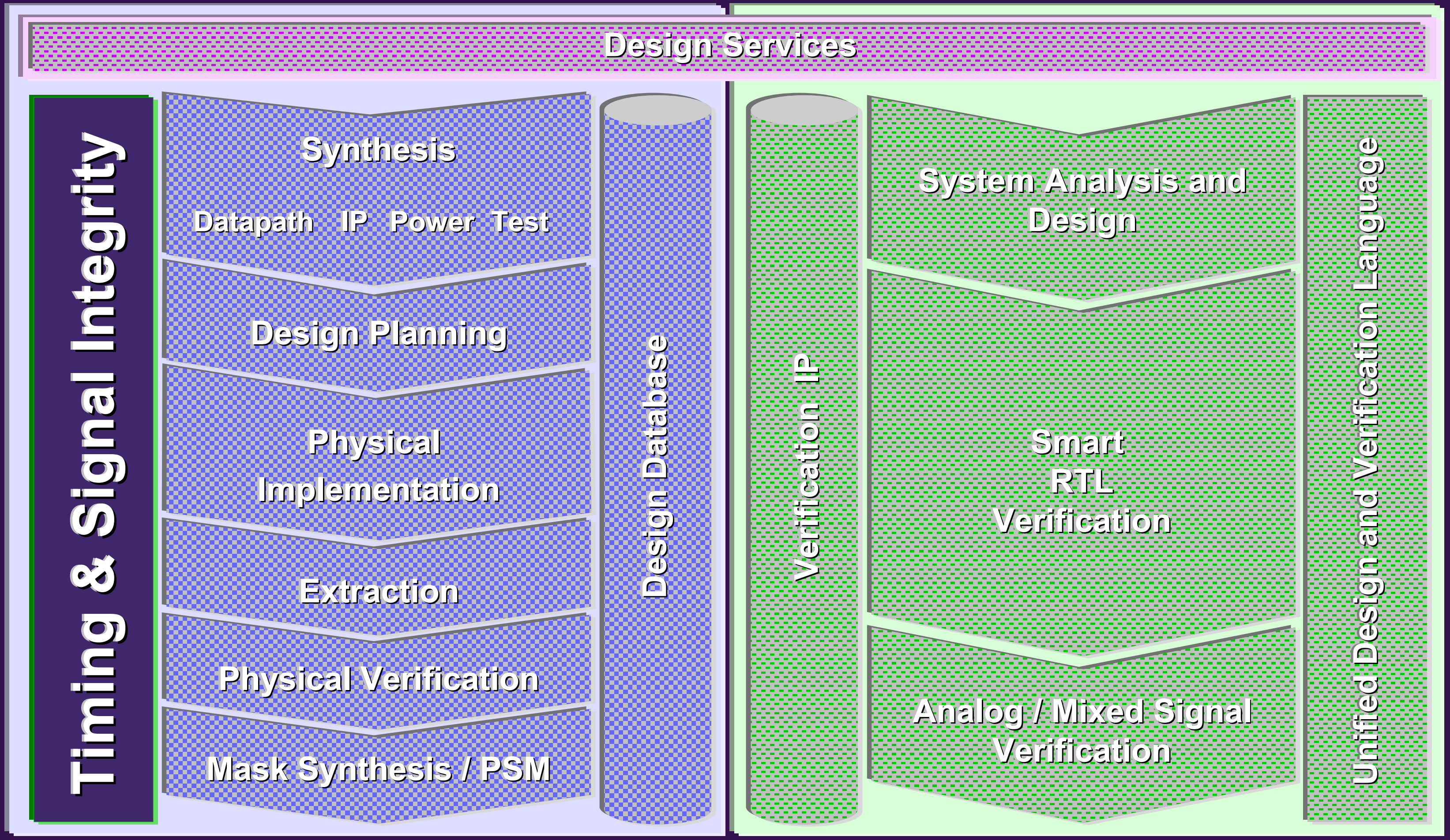
Assertions Enable Verification Automation



Assertions Constrain Exploding Verification State Space



Timing Closure and Signal Integrity



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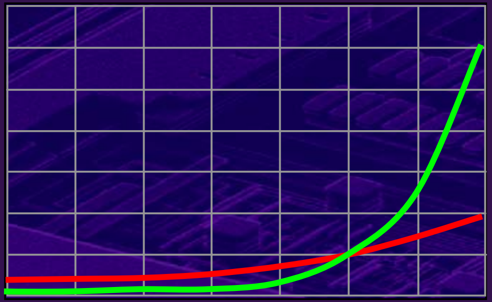
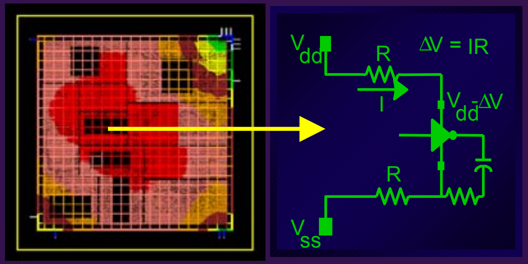
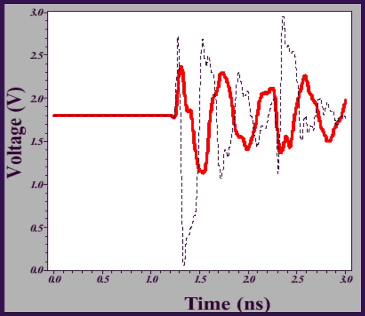
Process Technology <130nm Creates New Problems for Design Technology

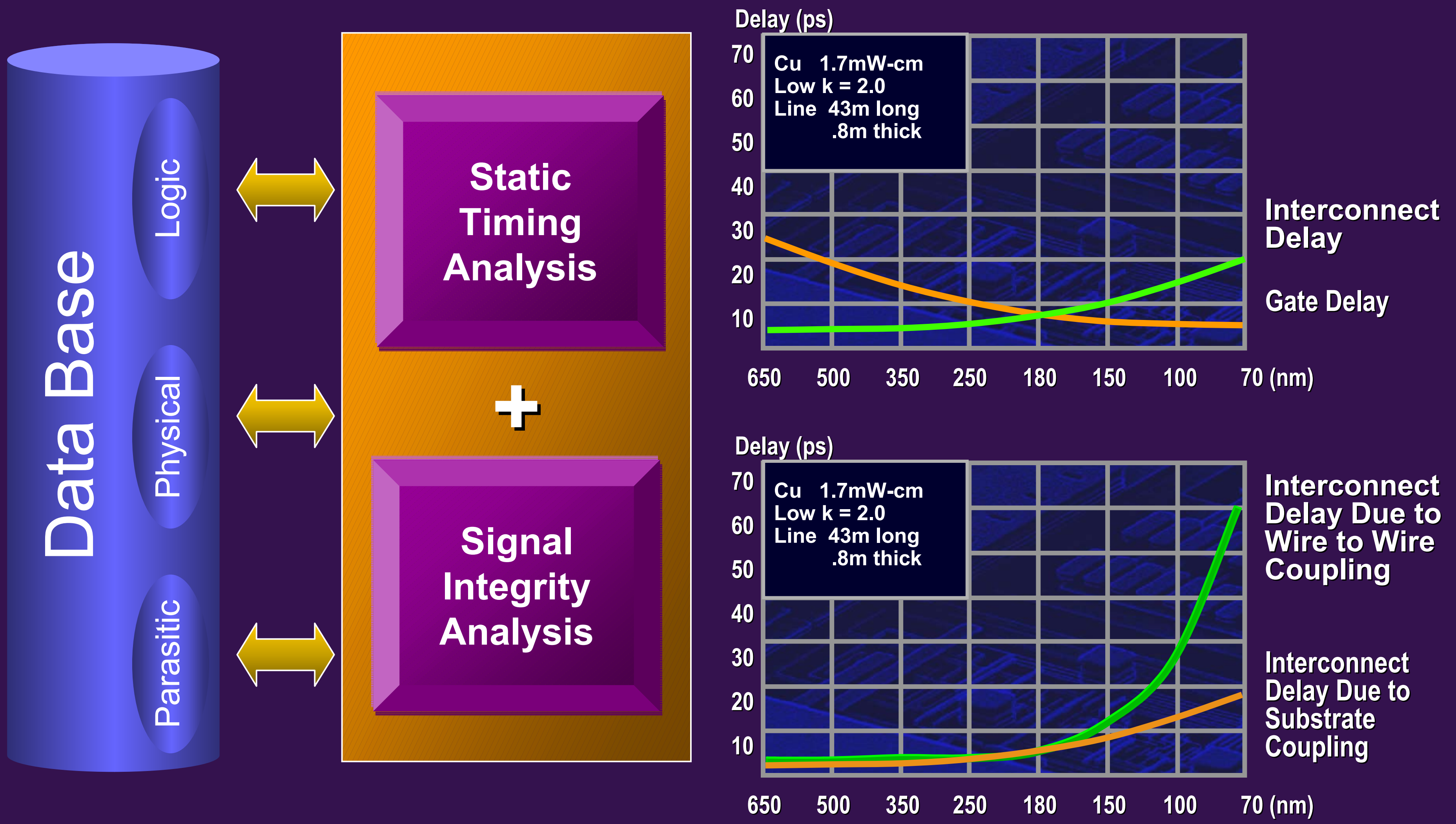
- The primary physical effect of concern is cross-coupled capacitance plus the miller effect
  - Functional errors in analog circuitry or dynamic logic
  - Timing errors in static digital circuitry
- IR drop (static leakage and dynamic IR drop) handled in power
- Other important effects & features are inductance, CD variation, EM



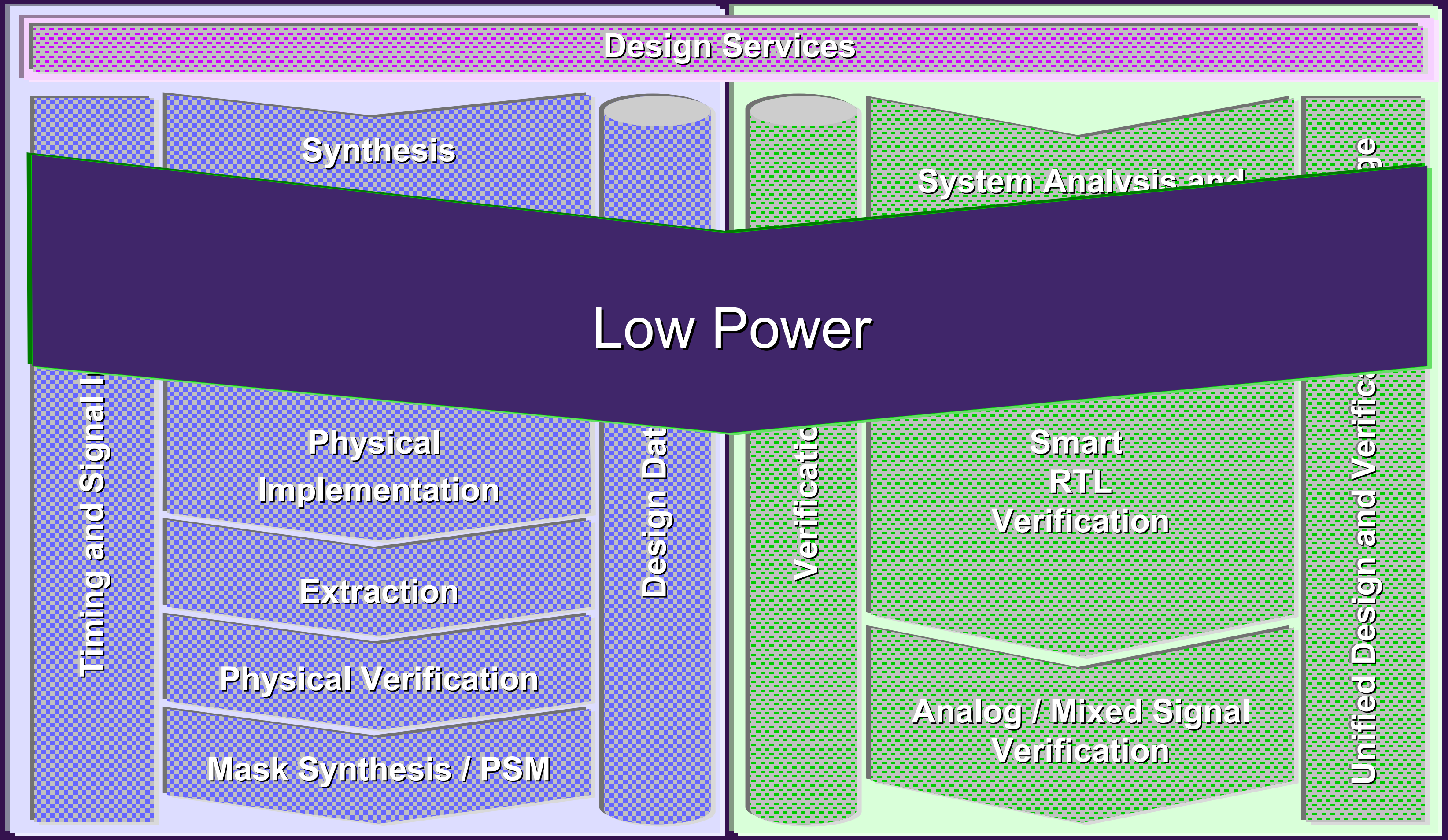




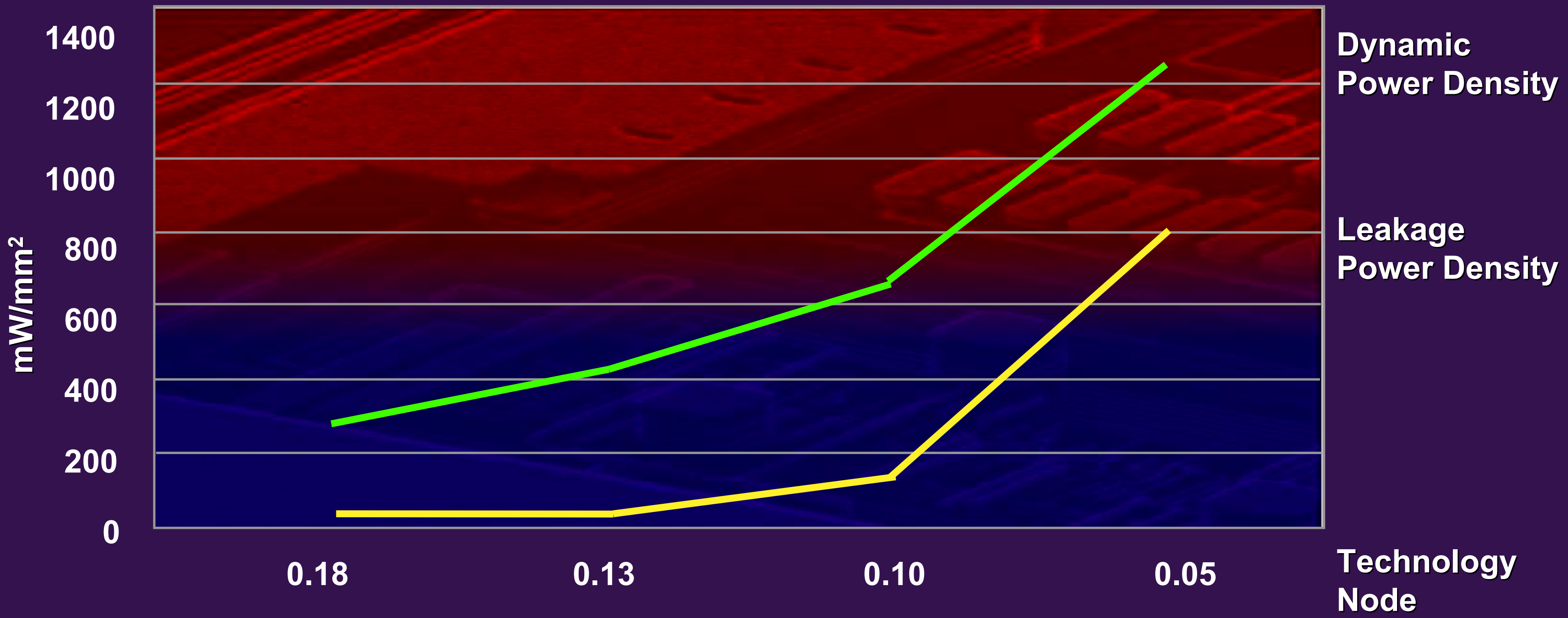
Static Timing Analysis



Low Power Design Flow



Power Scaling



- Technology parameters from UMC roadmap
- V_t for high performance design / libraries
- Total switched capacitance grows from 600 pF/mm^2 to 2000pF/mm^2
- Area scales down, function is the same

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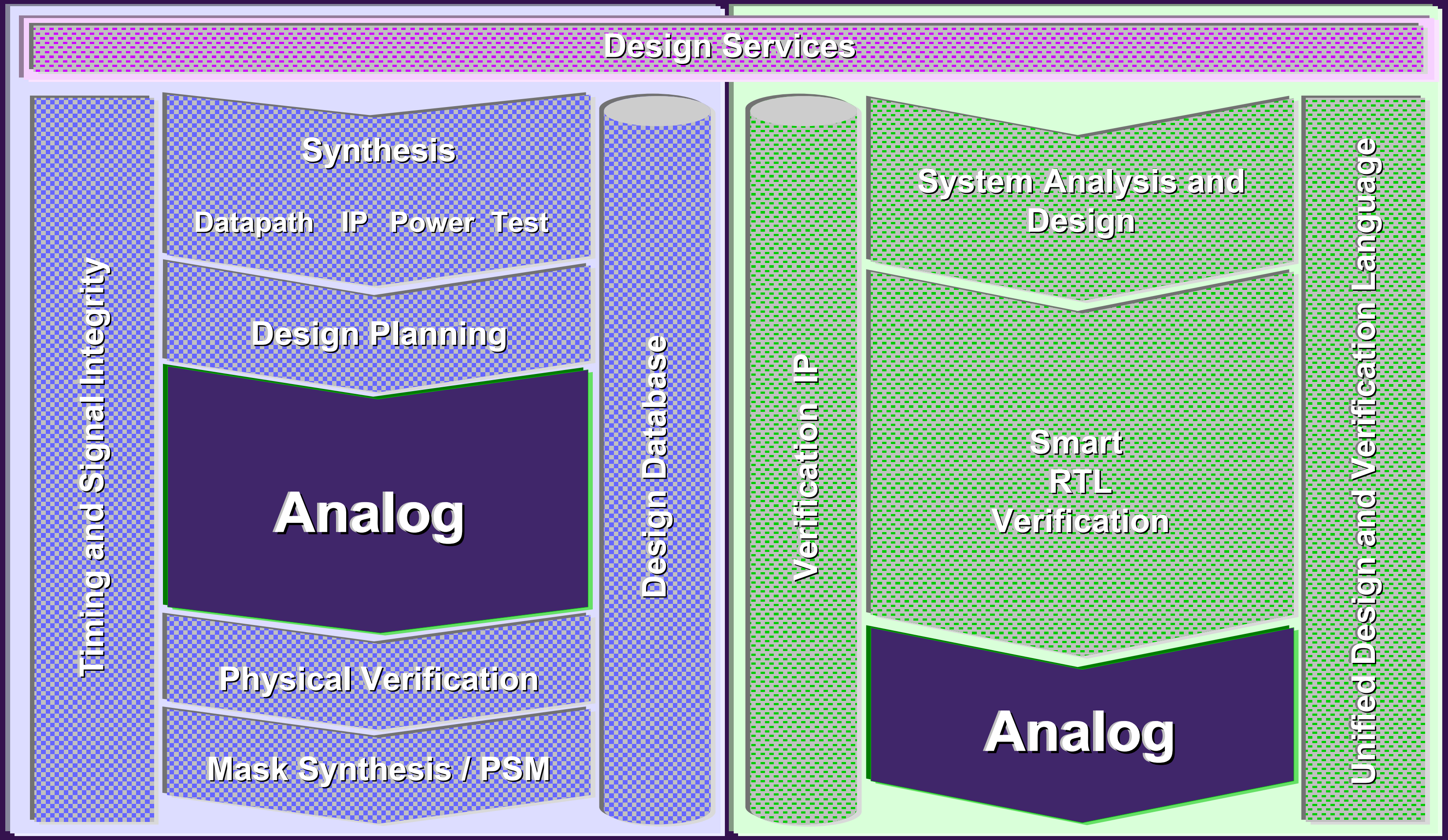
Low Power Design Enablers

- Power modeling and analysis
- Clock gating and tree optimization
- Dynamic voltage scaling
- Power gating
- Leakage optimization using multi-Vt
- Modeling process variation
- Support asynchronous design

Analog Design Flow



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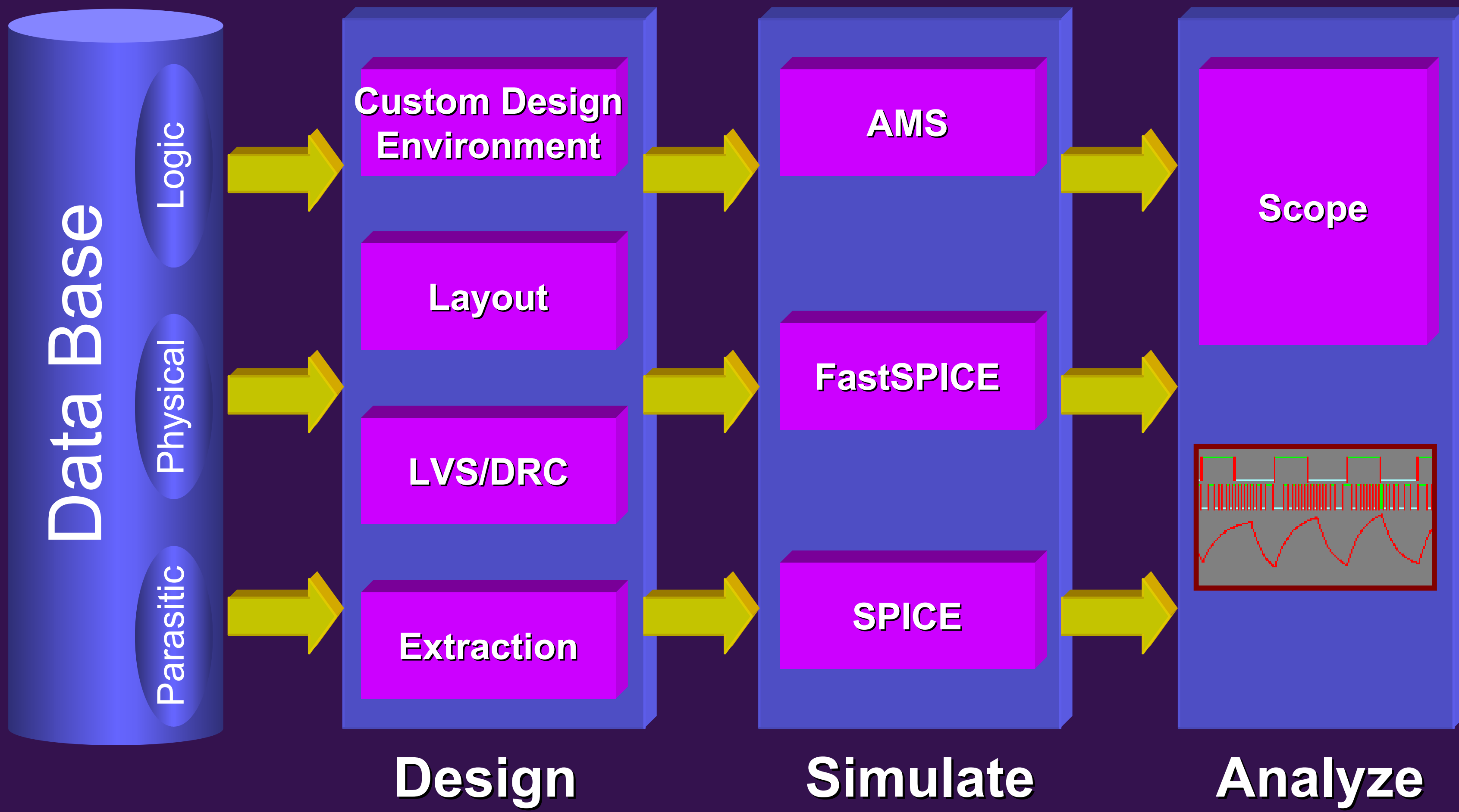
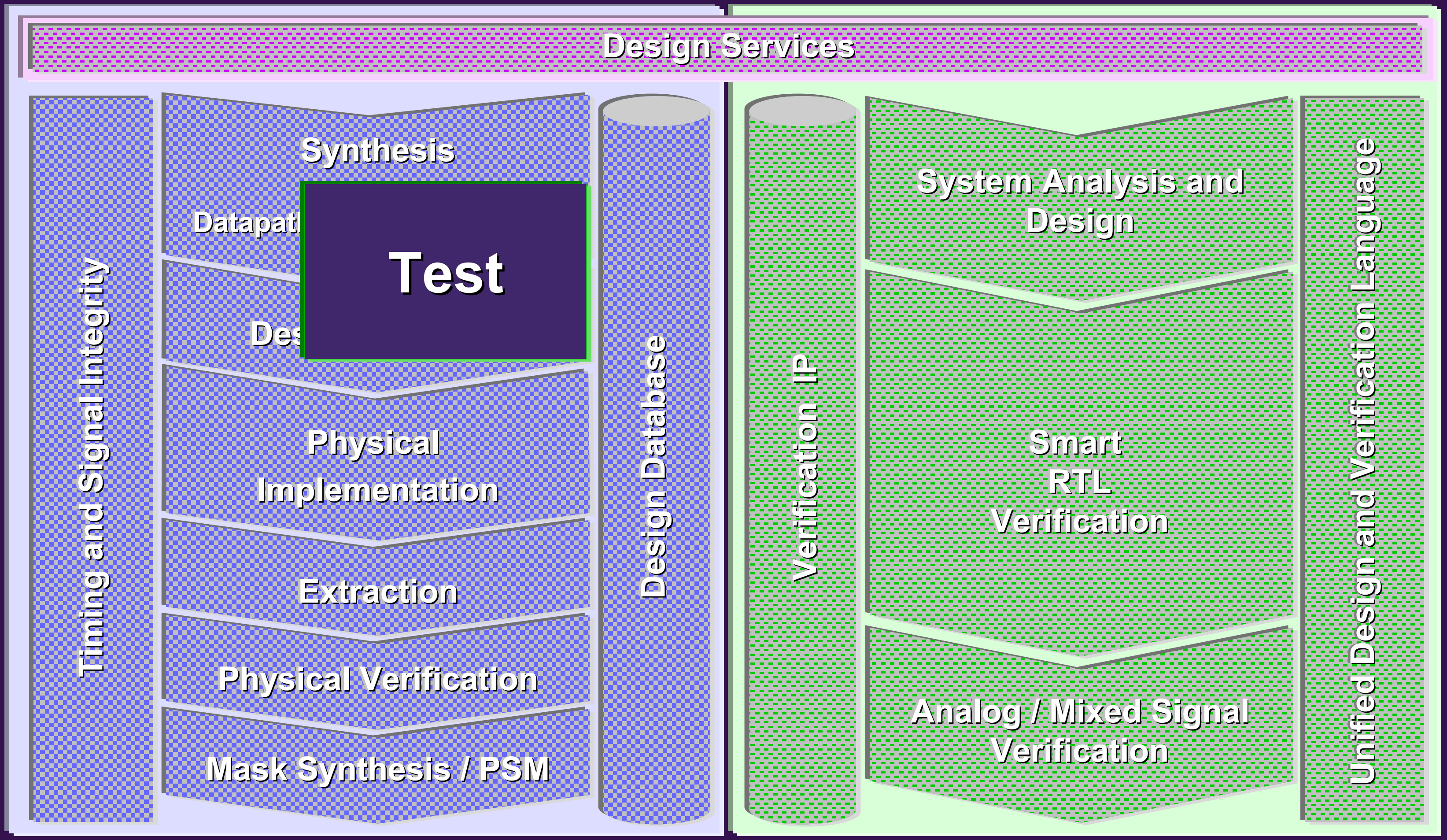
Integrated Custom & Mixed-Signal Analog Design Tools



Built In Self Test (BIST)



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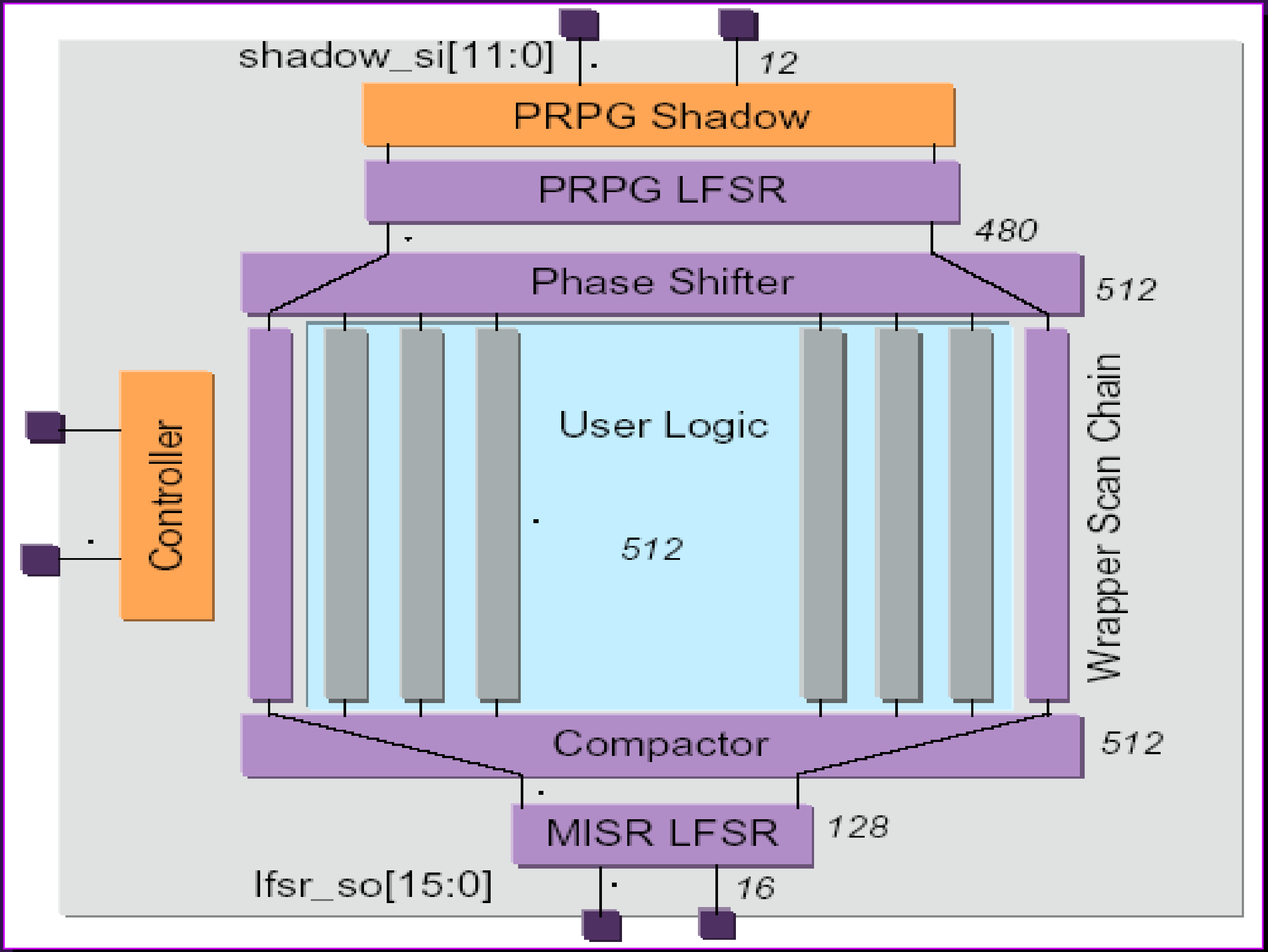
Design for Test

Synopsys SoCBIST Solution



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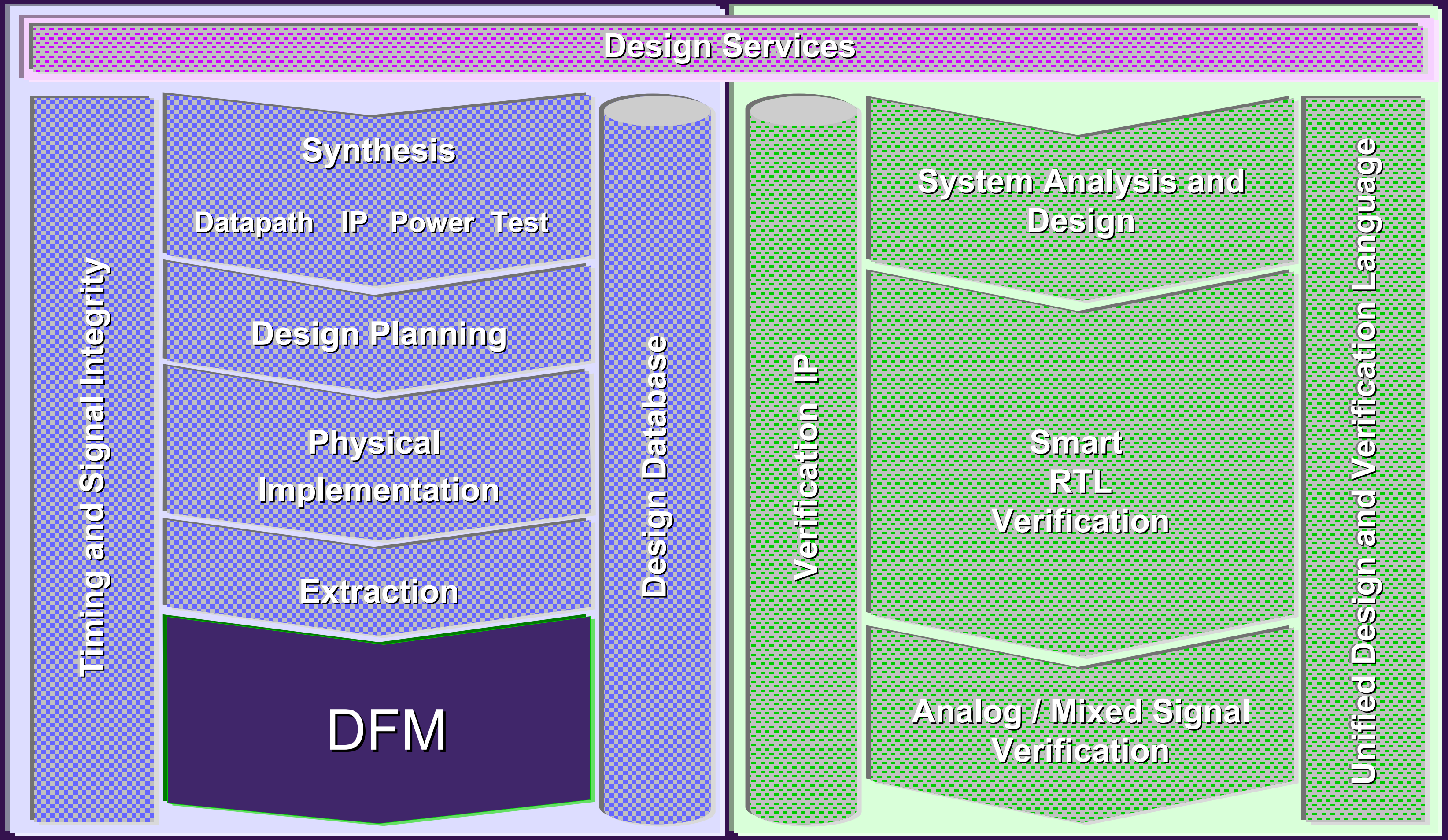
Design For Manufacturing

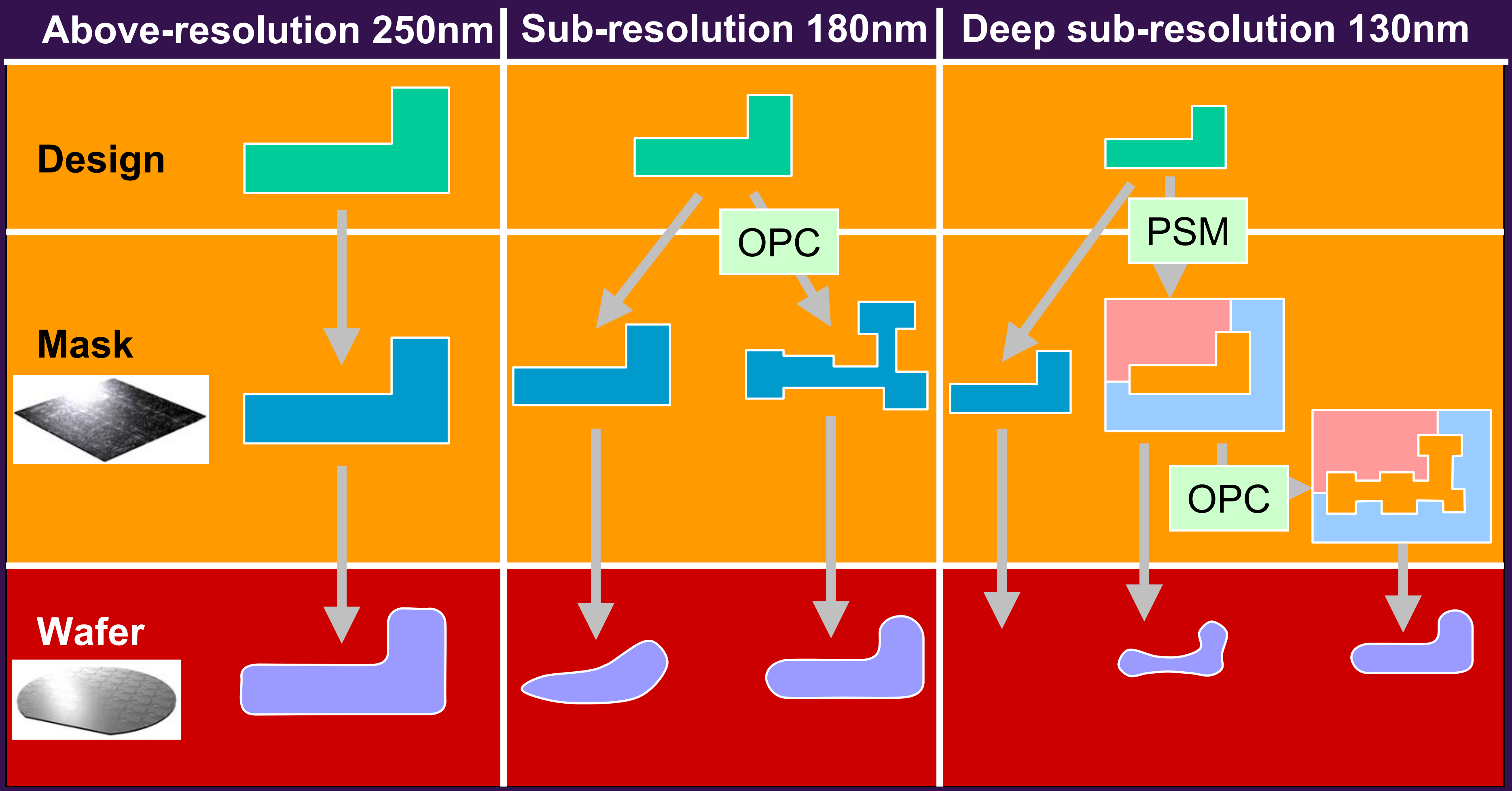


DFM

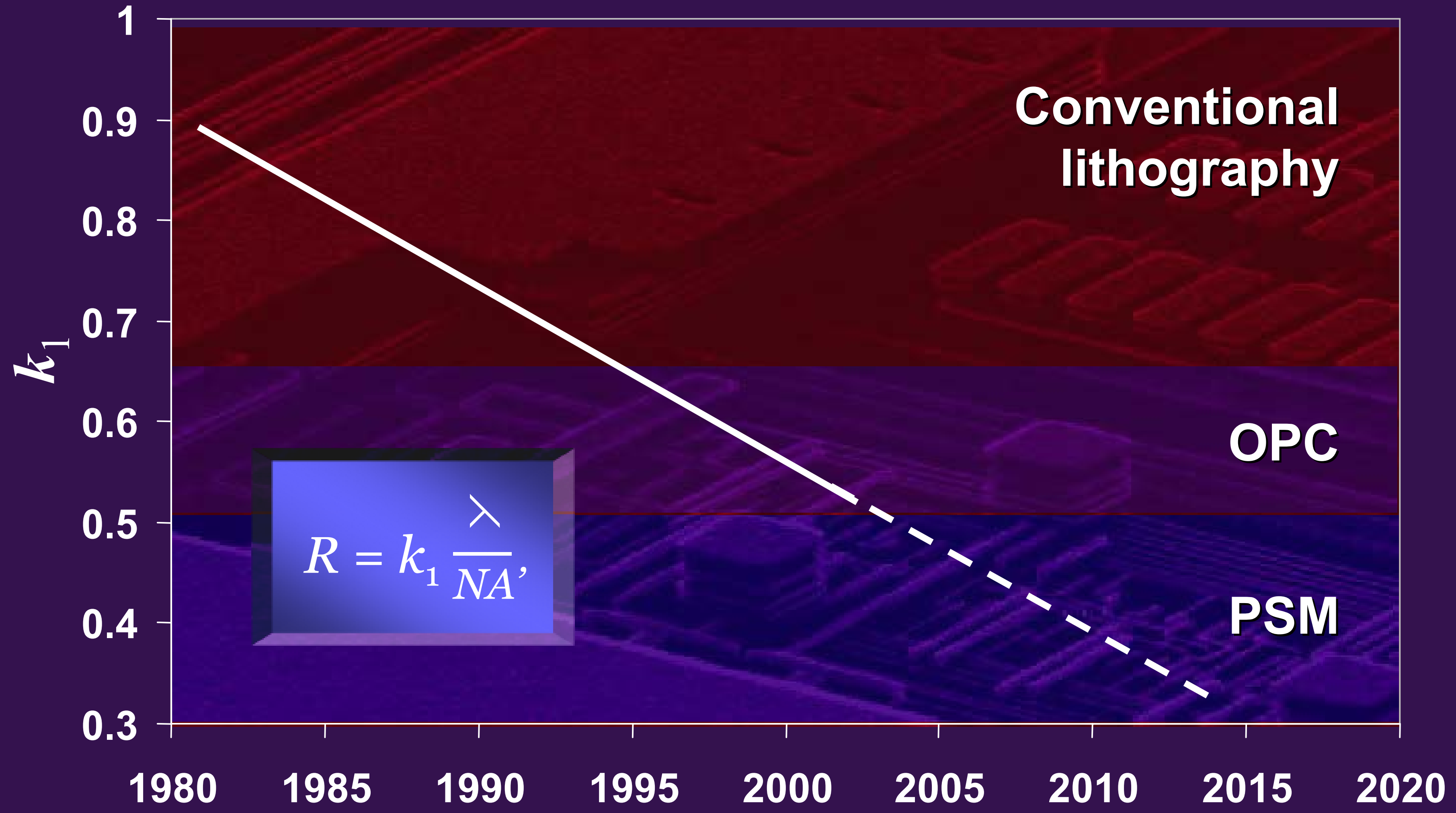
- Mask synthesis
- Dealing with variability
  - Statistical timing analysis
  - Physical design for yield / reliability

Mask Synthesis - RET

248nm Stepper

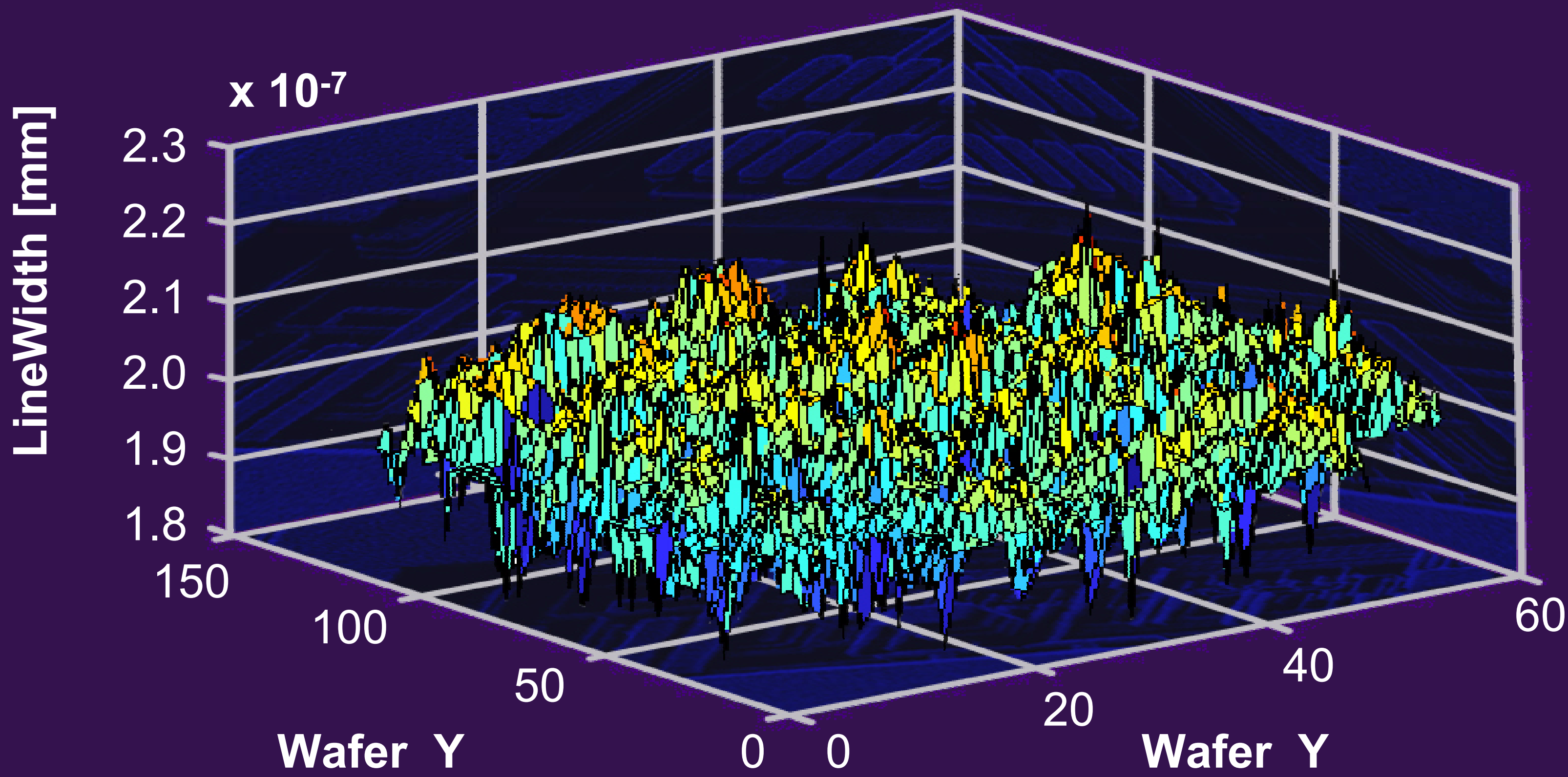


Evolution of RET



CD Variation Across a Wafer

Wafer Map for No-DPC Horizontal Isolated Structures



Incorporate analysis of timing variation into statistical timing analysis

Source: Spanos, UCB

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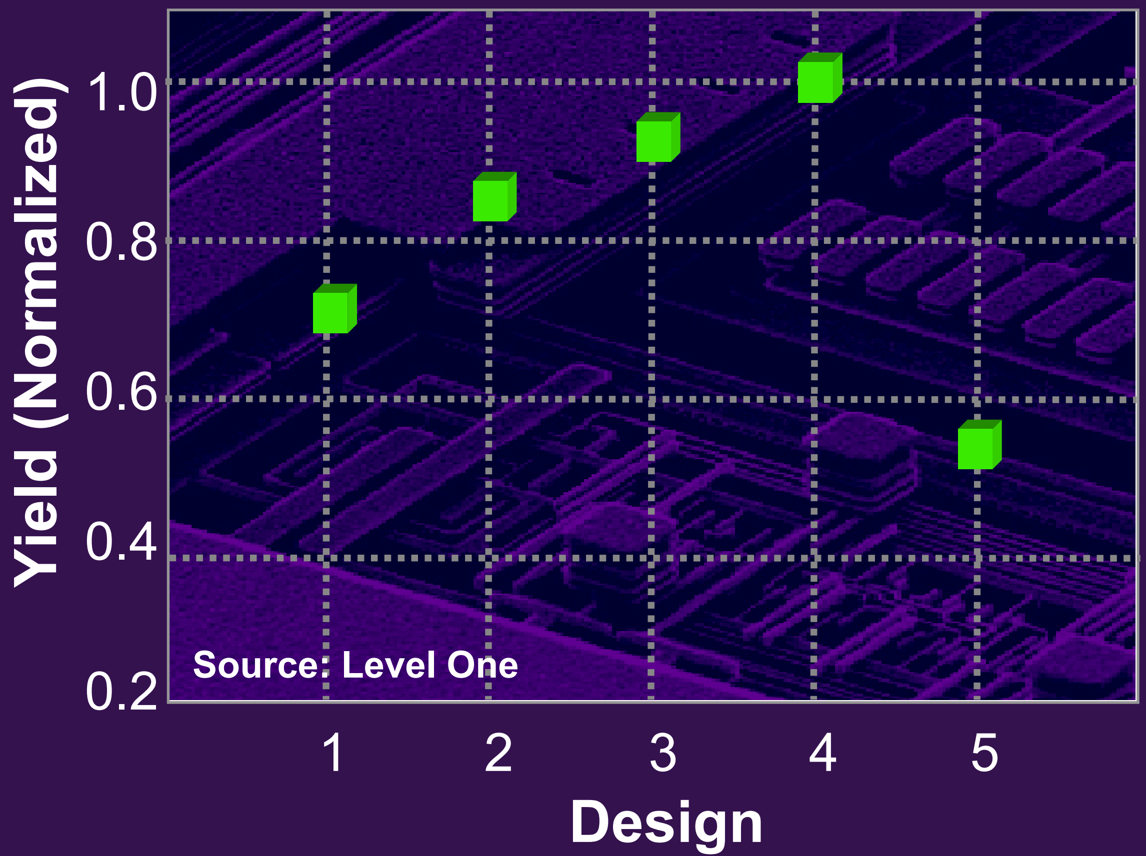
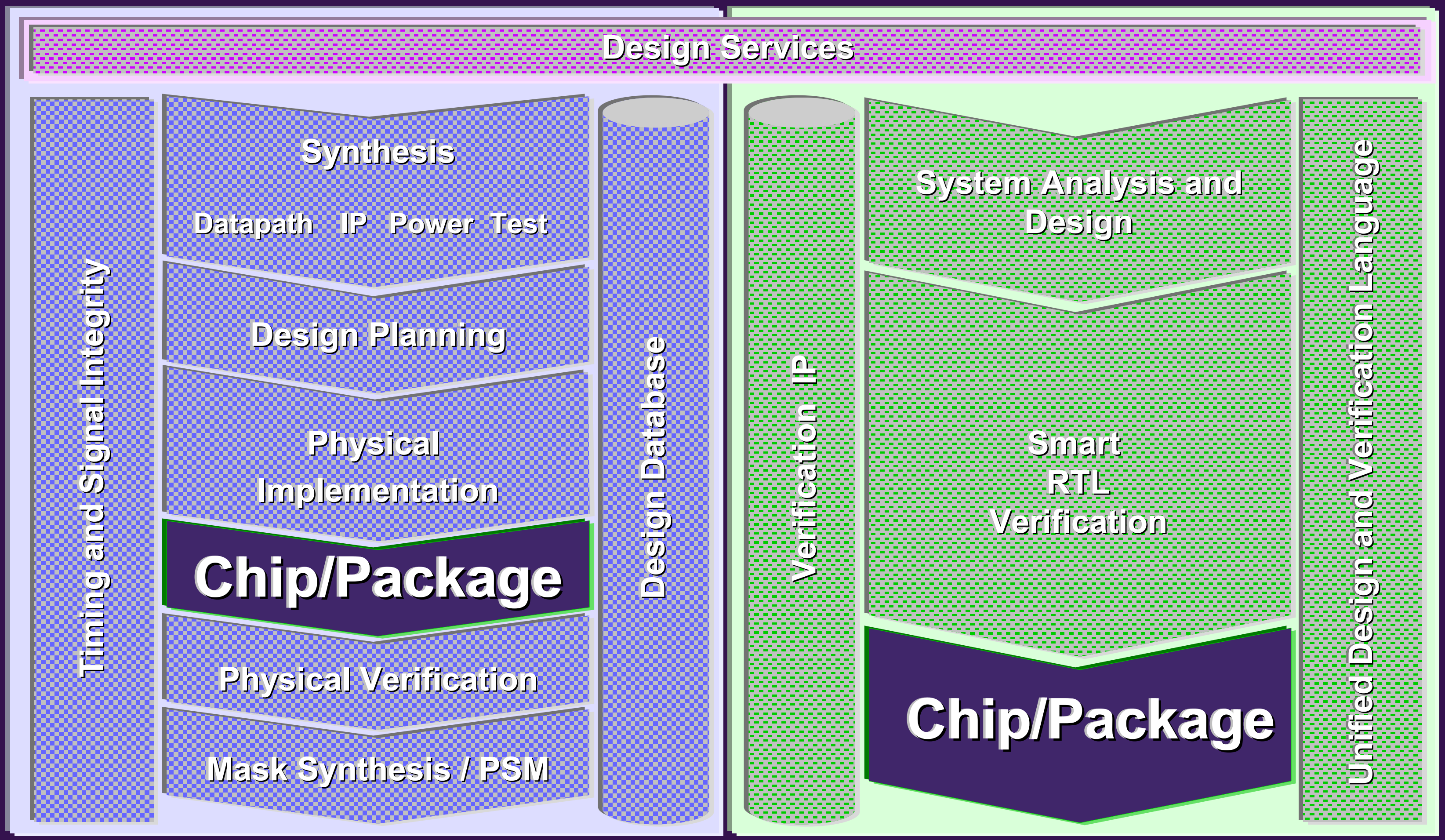
Physical Design for Yield

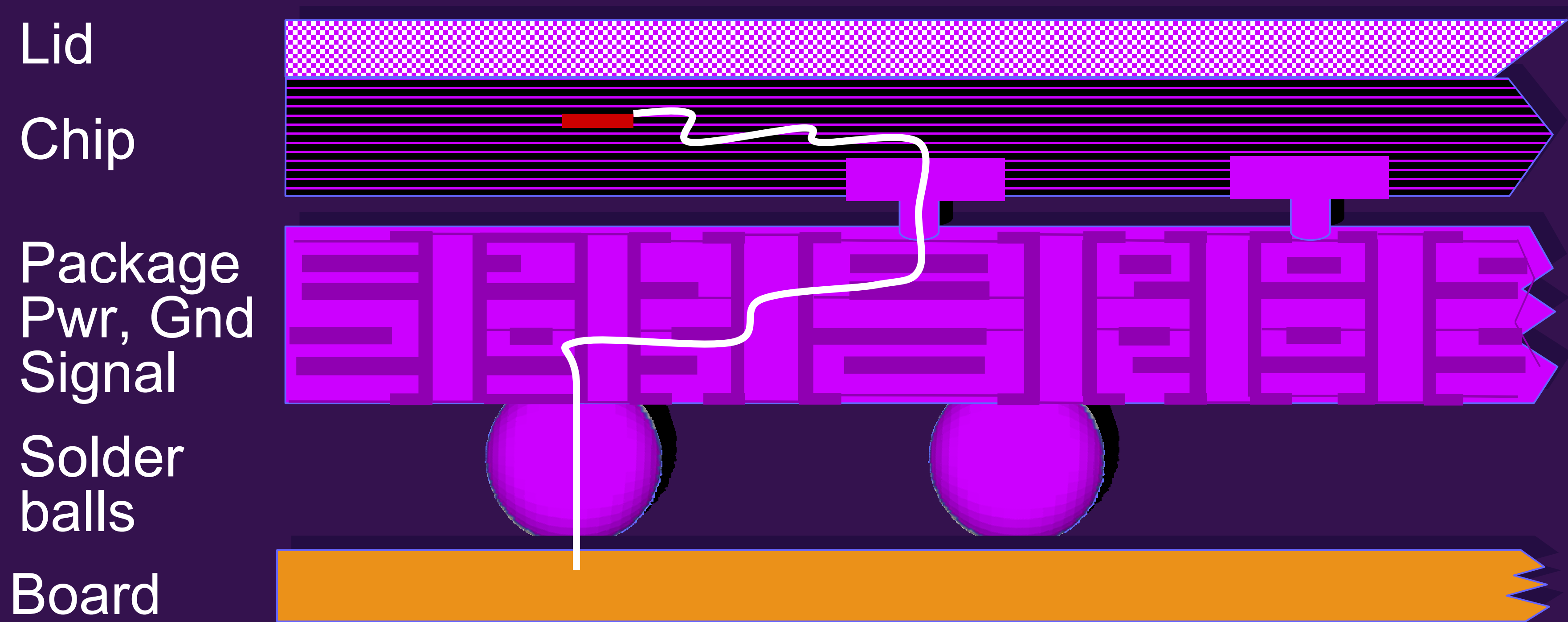


- Multiple vias
- Wire spacing
- Wire width
- Limit current density
- …

IC / Package Co-Design



IC / Package Co-Design for Flip Chip



- Analyis
  - Extraction RLC
  - Simulation Spice
- Design
  - Package feasibility
  - Bump patterning, assignment
  - P/G assignment
  - Driver placement
  - Routing

Summary:
130 / 90 / 65nm Require Many Changes

- Methodology
  - IP, central data base, hierarchy
- Verification
  - Simulation, test benches, formal verification
- Design
  - Timing closure and signal integrity
  - Low power design flow
  - Analog design flow
  - Build in chip-level self test
  - Design for manufacturability
- Chip / package design

