MPSOC ‘ 2003
July 7th, 2003

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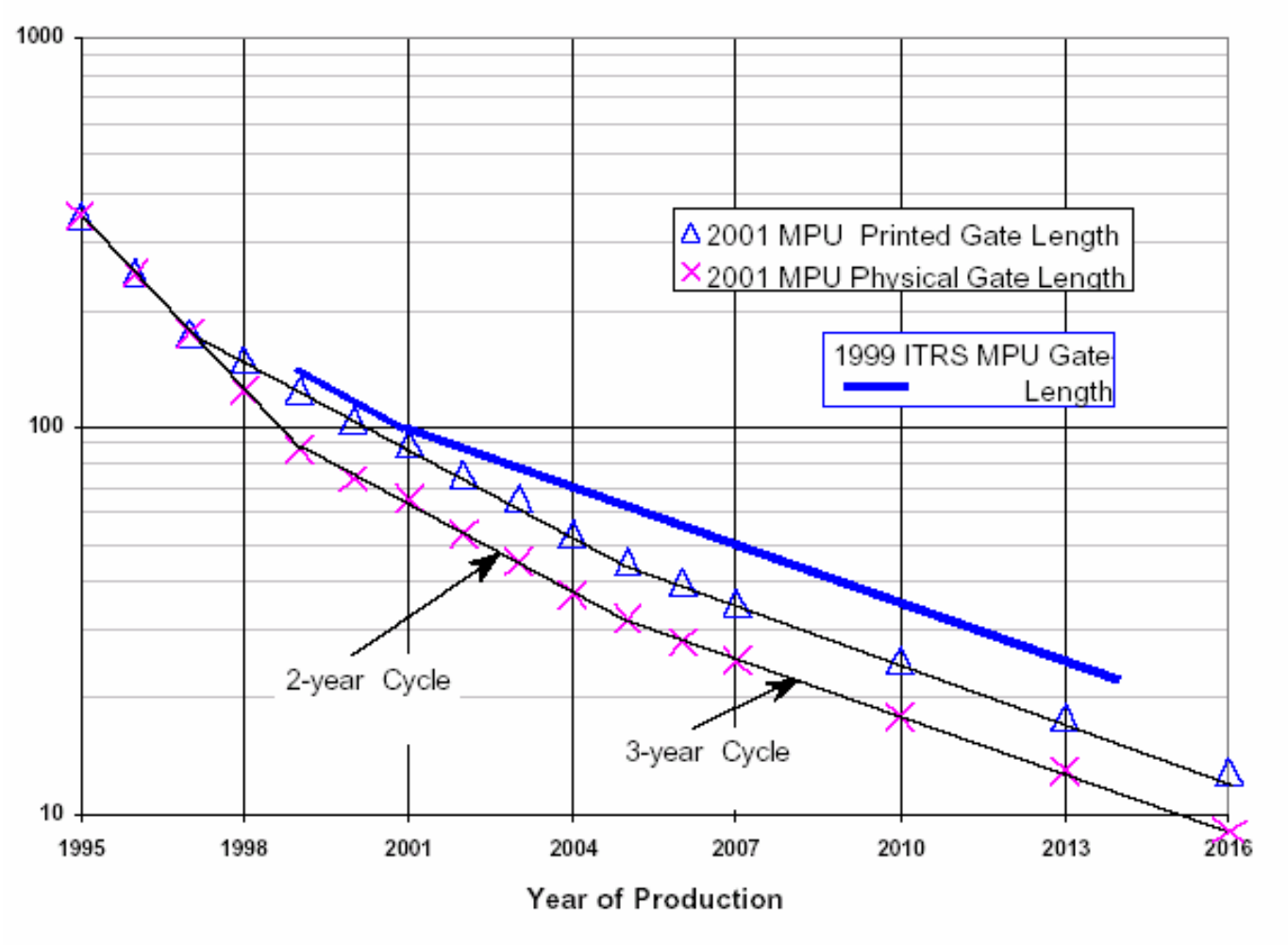
STMicroelectronics

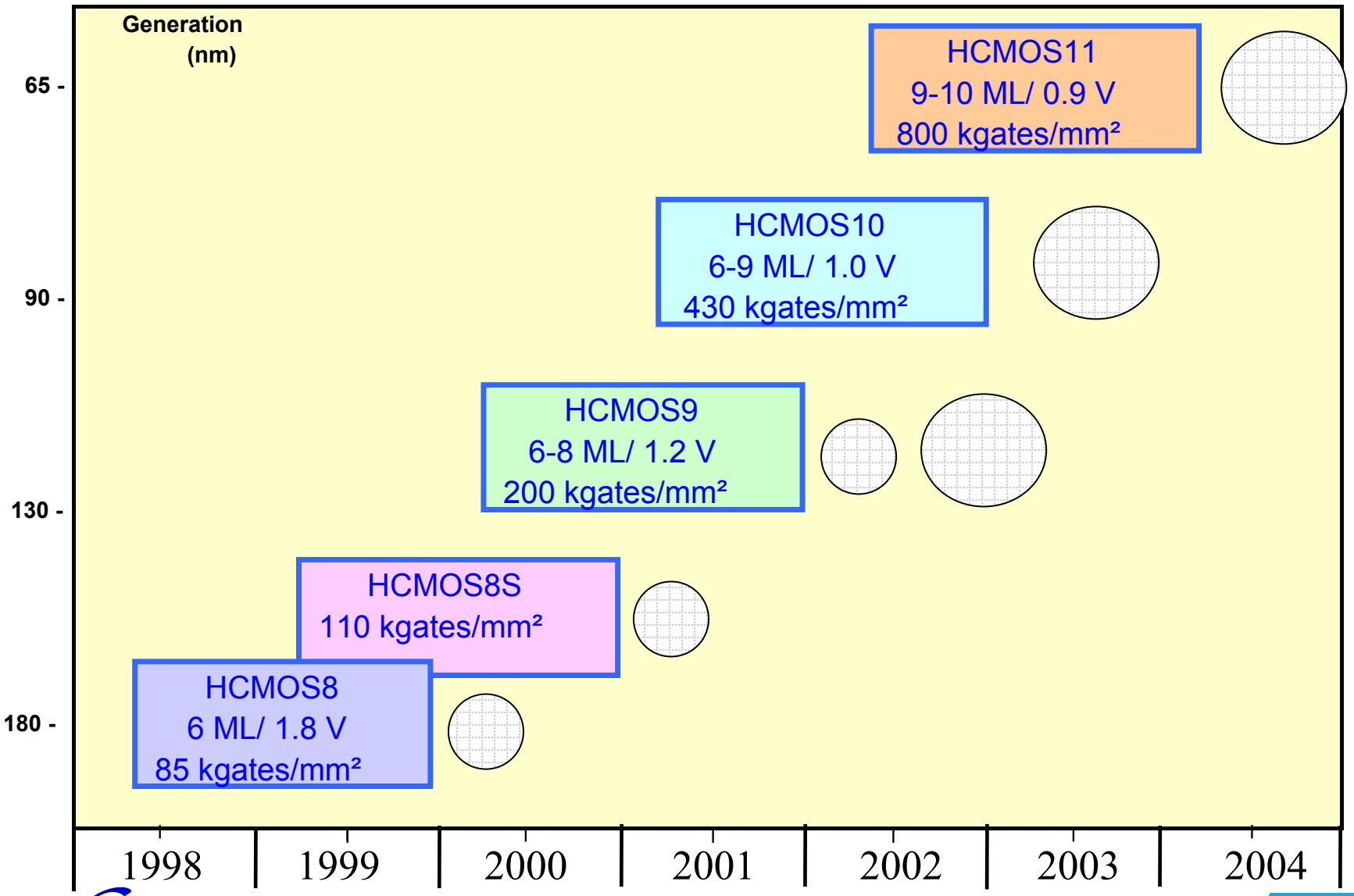
Agenda

- SoC trends and links with process/design
- RTL-to-Layout and cell Libraries trends
- System-level, IP reuse and HW-SW codesign
- Off-roadmap activities
- Conclusions

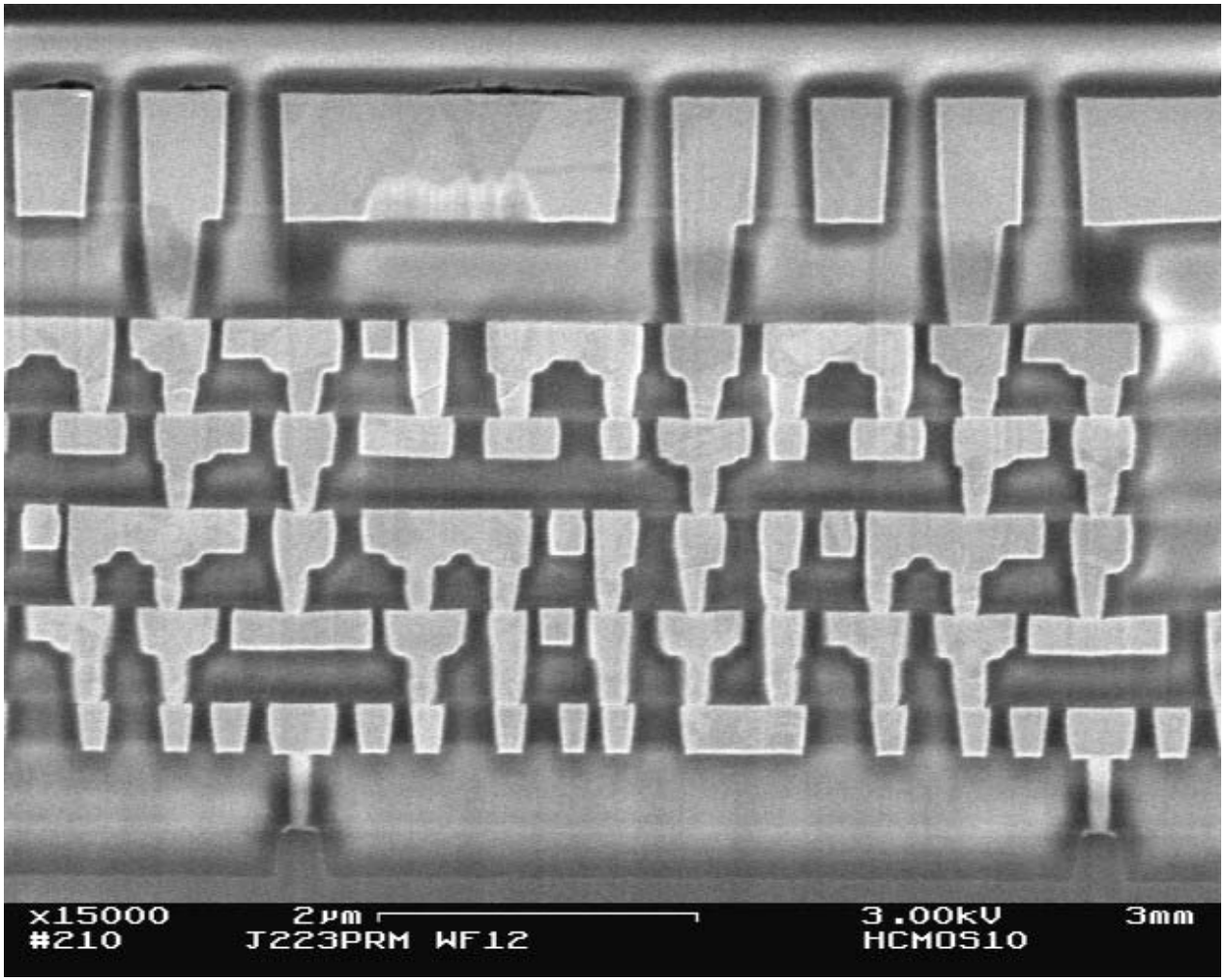
ITRS Roadmap – Gate length



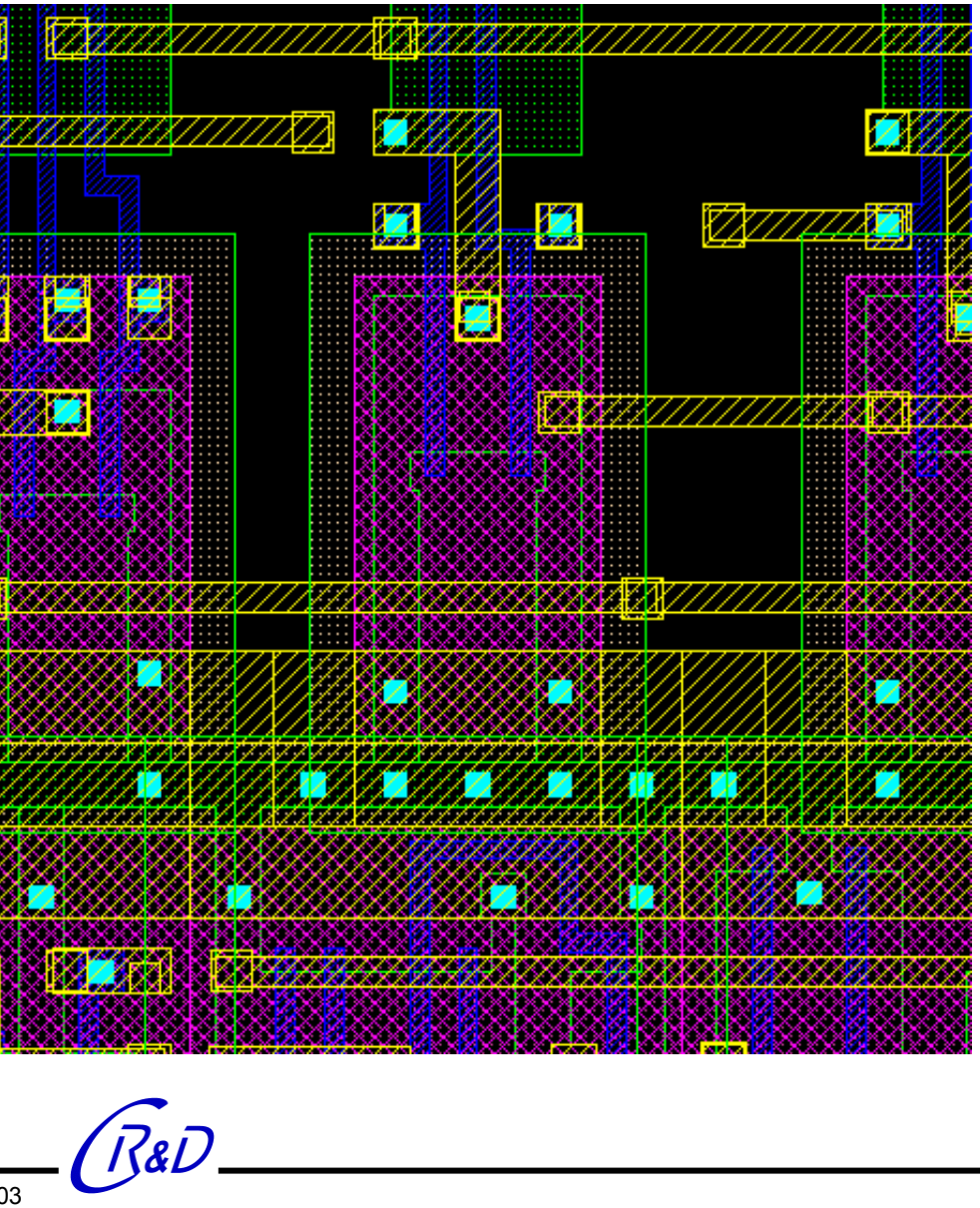
CMOS roadmap



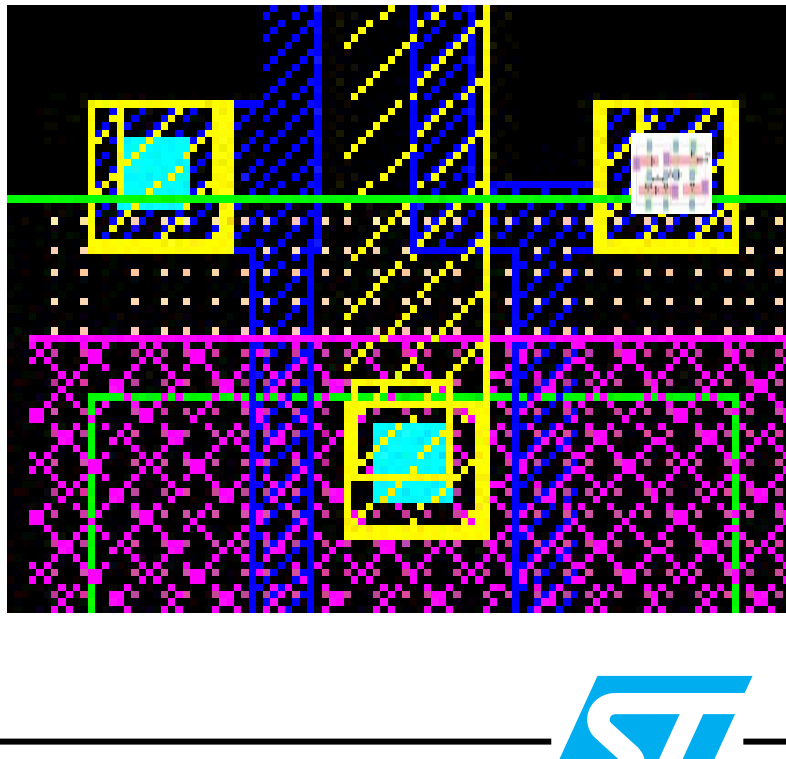
90nm full SiOC/Cu interconnect



0.5um vs 65nm Design Rules



Contact

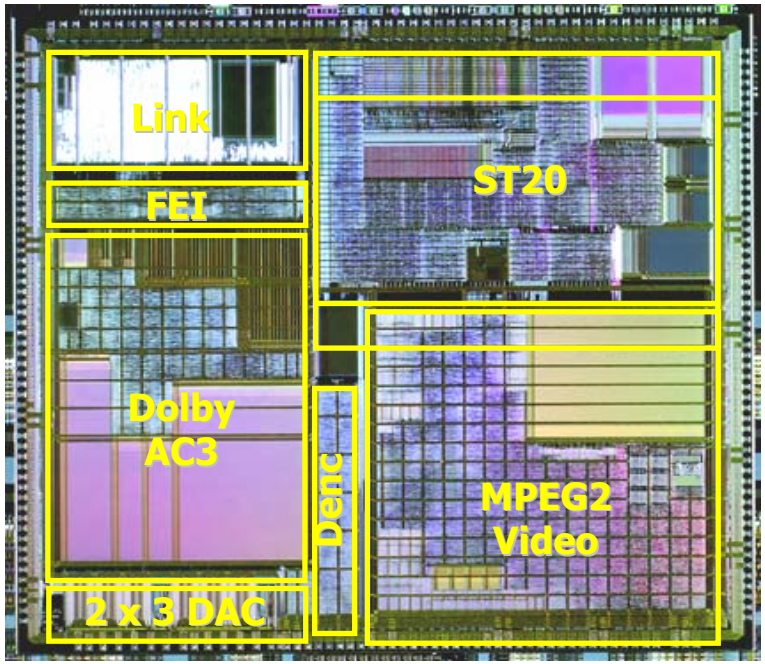


SoC at the heart of conflicting trends

Time-to-market:

Process roadmap acceleration

Consumerization of electronic devices



Complex systems:

uCs, DSPs HW/SW

SW protocol stacks

RTOS's

Digital/Analog IPs

On-Chip busses

Process options explosion (analog, RF, imagers, …)

Deep sub micron effects:

crosstalk

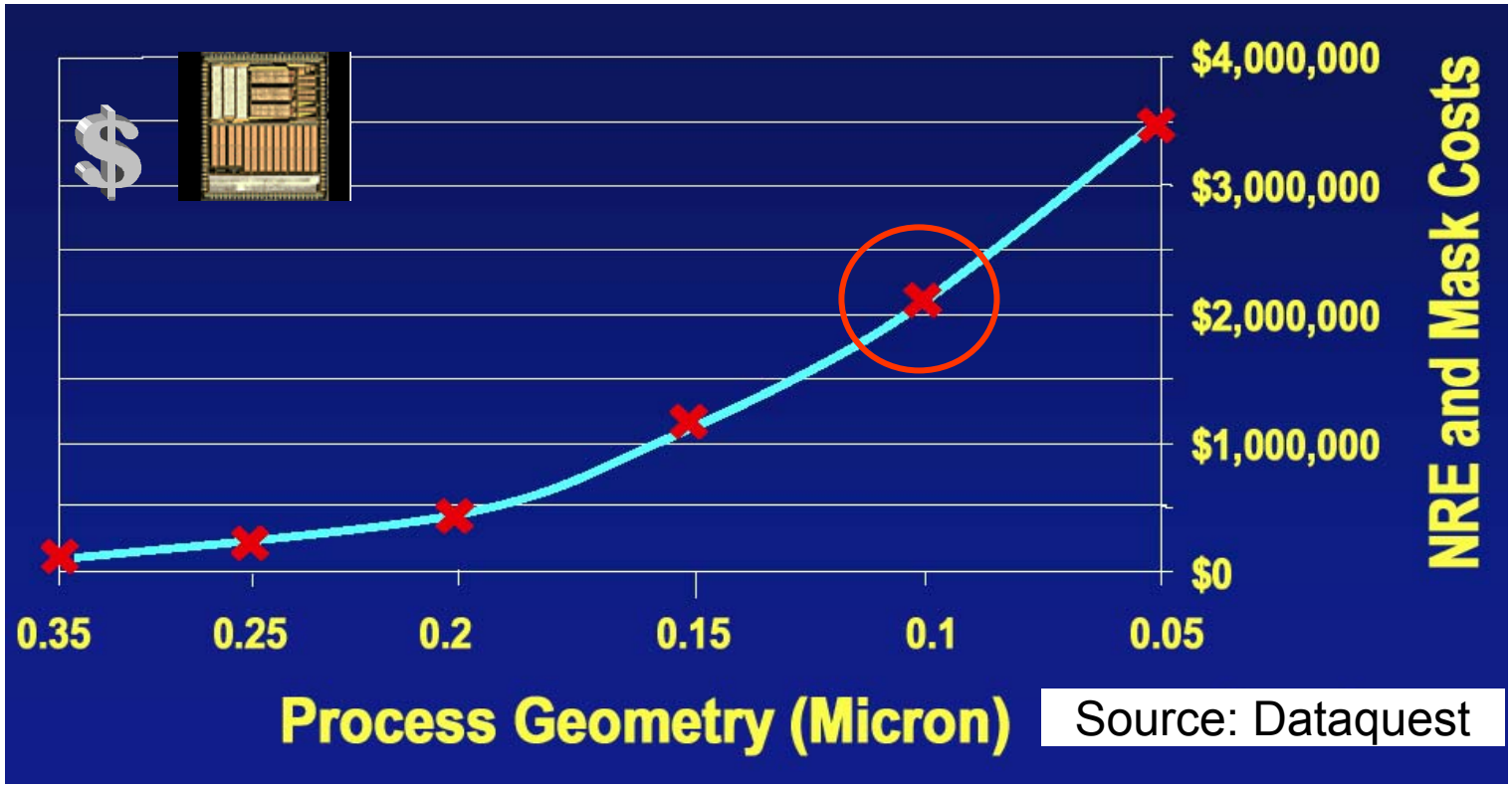
electro migration

wire delays, on-chip-variation

mask costs (OPC, PSM)

copper wires

SoC Economic Trends: Mask NRE

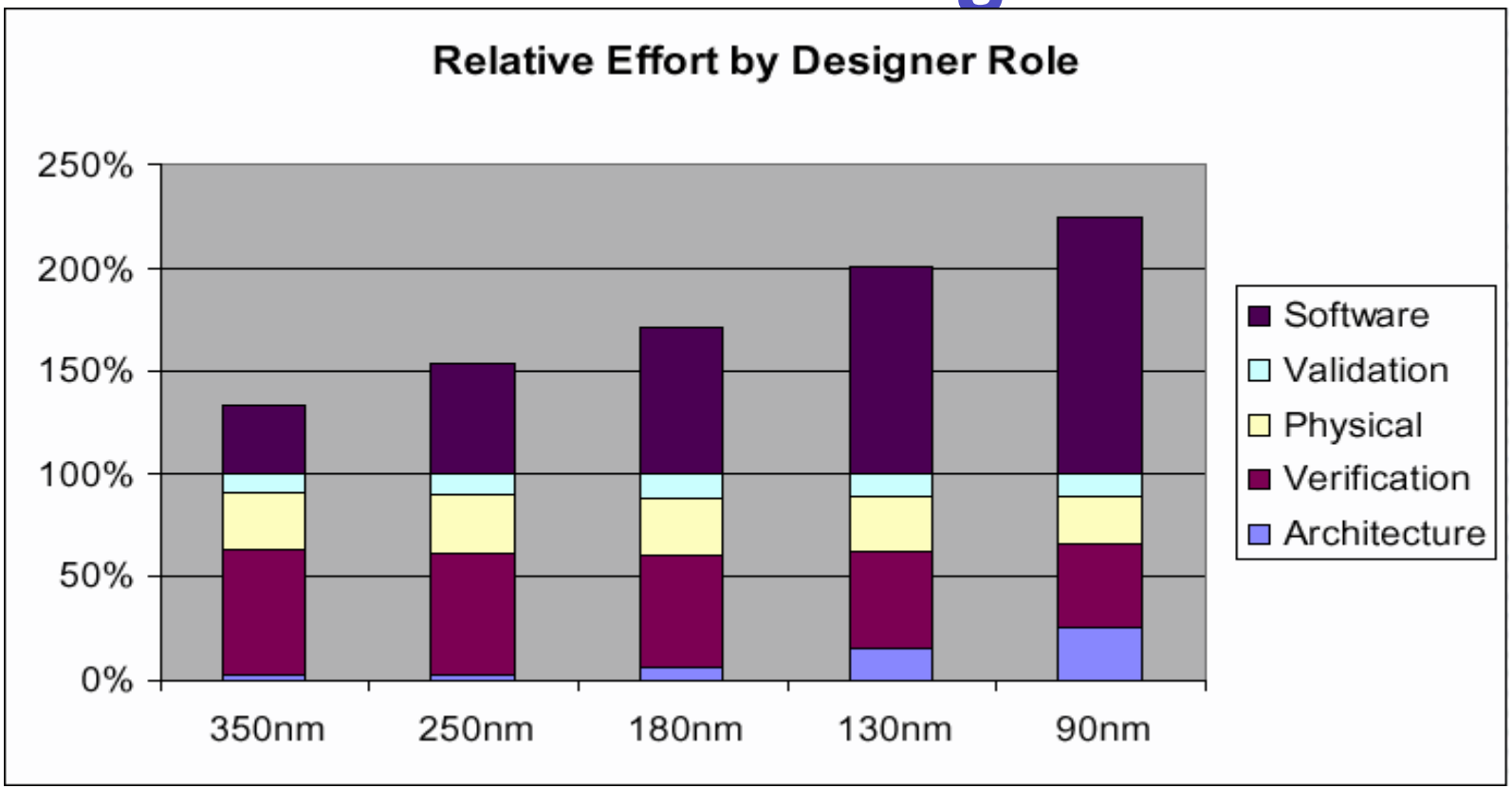


– For $5 ASP with 25% profit margin:
  Need to sell over 1.6M parts to break even

Ideas to Minimize Mask costs

- Share mask costs for prototyping
  - Shuttles
  - Several layers on same reticle
- Share mask costs for production ?
  - With other ASICs (in same chip-set, similar volumes …)
  - For same ASIC, put several non critical masks on same reticle
- For an ASIC family / emerging standards
  - Put variable HW IP in eSoG, eFPGA
- Mask-less programming

SoC Design + Rising Complexity = New Challenges

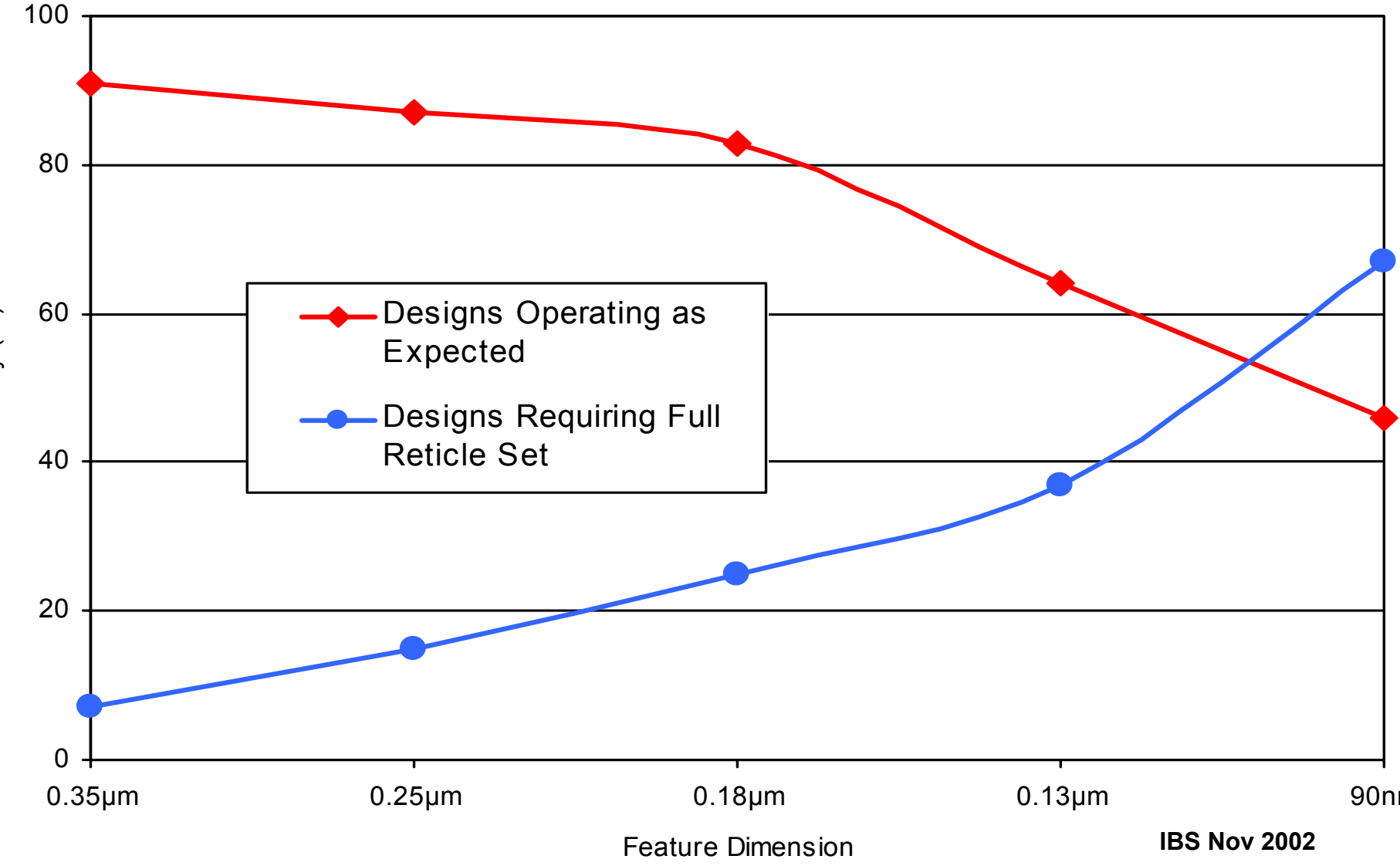


IBS Nov 2002

* Architecture effort overtakes physical design at 90nm

* Software costs overtake total hardware costs at 130nm

ROBABILITY OF DESIGNS OPERATING A EXPECTED



IBS Nov 2002

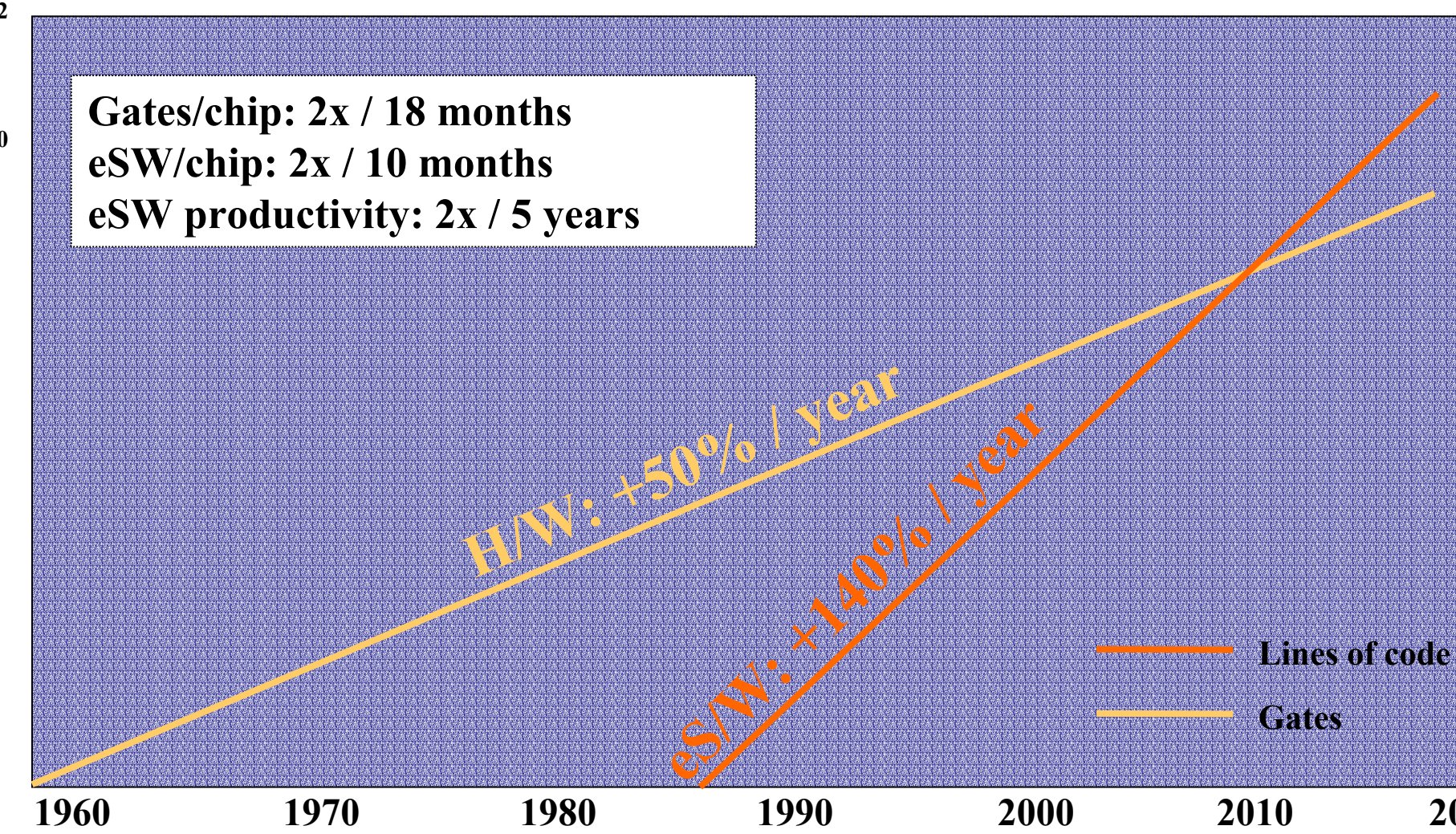
Key Trends: ASICs down, Multi-processors & FPGAs up

- ASIC/ASSP ratio: 80/20 in 2000, 50/50 in 2003
- Telecom company trends
  - In-house ASIC design way down
  - Replace by commercial off-the-shelf, programmable ASSP
  - High-end NPU's used in non-NPU applications
- Number of embedded processors in SoC rising:
  - ST: recordable DVD 5
  - Hughes: set-top box 7
  - ST: HDTV platform 8
  - Latest mobile handsets 10
  - NEC: Image processor 128
  - In-house NPU >150

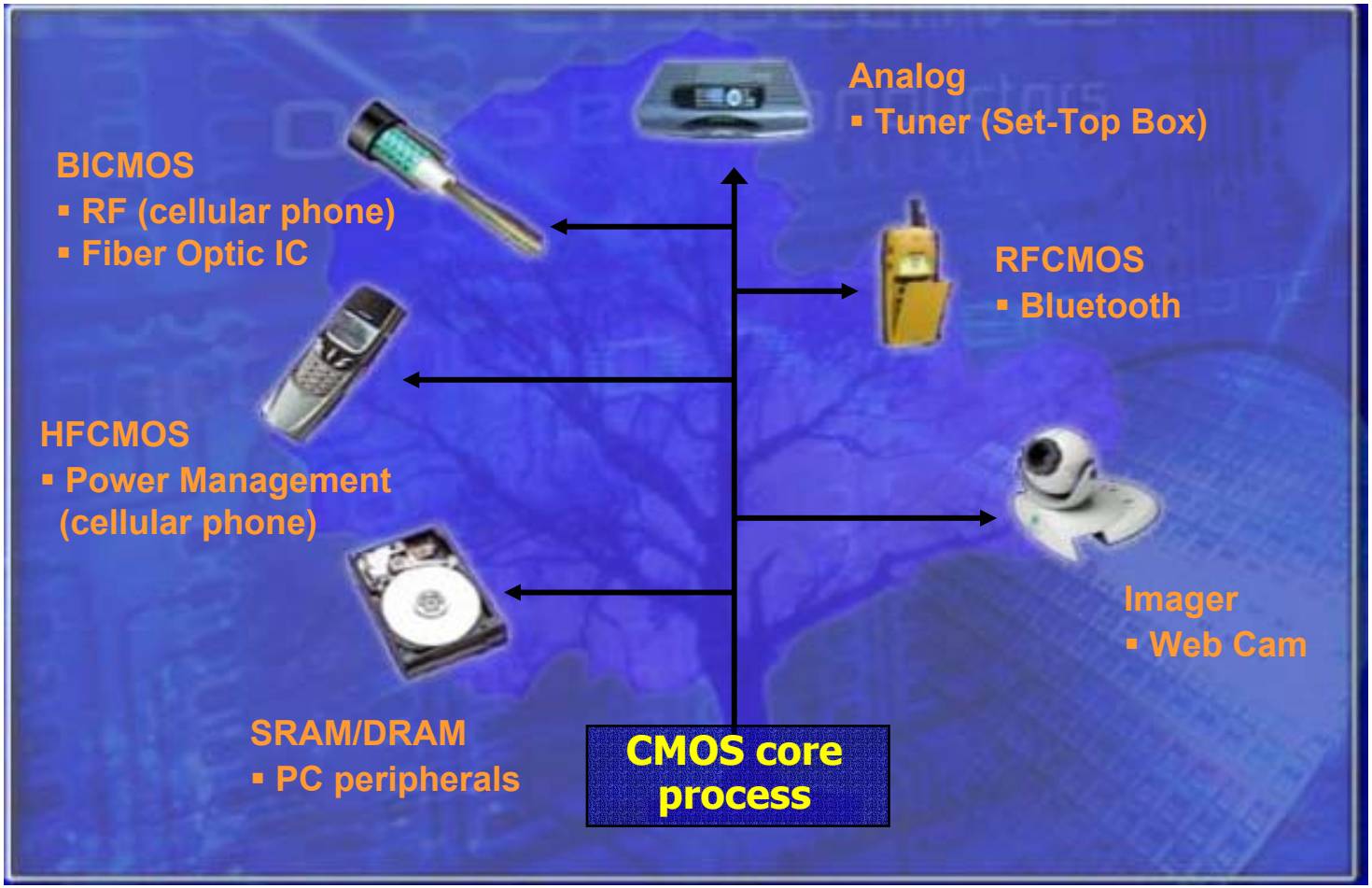
Key Trends: Embedded S/W content in SoC is way up

- eS/W: Current application complexity
  - Set-top box: >1 million lines of code
  - Digital audio processing: >1 million lines of code
  - Recordable DVD: Over 100 person-years effort
  - Hard-disk drive: eS/W represents 100 person-years effort
- In multimedia systems
  - S/W cost (licenses, royalties) 6X larger than H/W chip cost
  - eS/W uses 50% to 80% of design resources
- eS/W has become an essential part of SoC products
- Software reuse essential now
- Software architecture becoming important
- Memory now dominating die area

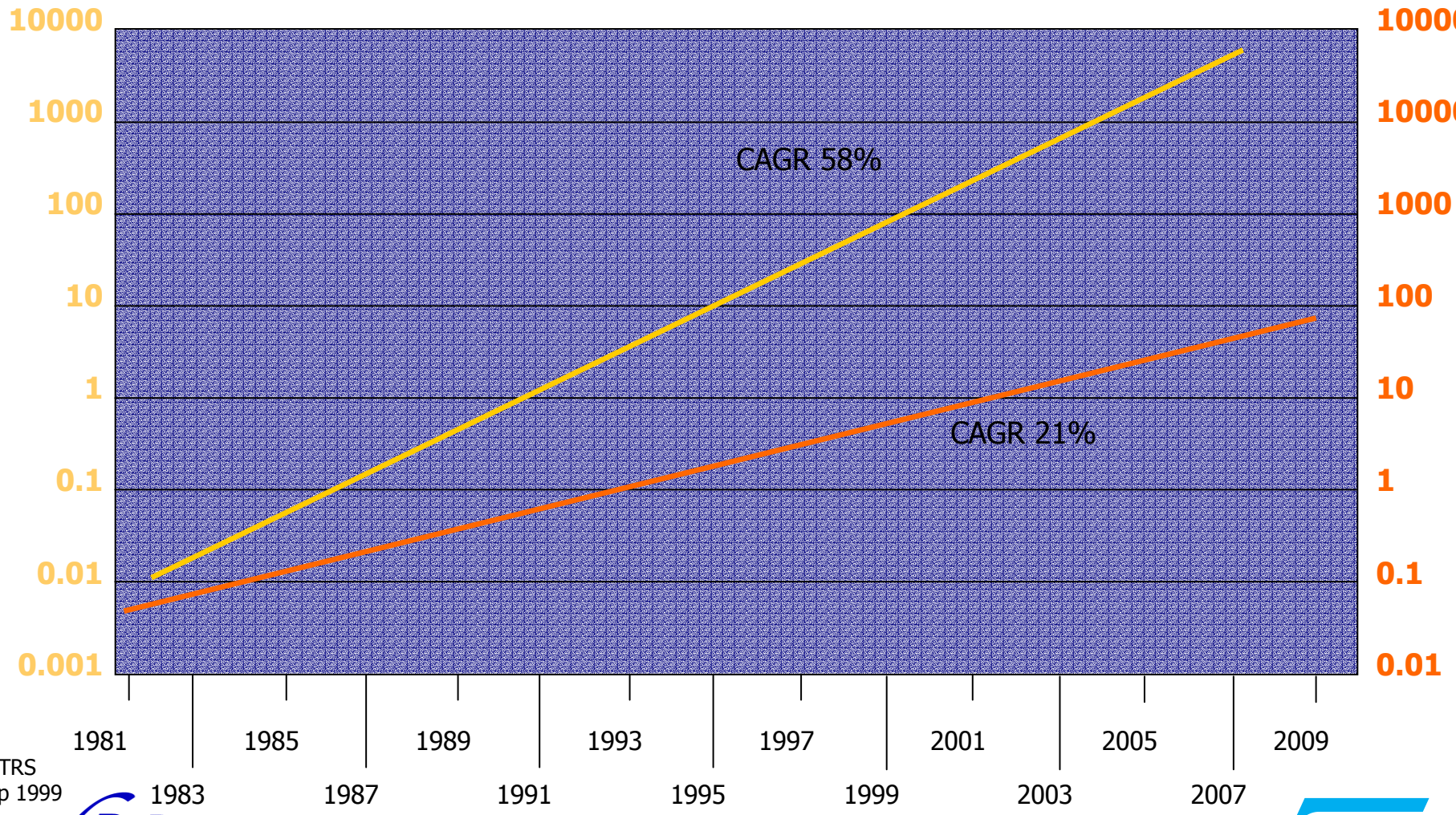
S/W and H/W Complexity Factors



Extending Core CMOS for SOC



Consequence: The Design Productivity Gap



TRS
p 1999

Agenda

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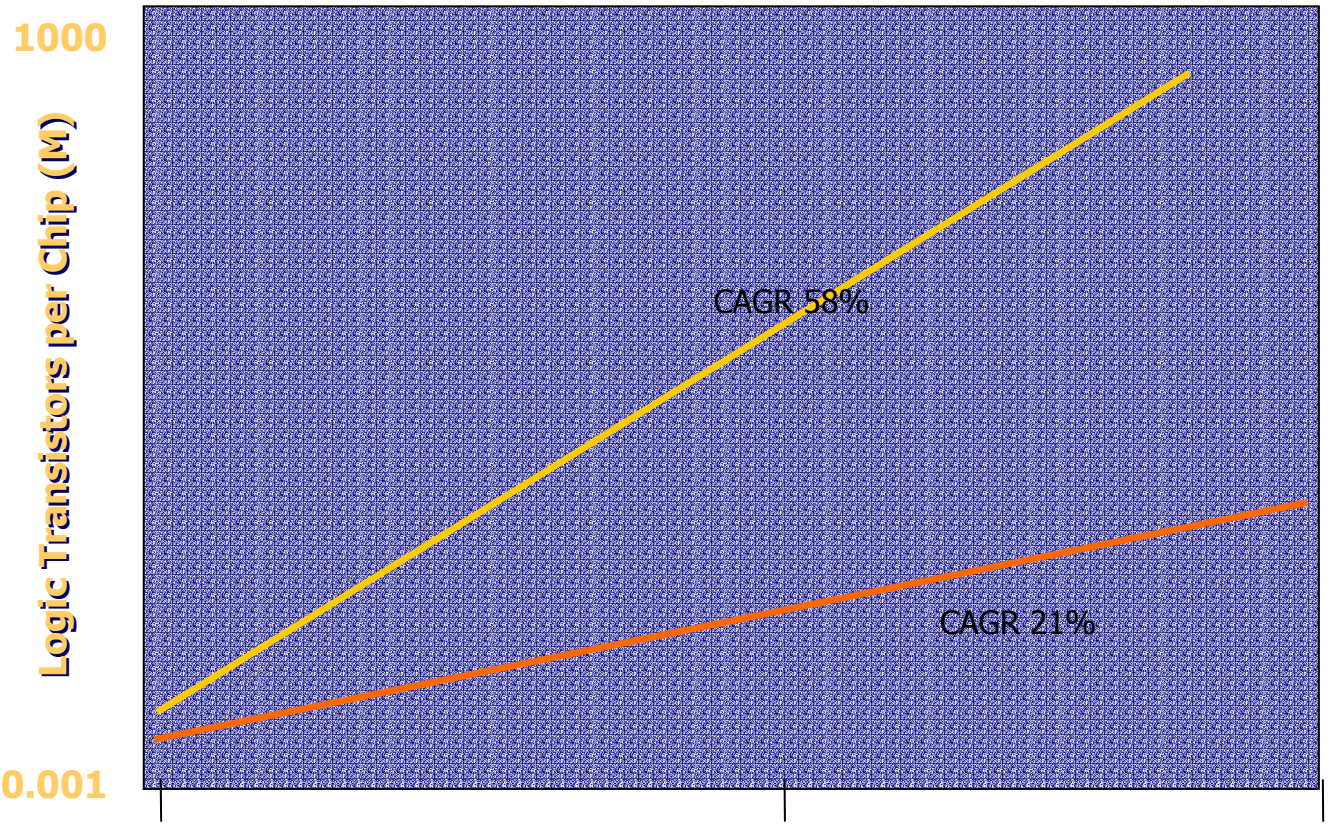
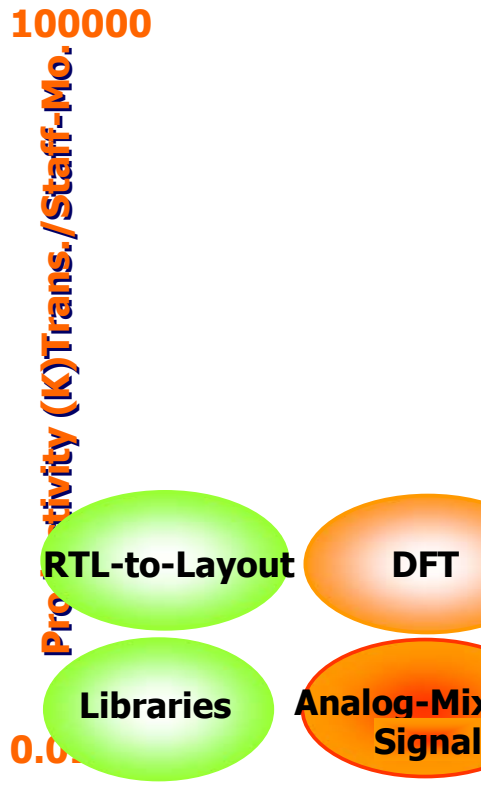
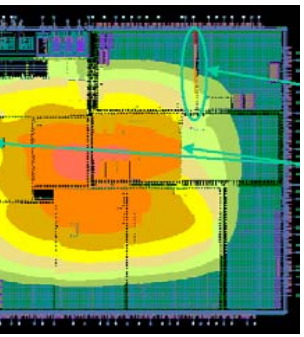
Staying on the Productivity Curve

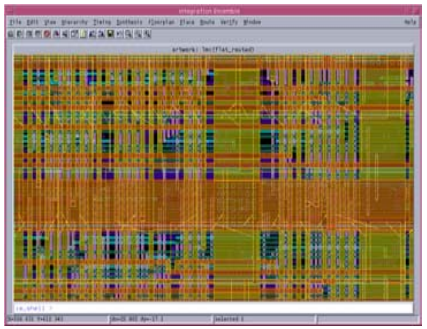




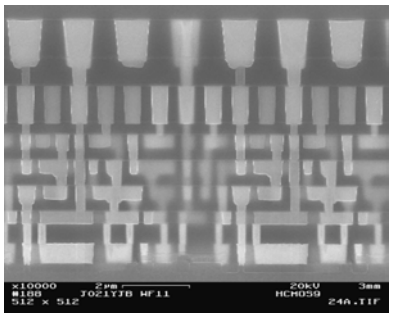
Deep Submicrons Effects modeled in 0.13um



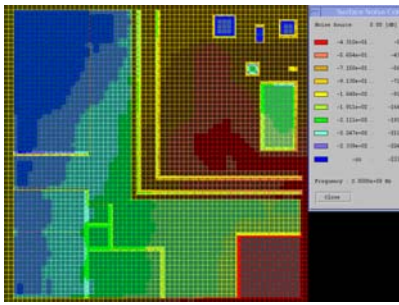
/oltage Drop
& EMG



Copper Routing



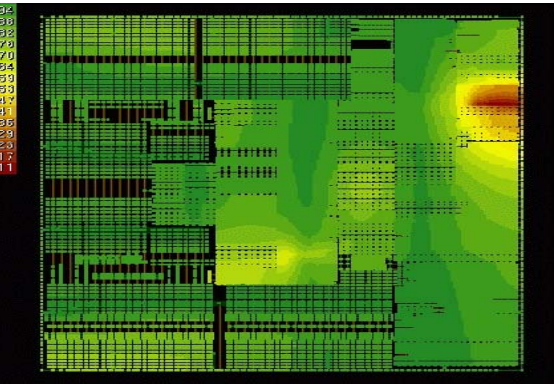
Cross Talk
effects

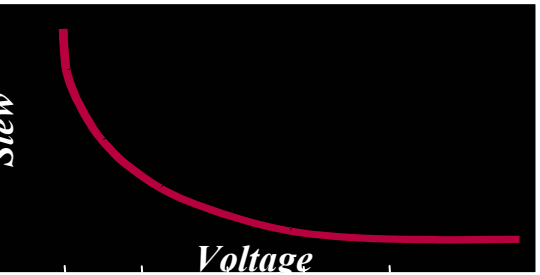


Substrate Noise

New Timing Effects (90nm)

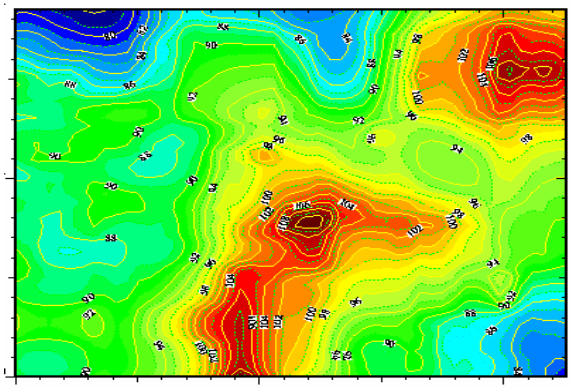
Voltage on-chip-variations

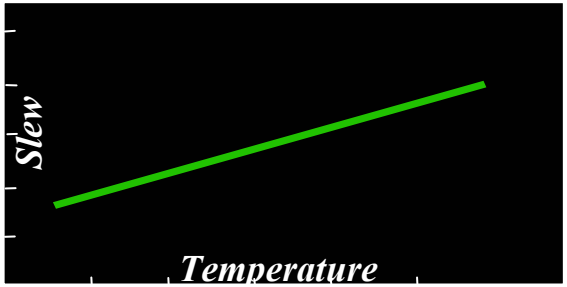




5% voltage change → 15% change in slew

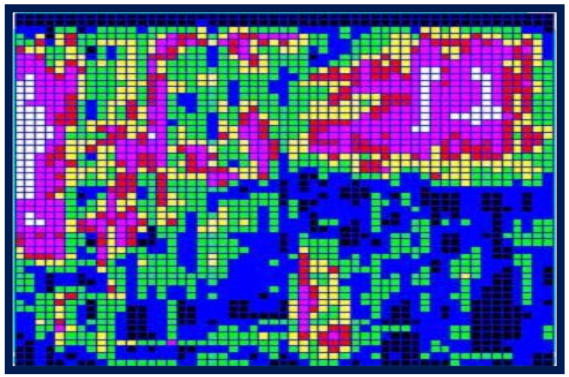
Temperature Map

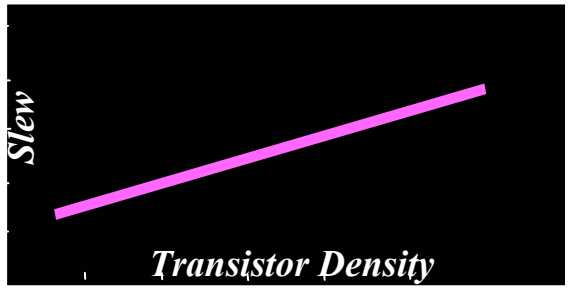




30° C change → 7% change in delay & slew

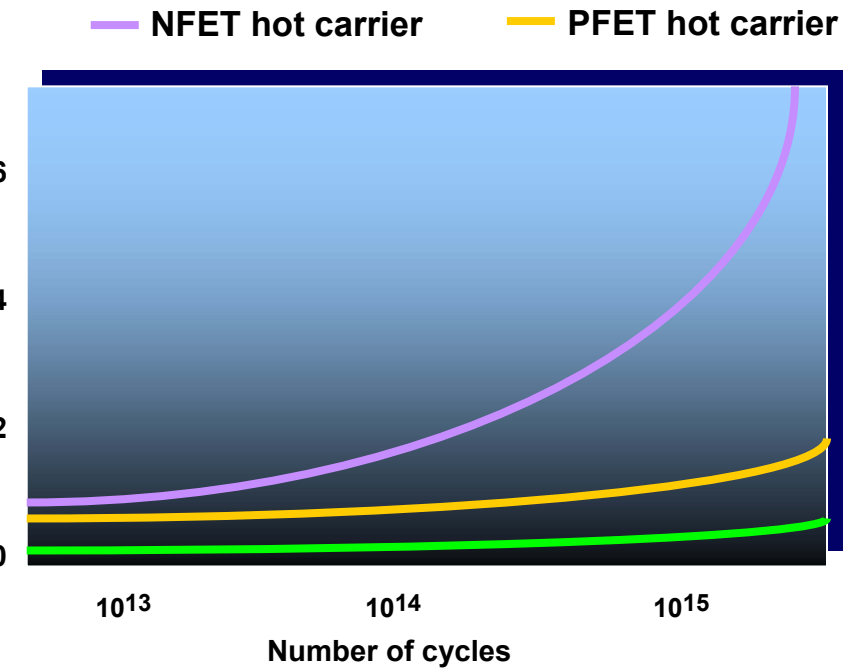
Transistor Density





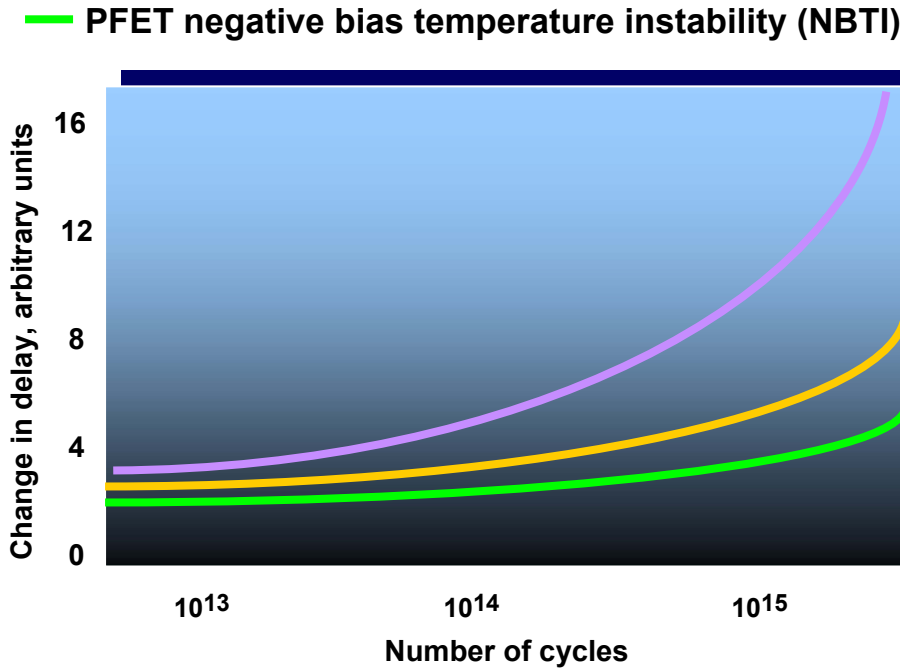
50% density change → 15% change in slew

Reliability effects in 0.13um



Ring oscillator change in delay vs. number of cycles @30°C.

At room temperature, NFET wear-out delays dominate due to hot carriers. NBTI in the PFET plays a smaller role.

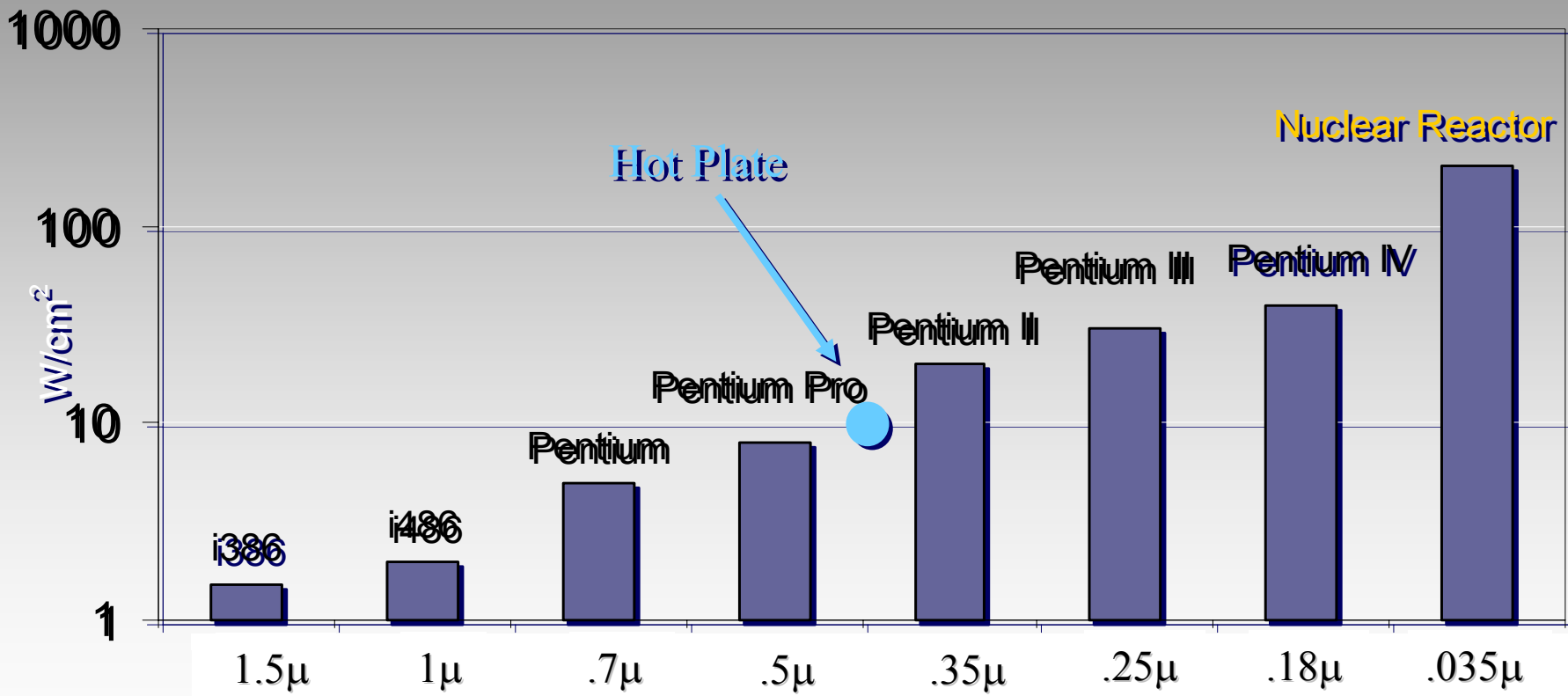


Ring oscillator change in delay vs. number of cycles @125°C.

Stressed to 125°, wear-out delays from NBTI plus hot carriers in the PFET equal delays in the NFET.

Source : IBM Corp.

Power Density in Microprocessors

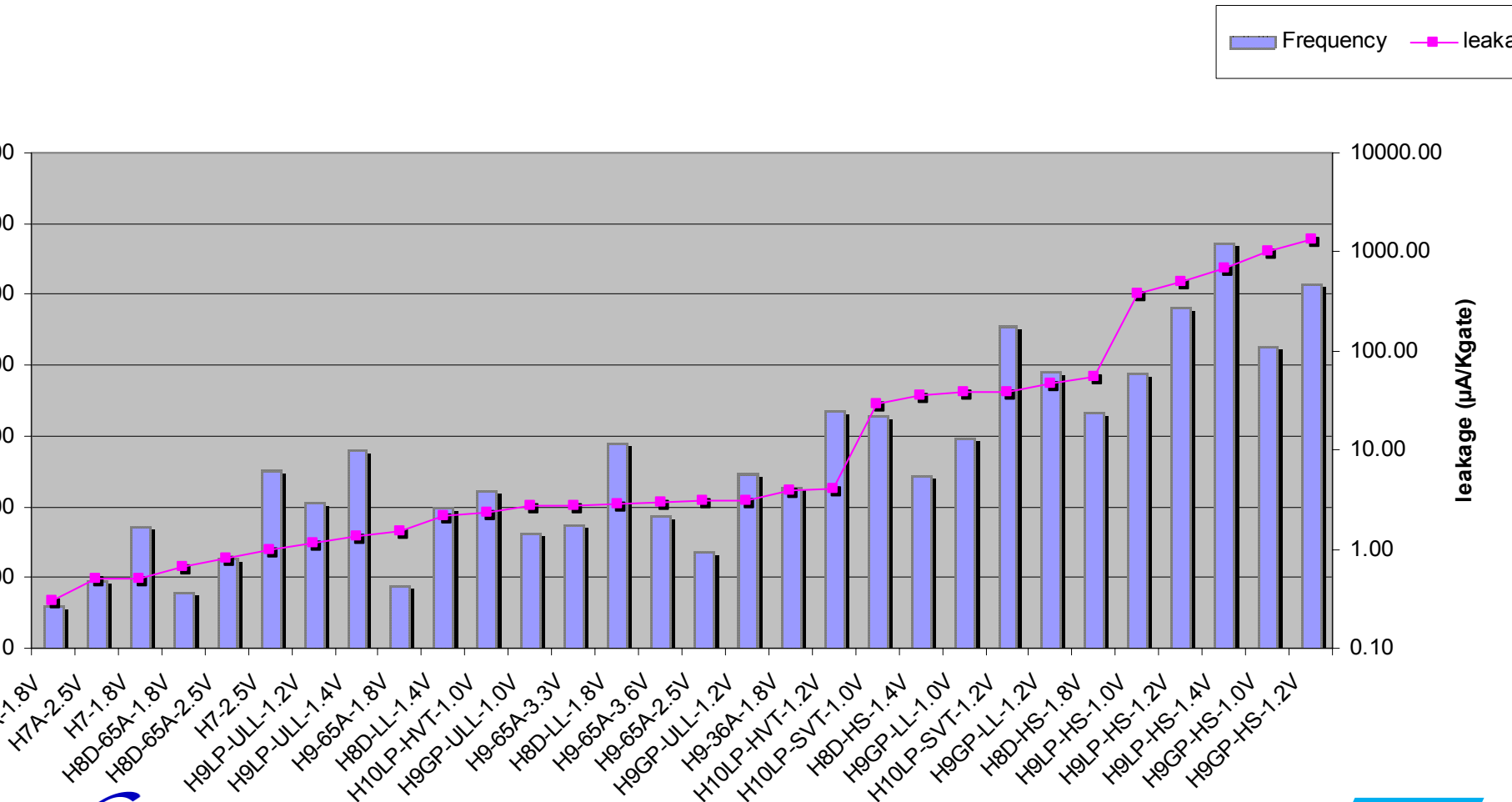


Fred Pollack, Intel

Static versus Dynamic Power

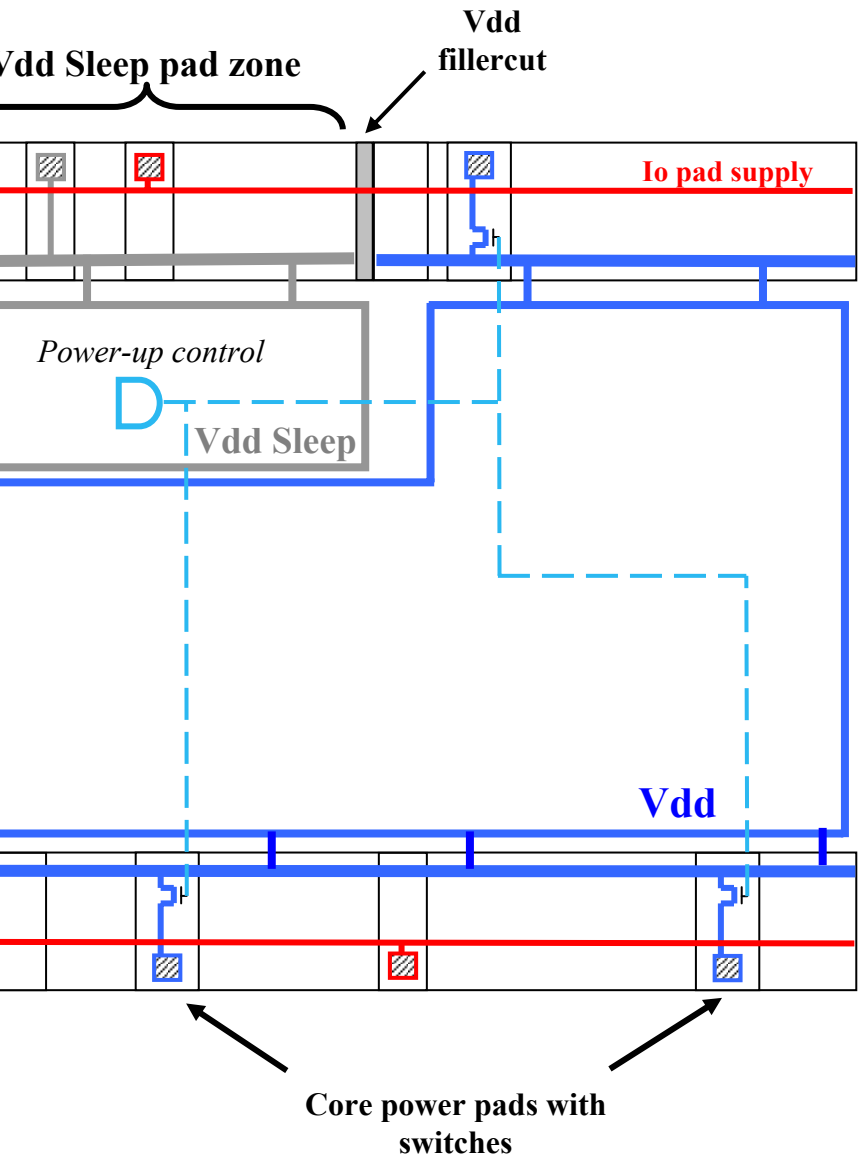
- Dynamic Power per Chip is rather stable due to system limitation: mechanical / battery
- Dynamic Power is under control:
  - VDD is decreasing (slowly)
  - Power management is in practice (clock gating, power shut down, …)
- Static Power is not under control: natural leakage of transistor multiplied by 10 every 2 years:
  - Power shut down is the best way to cut leakage
  - Very low voltage retention or zero leakage Non Volatile memories are potential solutions
- Static Power is becoming as big as Dynamic Power at high temperature (wasted power, no solution)

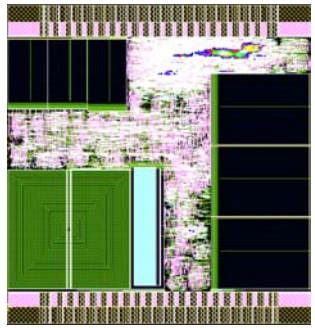
SoC Frequency & Leakage evolution from 250nm to 90nm



technology

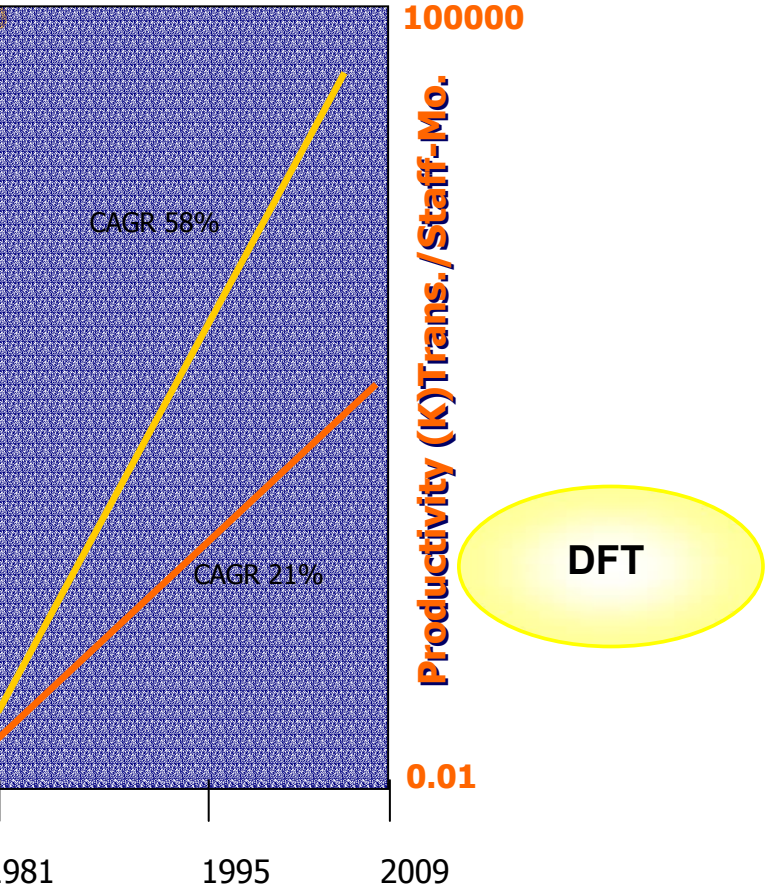
Low-Power techniques for wireless





- Two supply zones: Vdd and VddSleep.
- Specific rules at RTL for boundary between Vdd and VddSleep areas
- Gnd is common for all cells.
- Pads are always powered.
- 3 power pads with embedded switches

Design For Test

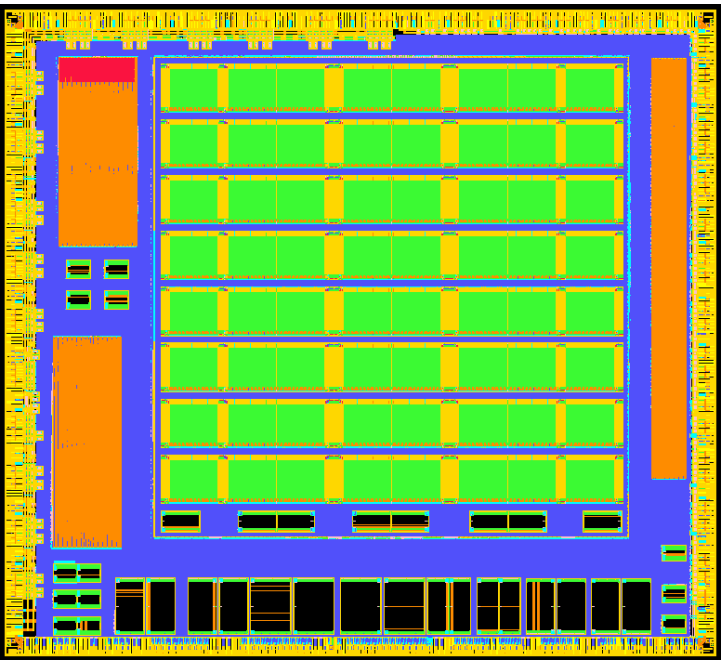


- Memory generators: eSRAM, eDRAM, eROM, eNVM
  - Include BIST generation
  - Redundancy mandatory above 1Mbit
- Logic
  - Scan / ATPG today
  - Commercial tools to reduce tes times by 10X
  - Implementing IEEE P1500 for core-based test
- Design-for-Manufacturing
  - Yield-improving design guidelin under definition

Beyond DFT: Yield management

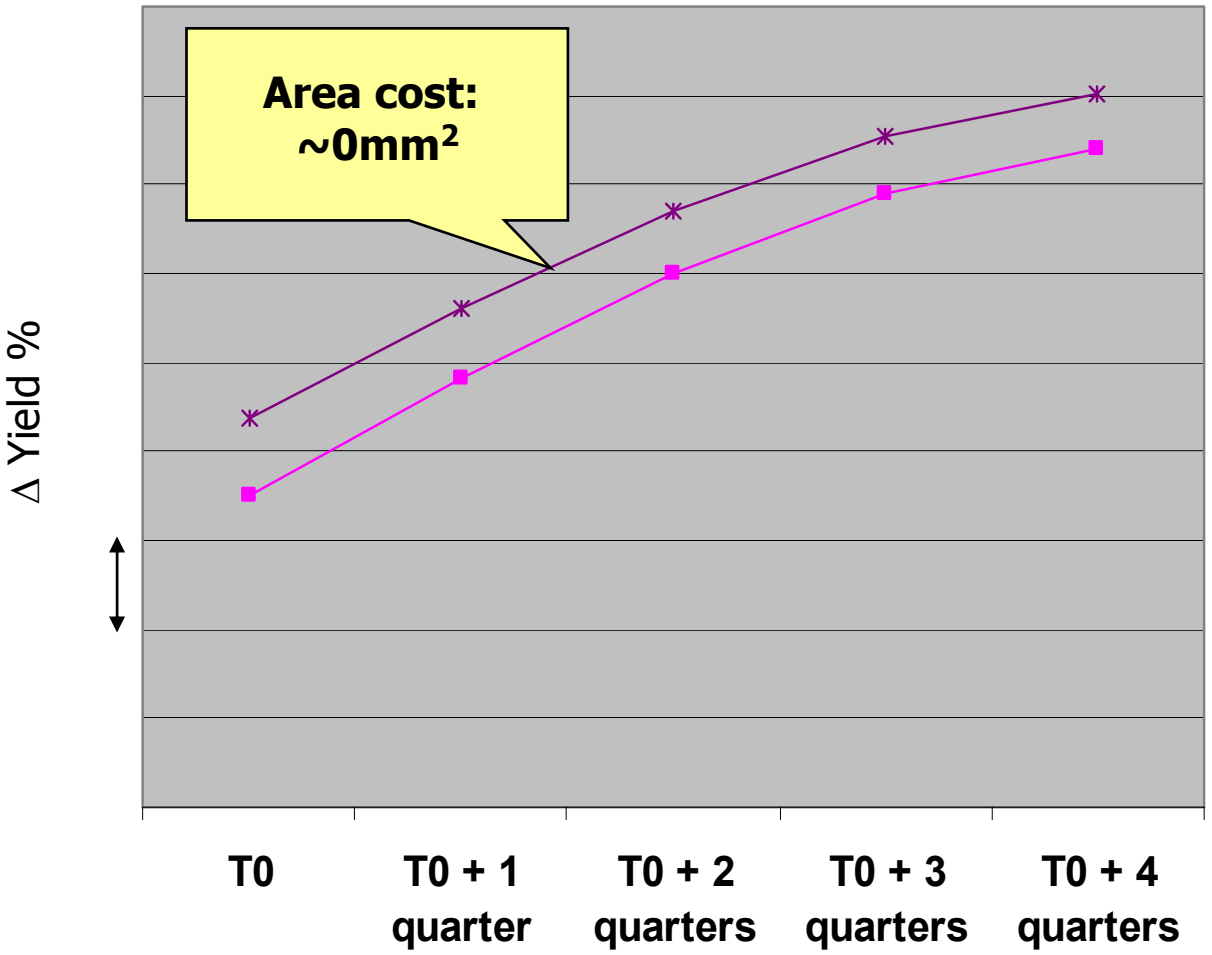
Telecom application example

- **Low yield seen on a complex chip integrating:**
  - **Large number of memory cuts: >50% of chip area**
  - **Small size cuts**
  - **Multiple memory types**

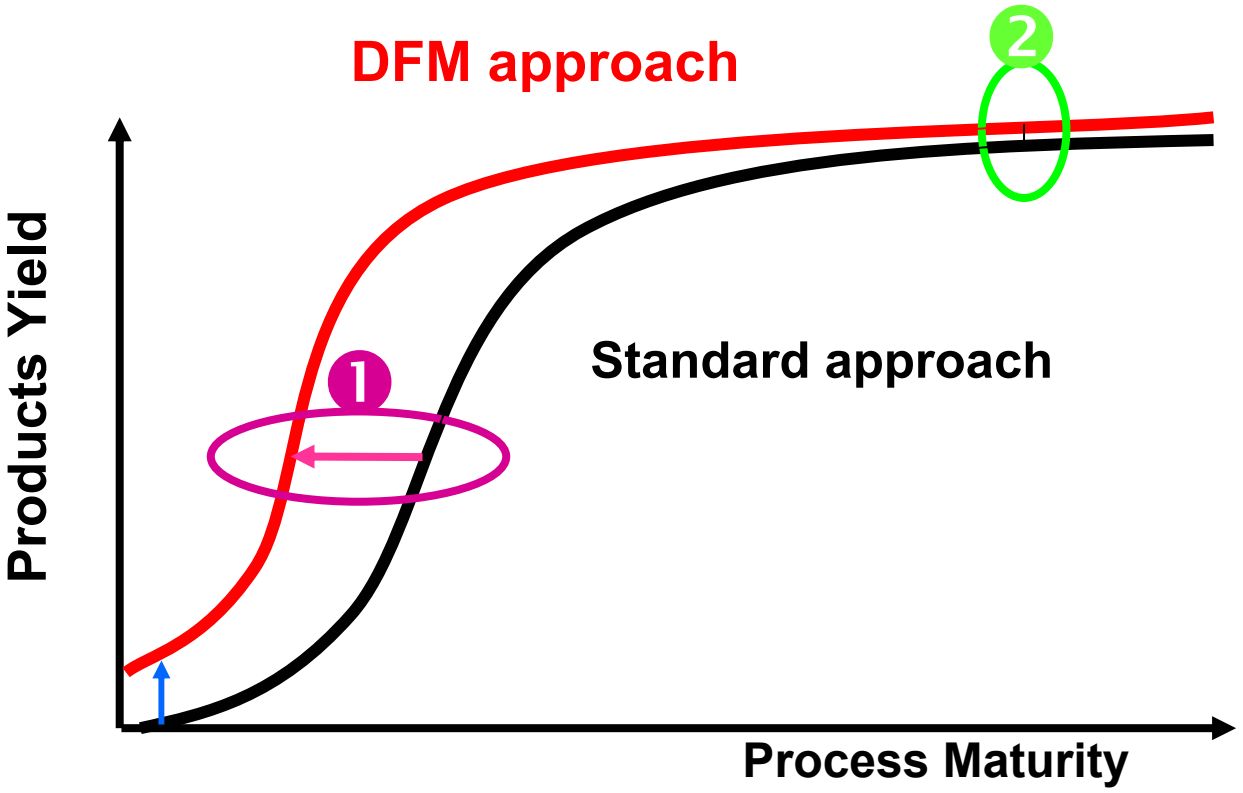


BLOCK	AREA (mm²)	AREA (%)	# Memory cuts
Analog	2.6	1.5%	-
Std Cells	65.2	38.1%	-
Dual ports 1,75Mb	21.5	12.5%	101
Multiports 2.25Mb	65.5	38.2%	64
Other	16.5	9.7%	-
Total chip	171.3 mm²		

Yield improvement: DFM result



Design For Manufacturability Gains



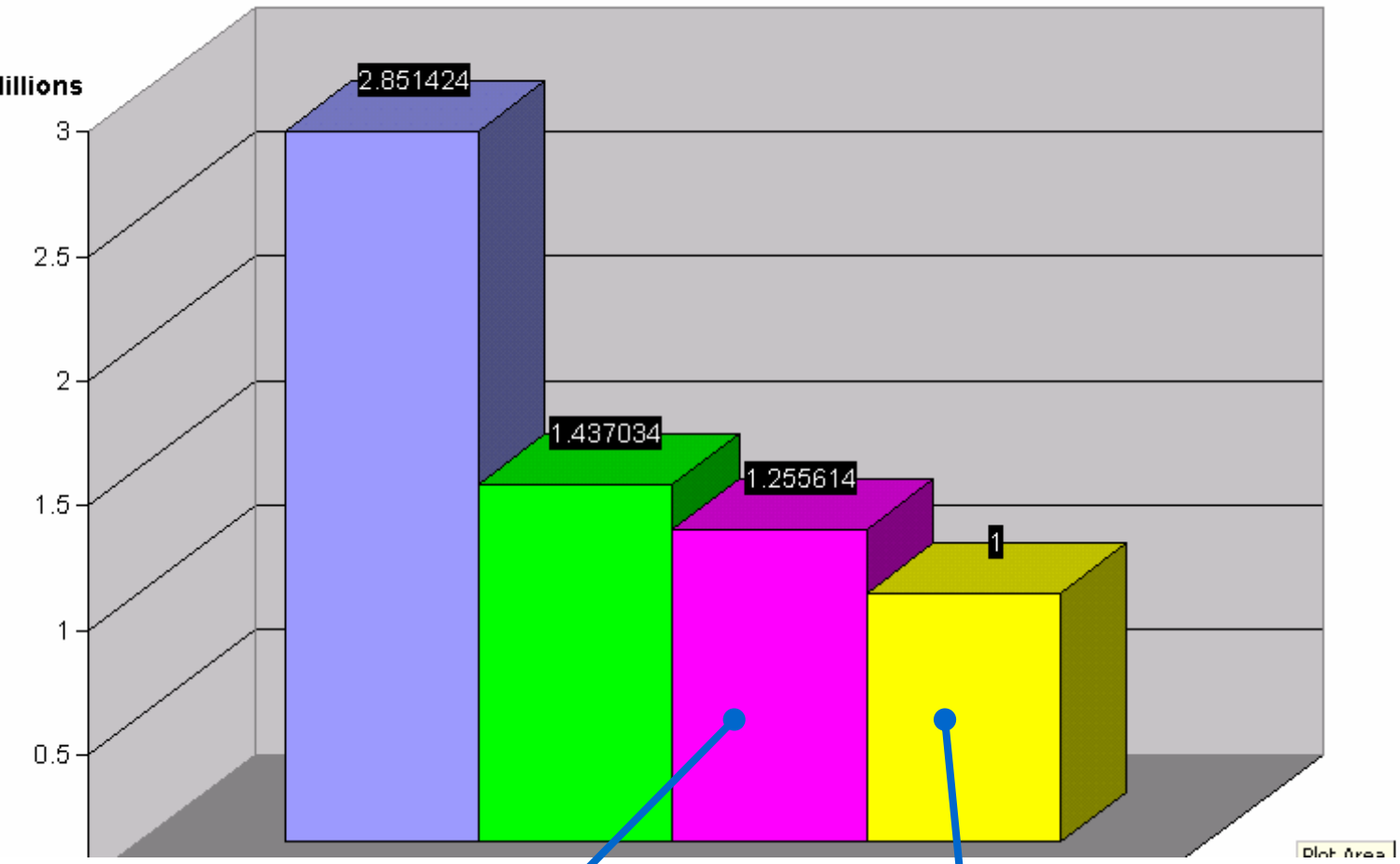
2 Yield gain for **mature** process (3 to 5%)

3 Robustness increase (versus design marginalities)

1 **Acceleration** for **ramp-up** process (~months)

4 Reliability improvement

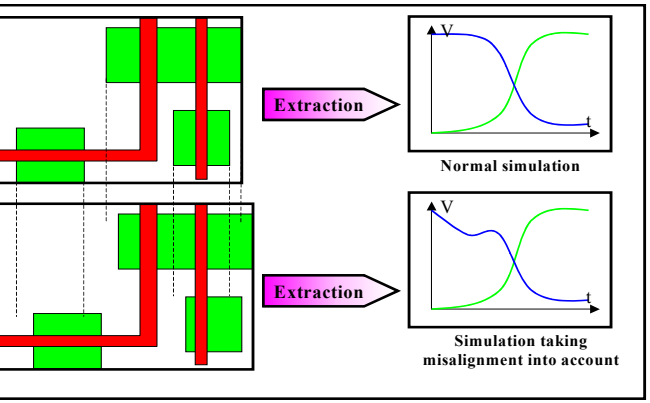
Potential for via redundancy



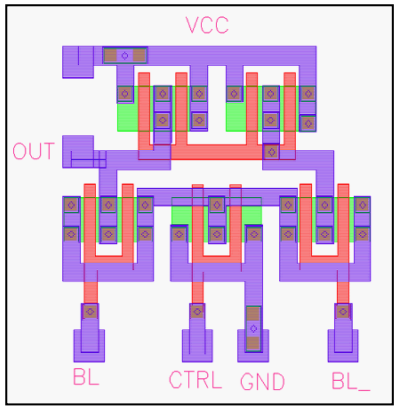
among 1.2 million vias, 1 million are redundable without area consumption

Design For Manufacturability

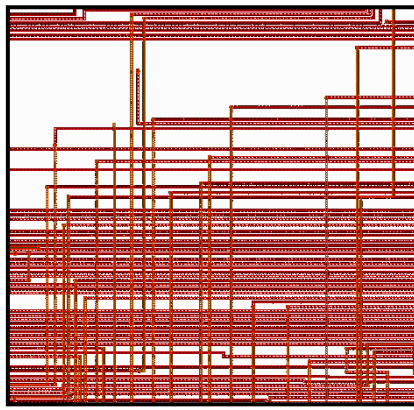
lisalignment impact



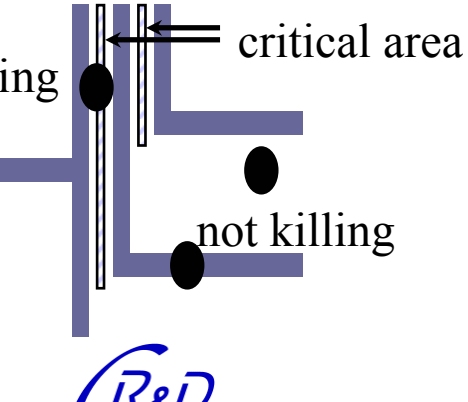
Matching robustness

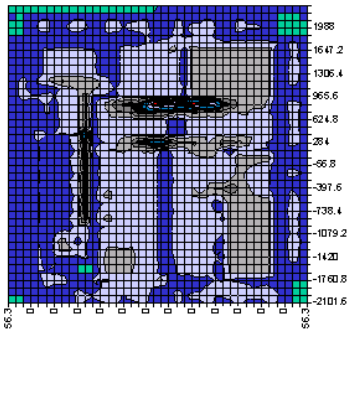


Wire spreading

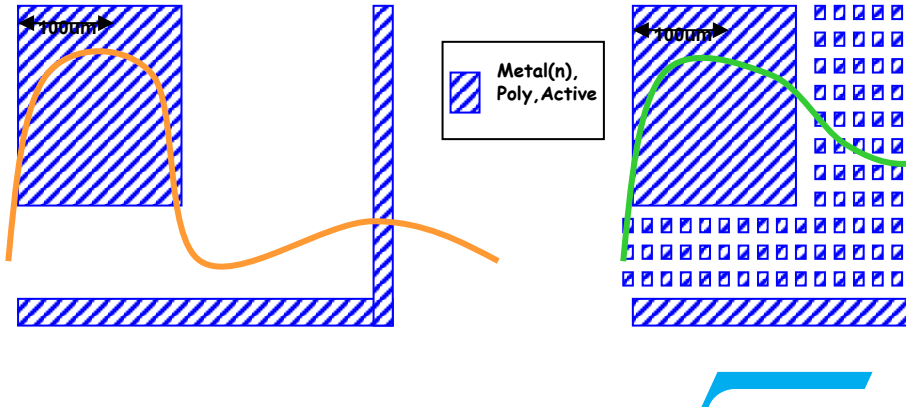


Critical area computation

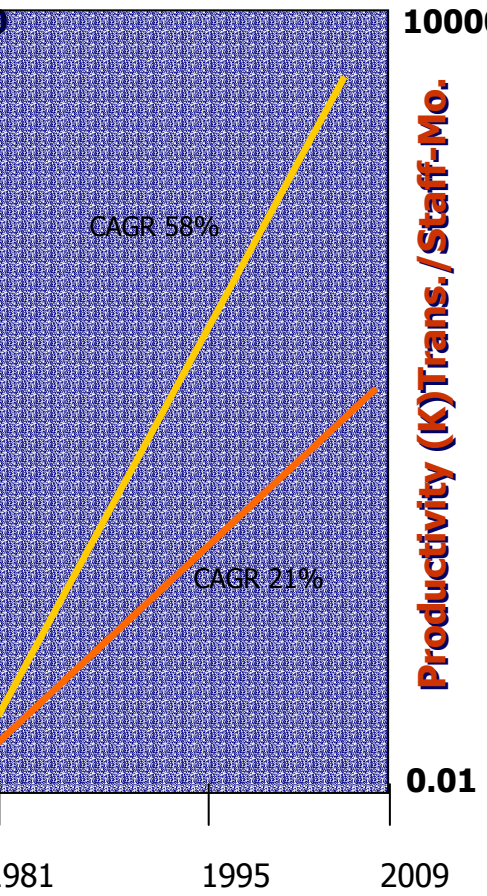




Tiling – densities for CMP



The Design Productivity Gap



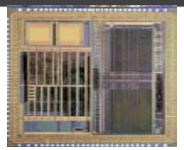
		0.25 µm	0.18 µm	0.12
Number of elements	Standard cells	600	950	145
	IOs	500	1100	150
	Transistor variants	1	2	6

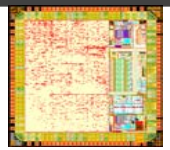
Variety and performance	eSRAM: low-power, low-leakage, high-speed, new a Embedded DRAM & Flash High speed IOs: USB2, LVDS, UDMA, PCI, Gbit link, Analog cells: ADCs, DACs of various # bits, power,

RTL-to-Layout

Low Power

Cell Libraries

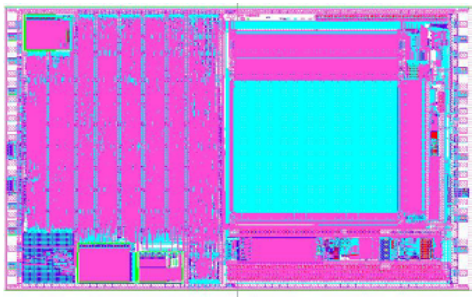




SoC's with CMOS-Imager process

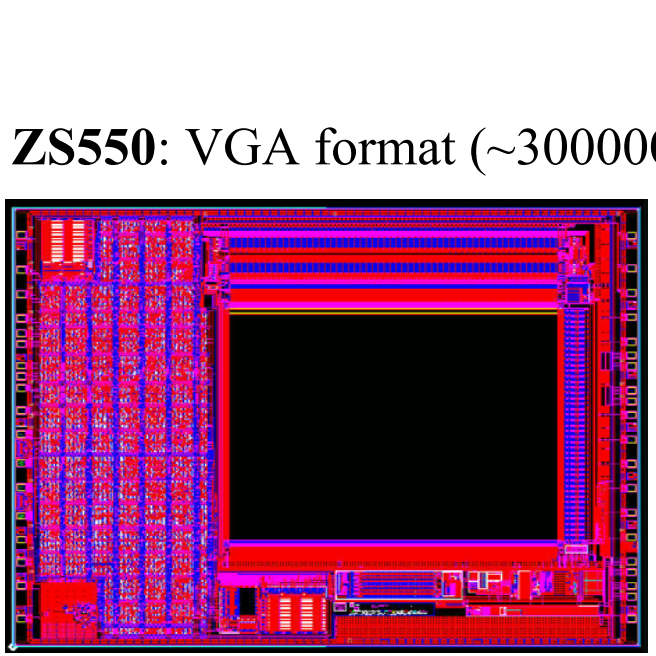
or mobile phone applications:

✓ **ZS450**: CIF format (~100000 pixels)



Area
24.0 mm²

✓ **ZS550**: VGA format (~300000 pixels)

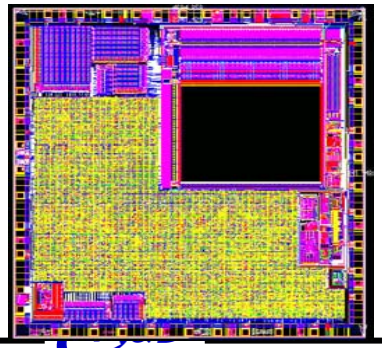


Are
39.6 m

or webcam applications:

✓ **ZS422**: QVGA format (~75000 pixels)

=> audio/video/video processing (SOC)

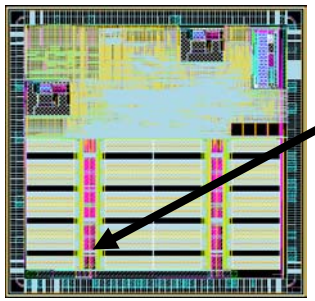


Area
24.1 mm²

Production 0.18um SoC's with eDRAM

Low-End Printer

(20mm²)

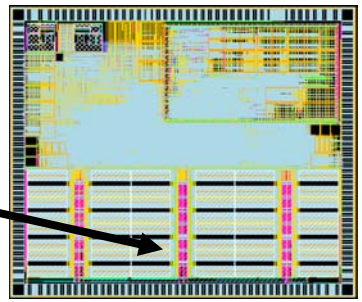


4 Mbits eDRAM

Includes ARM micro

High-End Printer

(34 mm²)



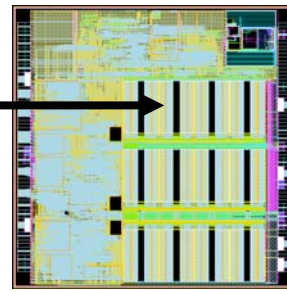
6 Mbits eDRAM

Includes ARM micro

Camera for cell phone

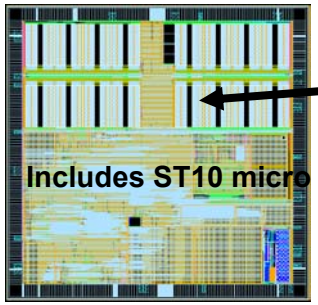
(15 mm²)

3 Mbits eDRAM



Disk Controller

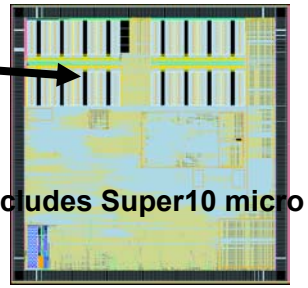
(26 mm²)



4 Mbits eDRAM

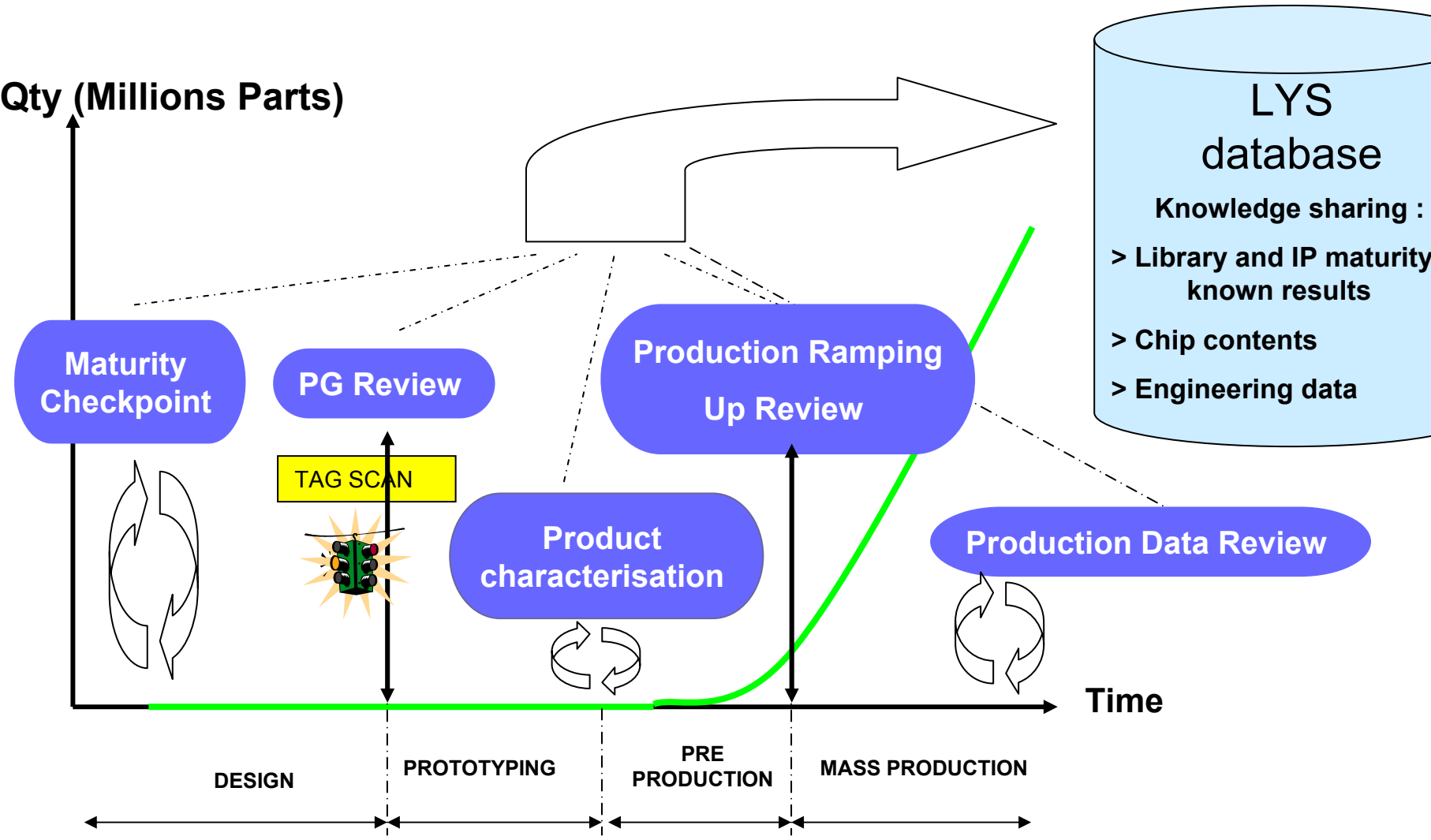
DVD recorder

(34 mm²)

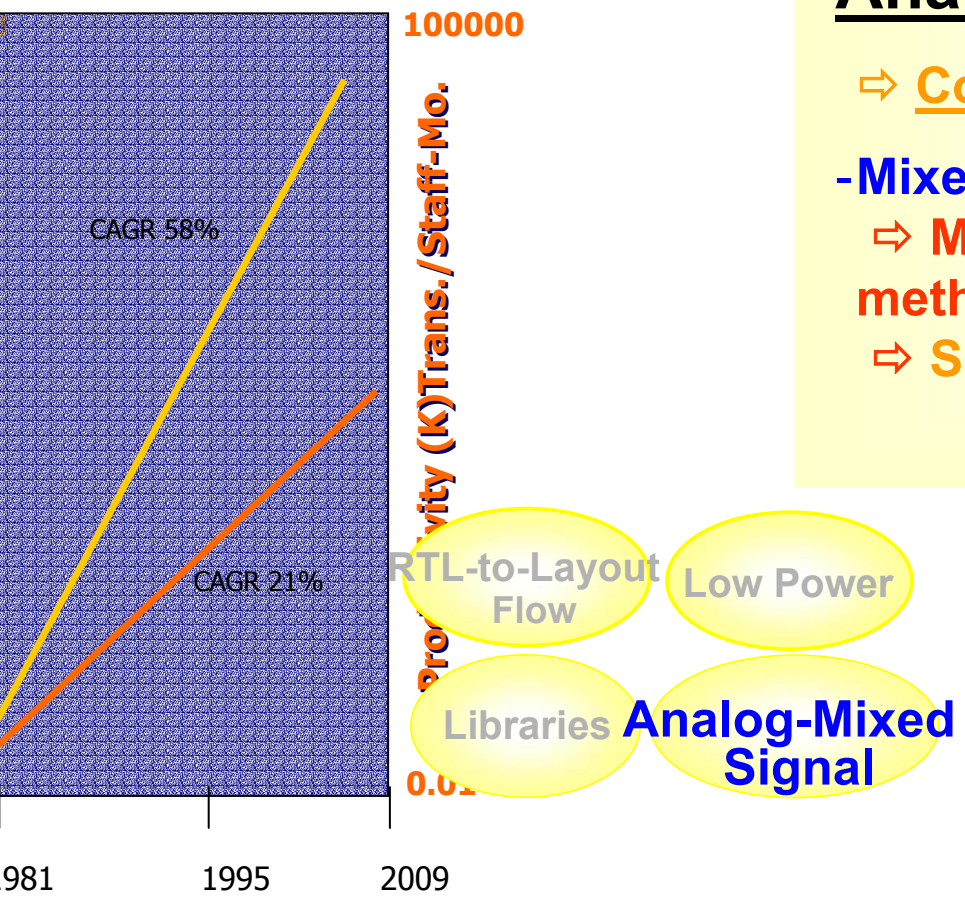


Library Yield System (LYS)

From 1st Design to High Volume Product Manufacturing



The Design Productivity Gap



Analog Designers shortage !!!

⇨ Commodity analog IP, Process Portin

-Mixed RF/Analog & Digital co-design

⇨ Missing full SoC co-verification methodology/tools incl Back-annotation

⇨ SoC Substrate-noise analysis

Analog Cell Design Productivity Improvements

OP AMP.
PLL
ADC
DAC

"Commodity" IP Generation
Low Freq.
Medium perf.

- Trans. Sizing Synthesis
- Fully automatic Layout

LNA
OP AMP.
PLL
ADC
DAC
SYNTH.

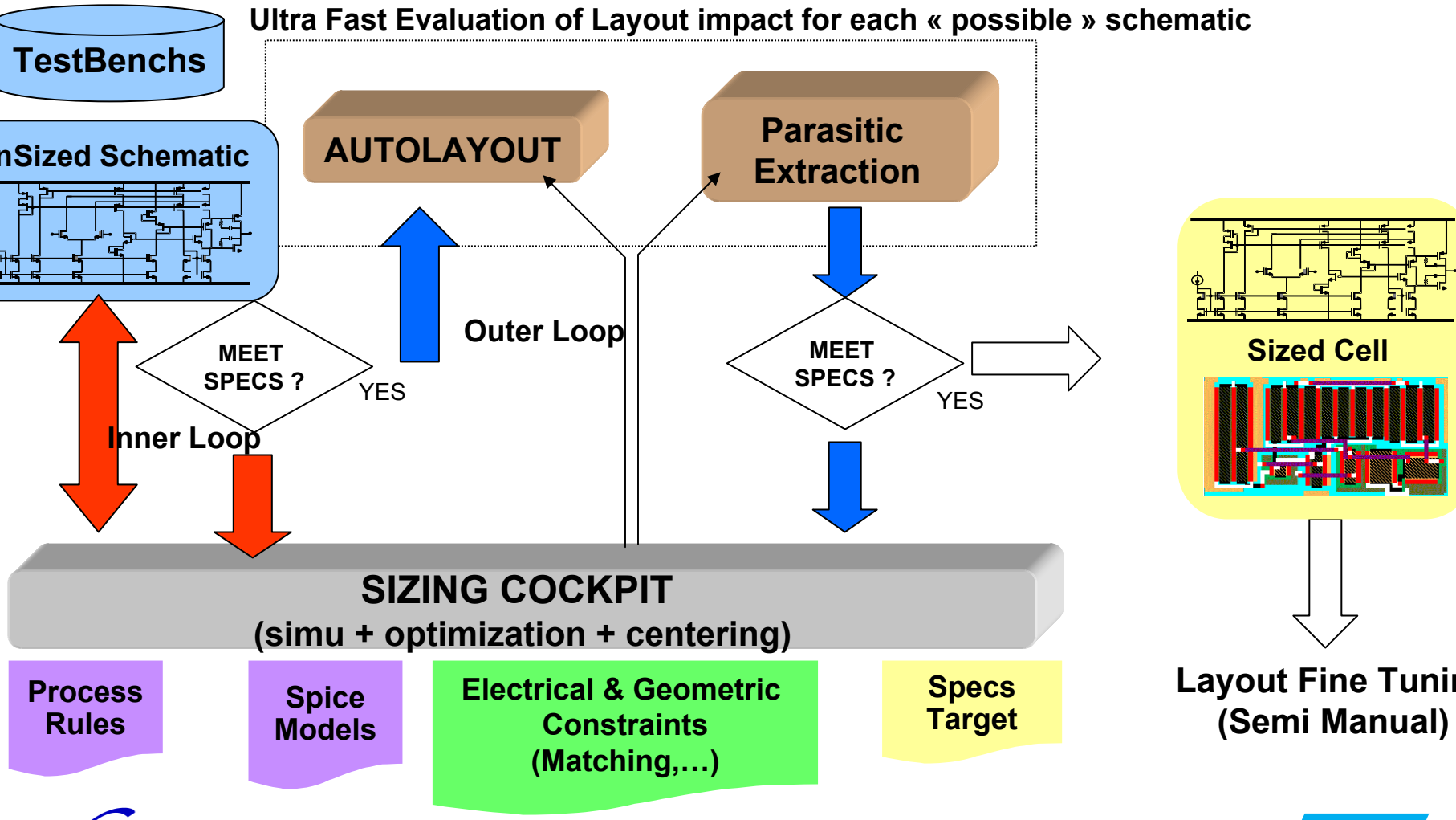
« Star » IP Design Assistance
High performance

- Sizing Flow
- Robustized Design
- Cell Characterization
- Behavioral model annotation
- Constraint-driven Layout

Support for IP Process Migration

- Auto Re-Sizing
- Auto Re-Layout

Cell Development « Future Flow »

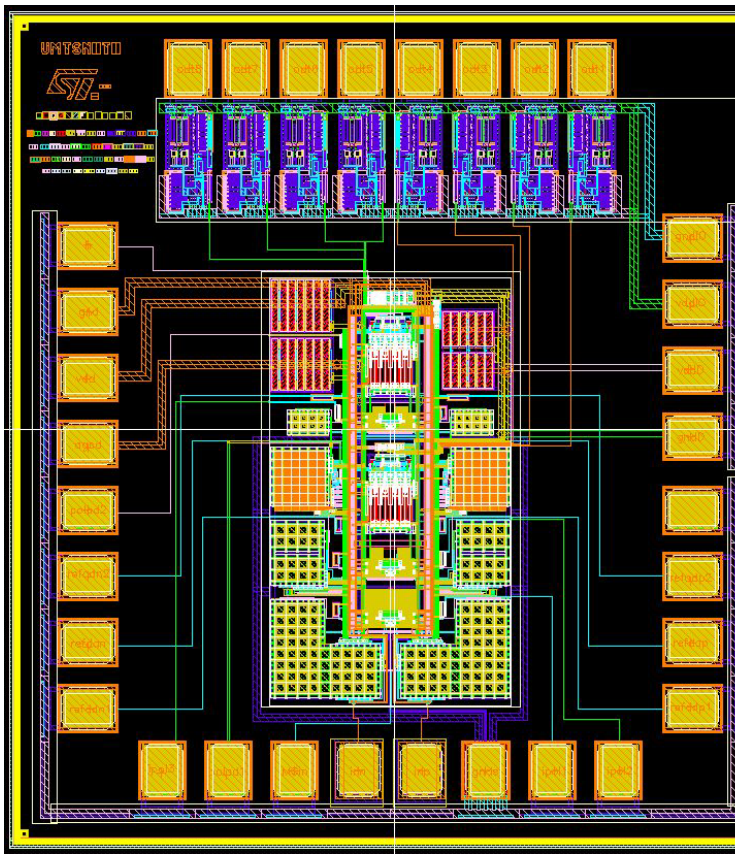


0.13um CMOS Dual-mode ΣΔ Modulator

Presented at ISSCC'2003

Features

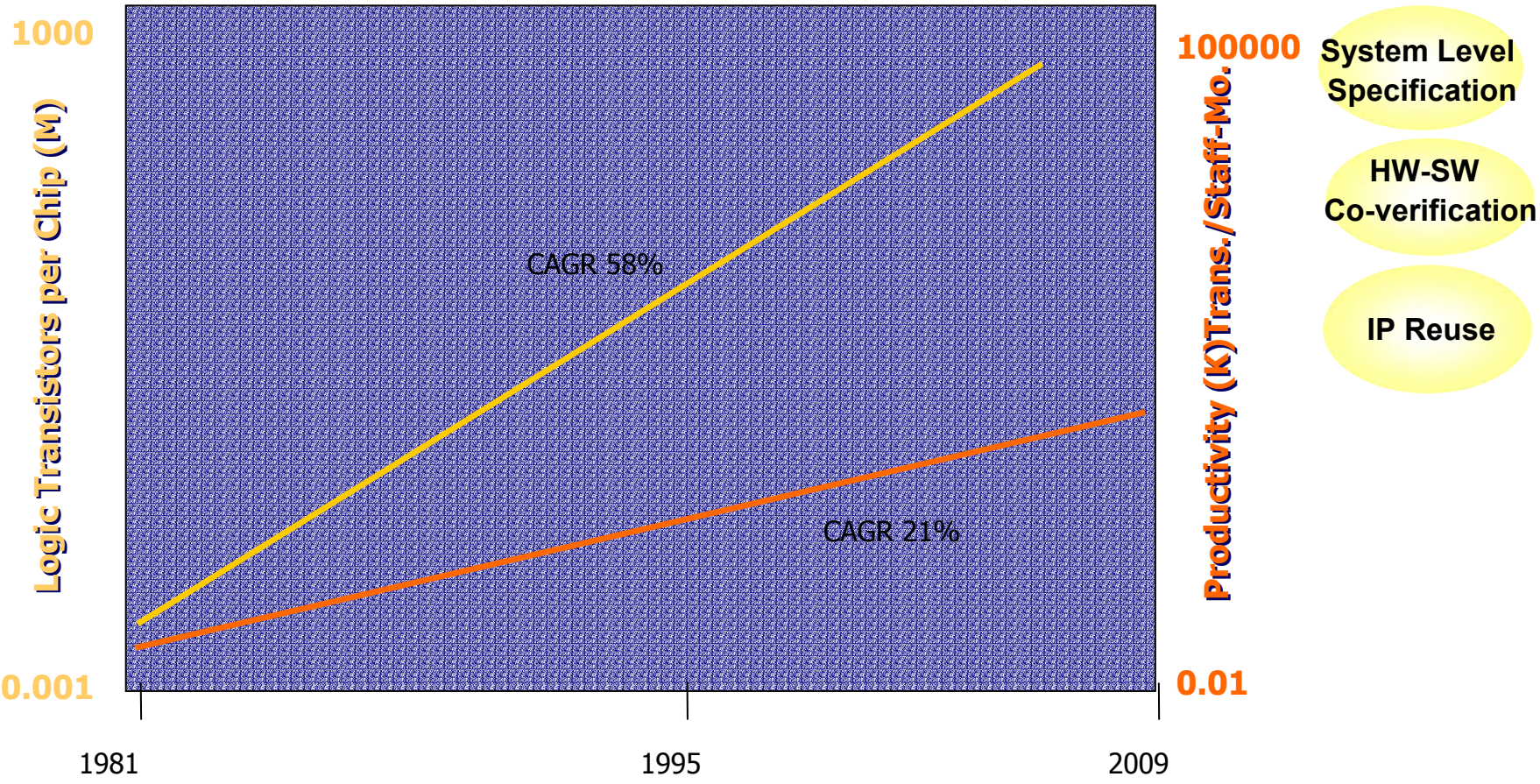
Application:	GPRS / W-CDMA
Resolution (ENOB):	13 bits / 10 bits
SNDR:	81dB / 64 dB
BW :	100kHz / 1.92 MHz
Fs :	39 MHz / 38.4 MHz
Consumption (1.2V) :	2.1mW / 2.9 mW
Core surface :	0.2mm^2
Architecture :	2nd-order / MASH2-1
Process:	CMOS 0.13µm



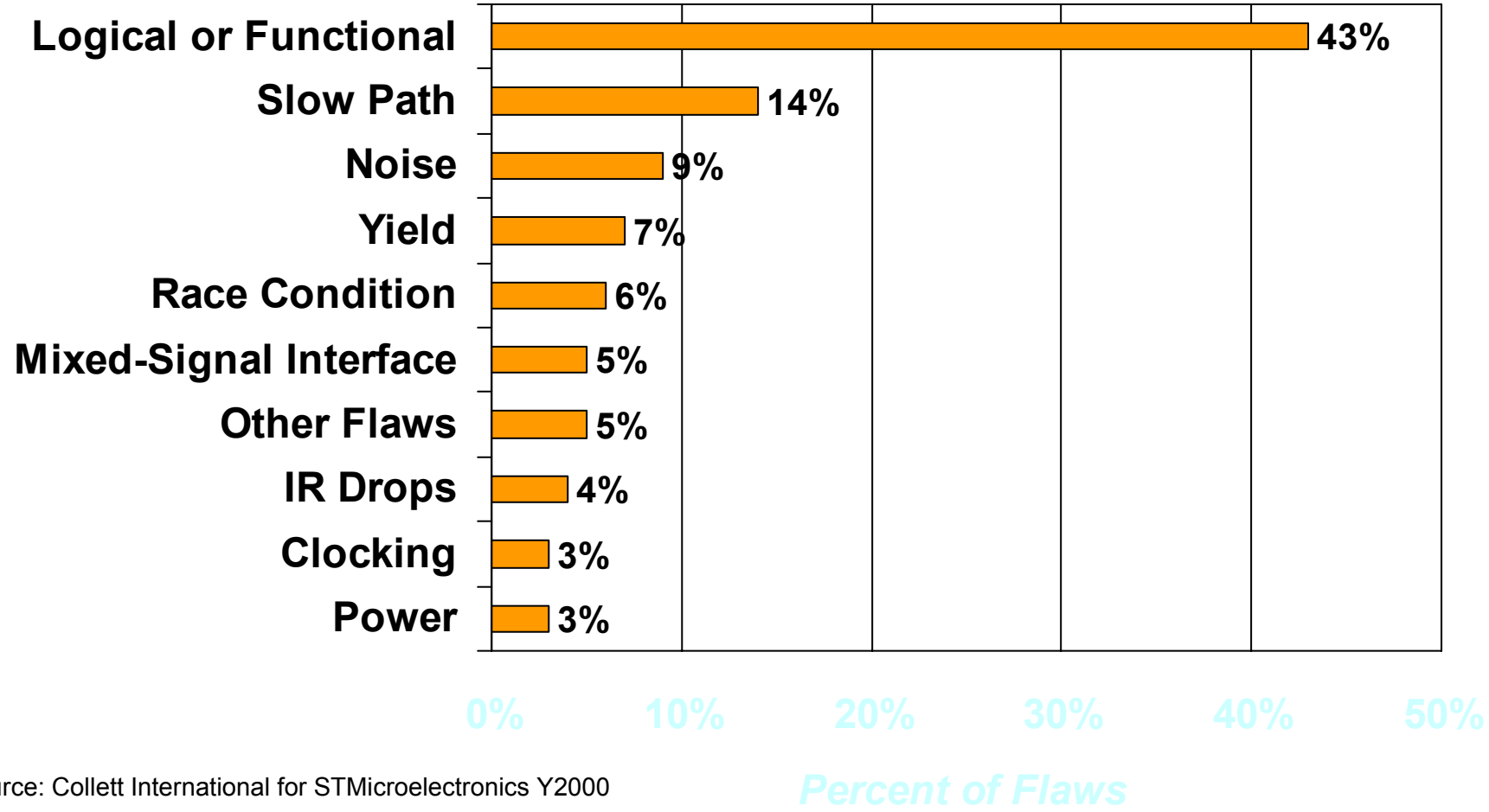
Agenda

- SoC trends and links with process/design
- RTL-to-Layout and cell Libraries trends
- **System-level, IP reuse and HW-SW codesign**
- Off-roadmap activities
- Support/partnerships with ST product divisions

Closing the Design Productivity Gap



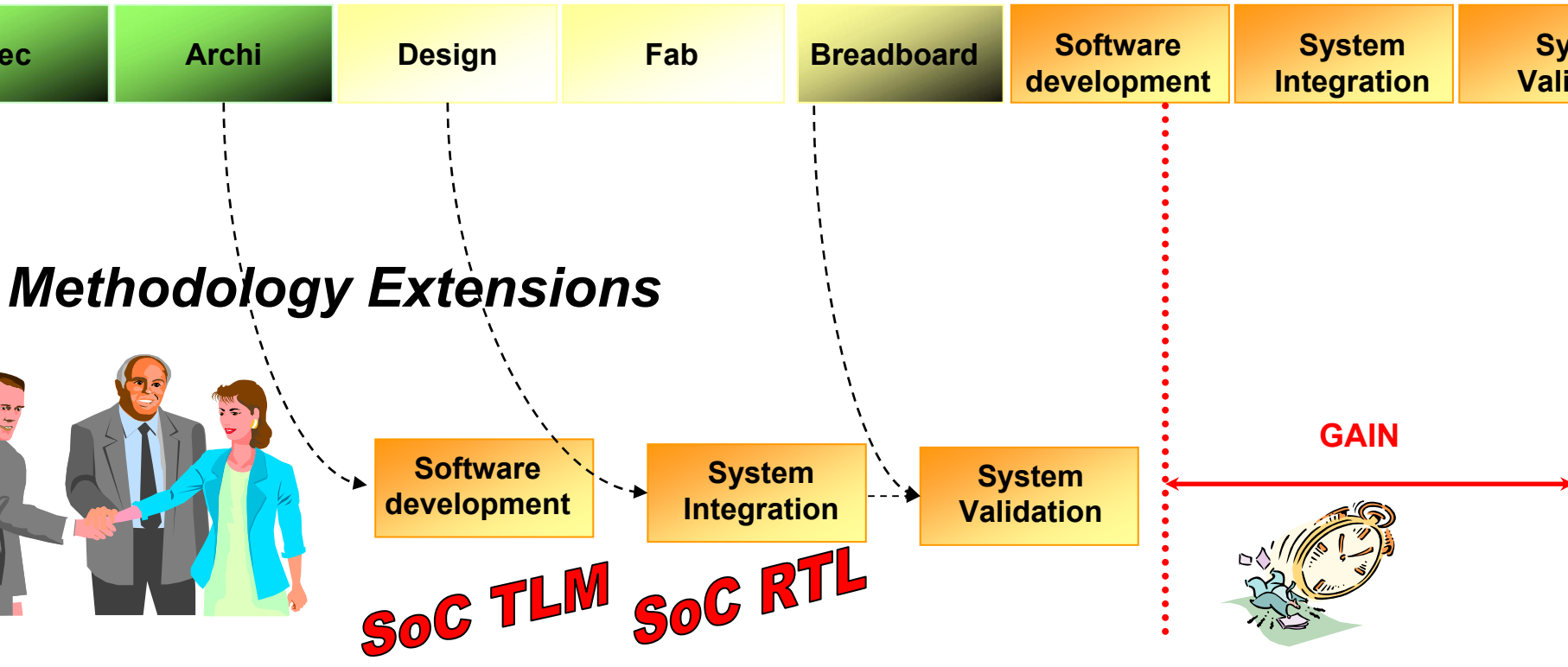
Percent of Total Flaws Fixed in IC/ASIC Designs Having Two or More Silicon Spins



Source: Collett International for STMicroelectronics Y2000

Concurrent Hardware/Software Design

Standard Flow

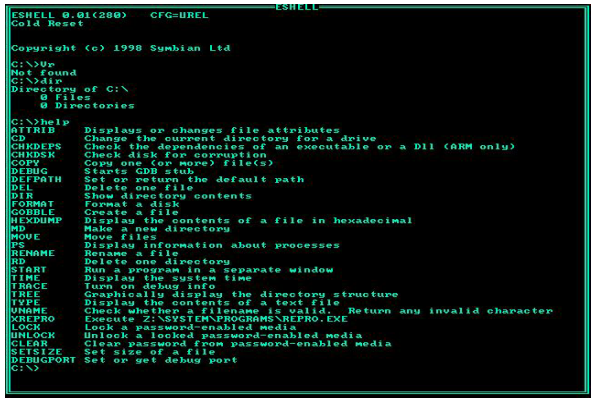


Methodology Extensions

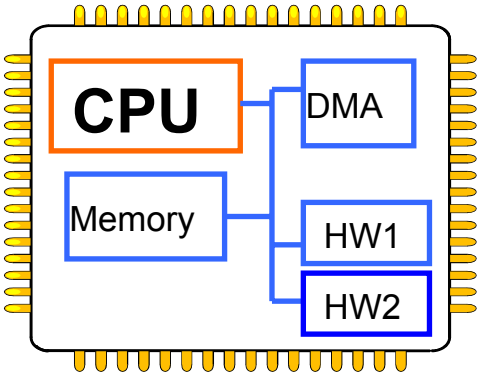
Operating-System is booting on simulated Cellphone (RTL)

- ***Software***
  Real RTOS

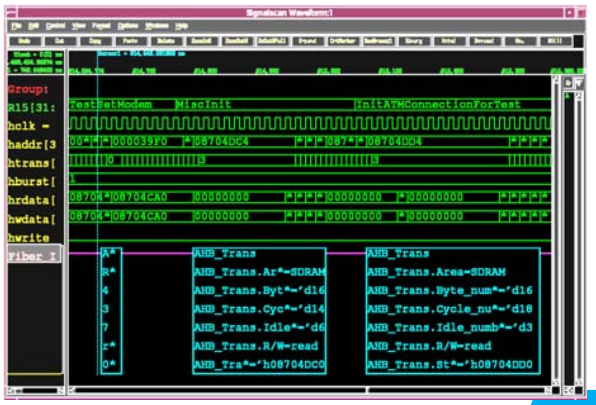
  (Symbian)



Processor
ISS simu



Peripherals
RTL simulation



HW-SW Co-simulation

Cycle-Accurate

200 instr / sec

TLM models - Fast SoC simulations

Real embedded Software

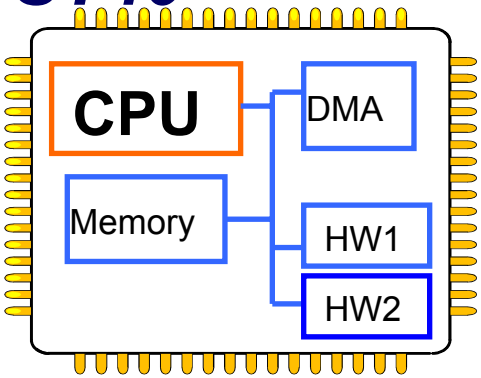
Application & Functional Verification

ST100 | SuperH | ST20 | ARM

ST40

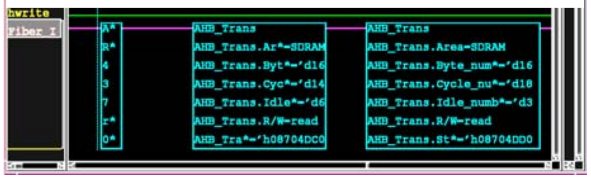
Processor

ISS simu



Peripherals

TLM simu



Standardization being proposed to SystemC OSCI by ST, Cadence, ARM

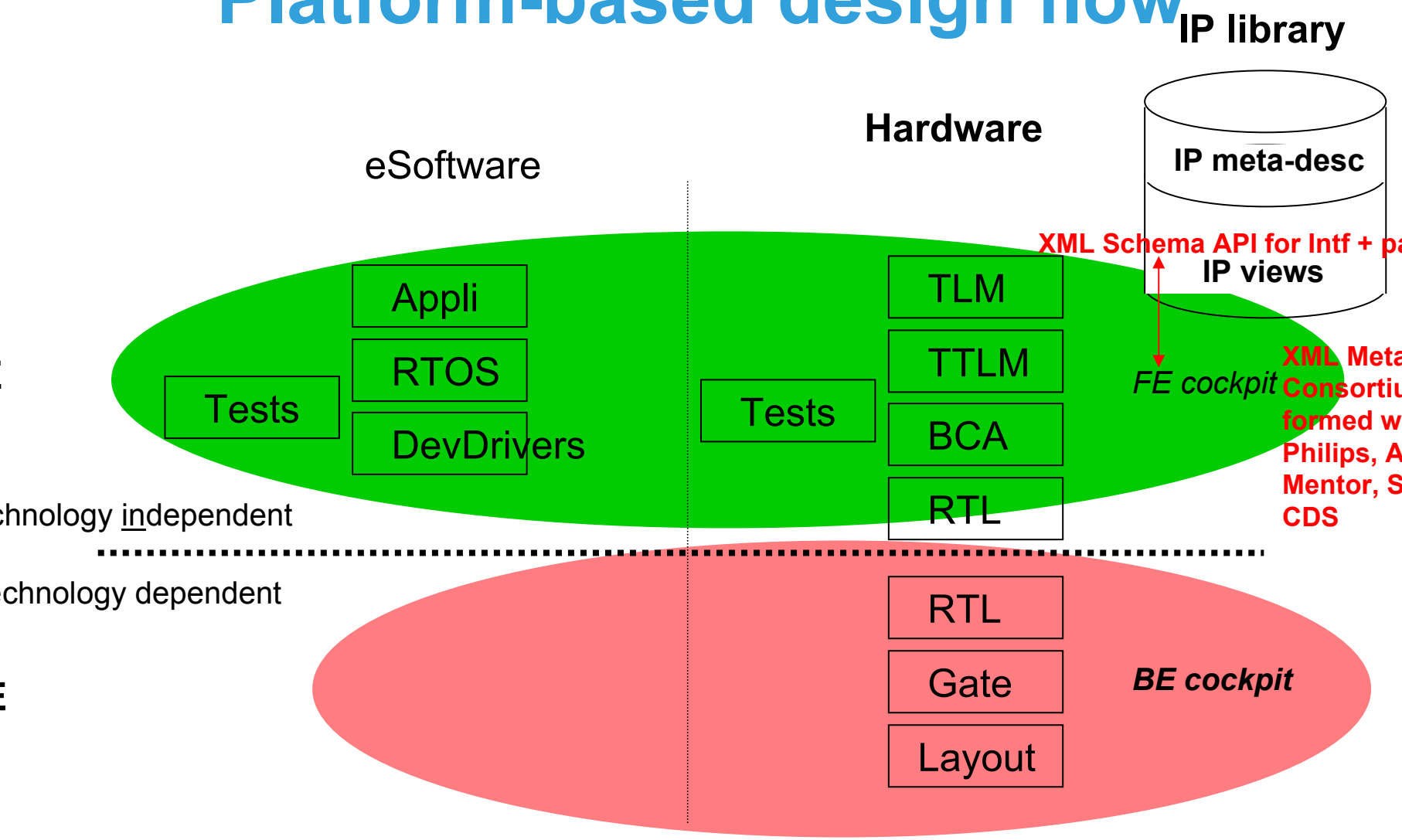
HW-SW Co-simulation

Transaction-Accurate

200 K+ instr / sec

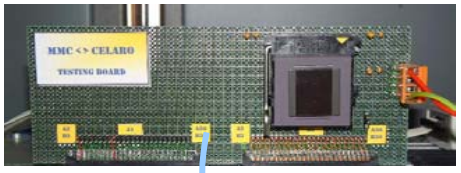
R&D

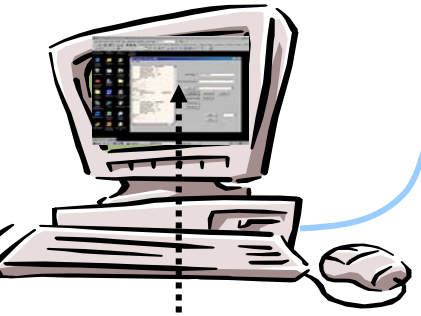
Platform-based design flow

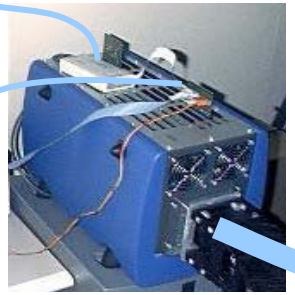


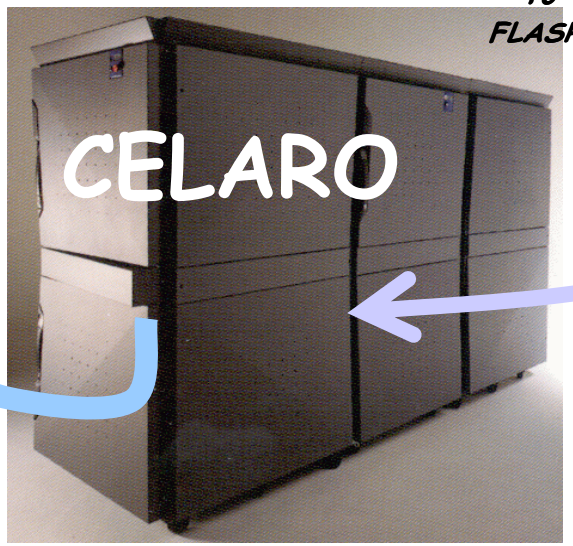
HW Emulation for MMC

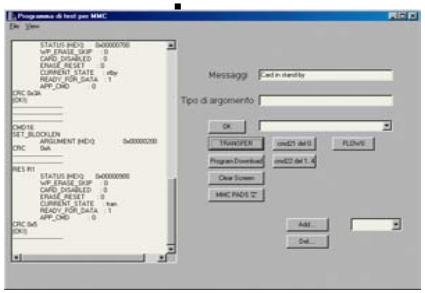
- Real M58LW128 FLASH chip in-circuit



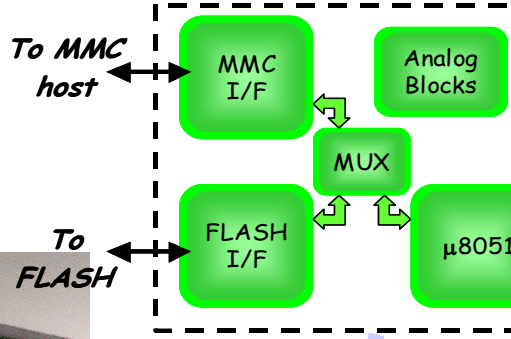








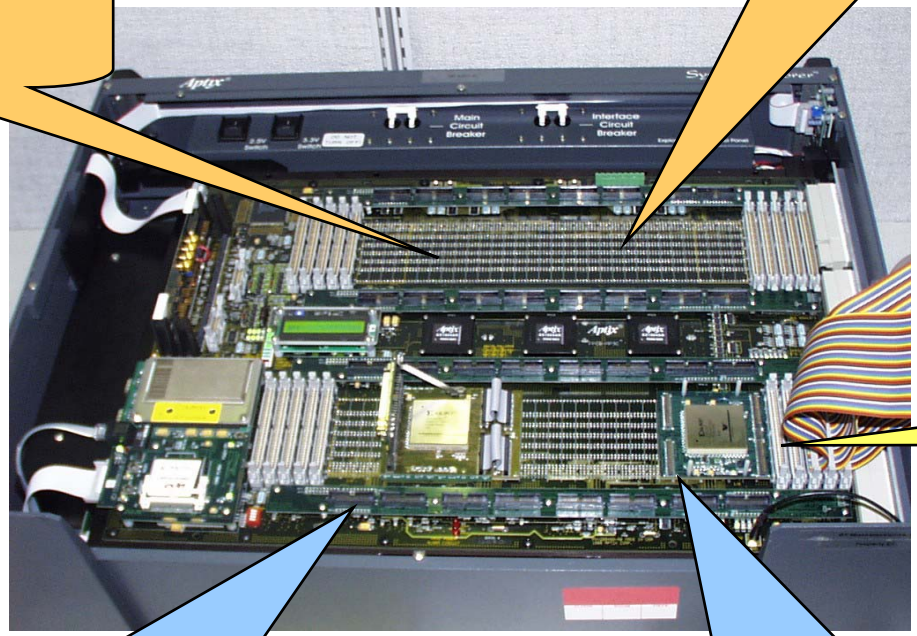
RTL Design



- 1w setup-time
- ~0.5MHz

- SW host running @100KHz
- Connection of HW host ongoing

First Prototype Platform: Aptix



HW/SW fast prototype platform

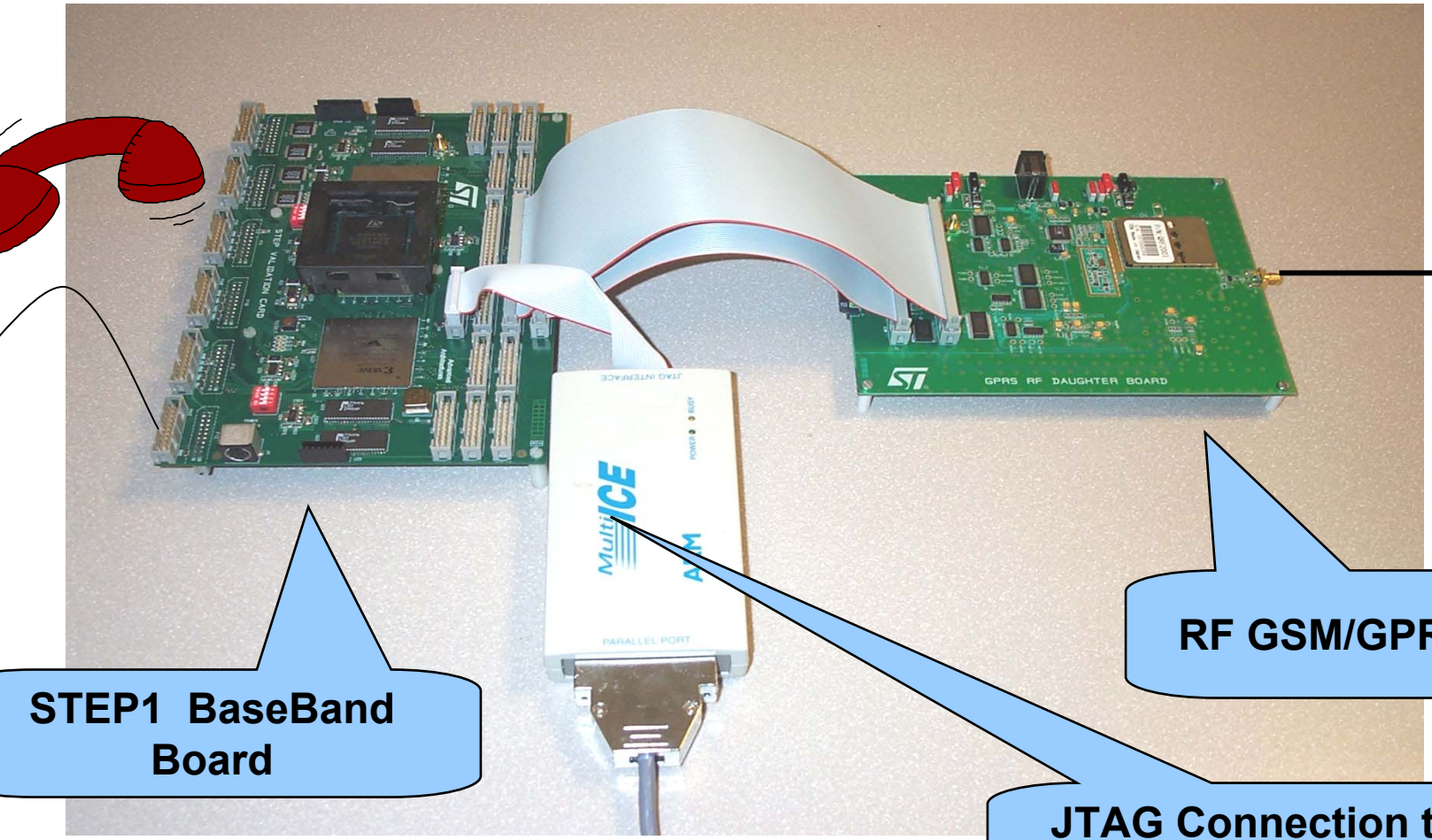
Faithful representation of the final design

Available much sooner than the final silicon

Guaranties the real-time behavior

Validation of the fundamentals of the SoC HW/SW architecture

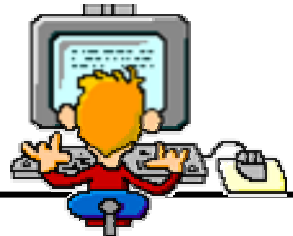
FPGA-based Prototyping Environment



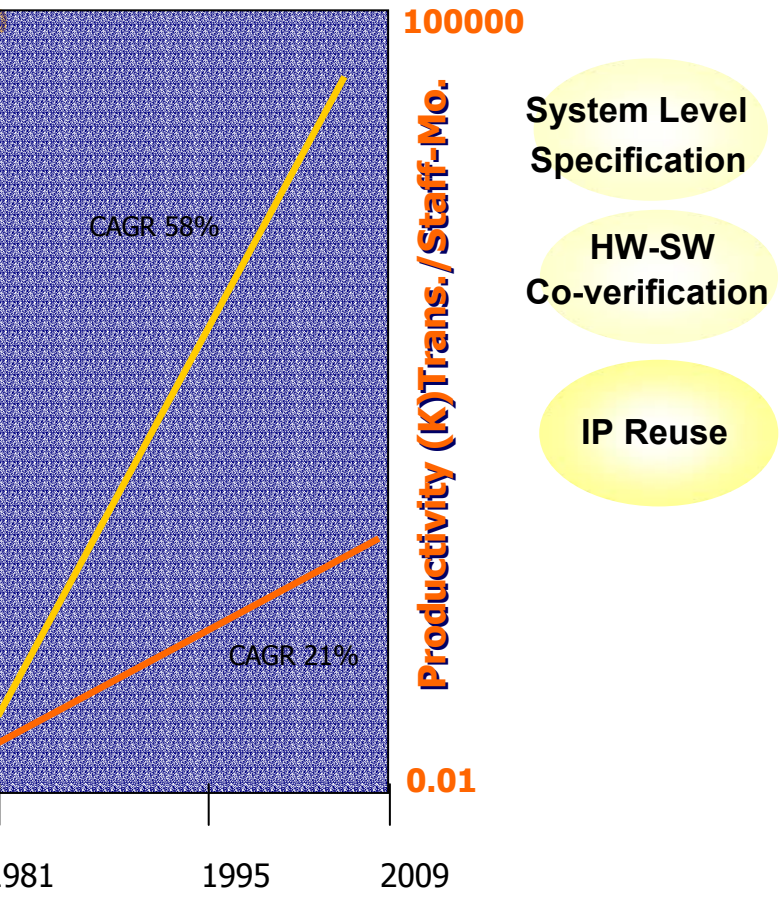
STEP1 BaseBand Board

RF GSM/GPRS Board

JTAG Connection to SW Debuggers

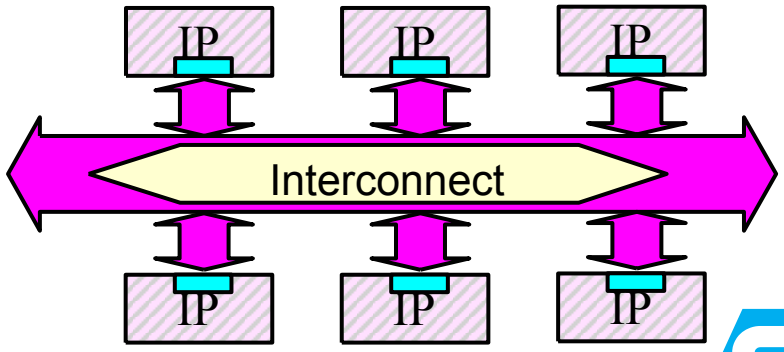


The Design Productivity Gap

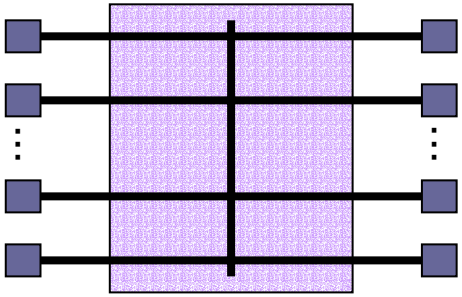


IP Reuse:

- ST Blue Book is now widely accepted ST design groups
- Need to establish a universal IP qualit standard and apply it!
  -> In ST, IPScreen 2.0/3.0
- Plug & Play concept requires that all I blocks adhere to same On-Chip-Bus protocol. (interface)
- -> STBUS, AMBA, other ?



Network-On-Chip (NOC) Overview

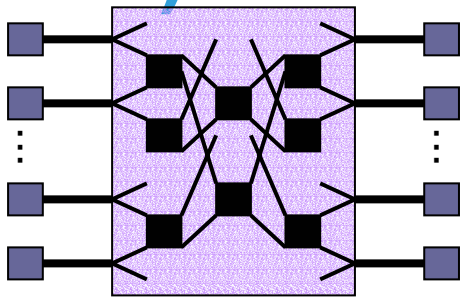


BUS-like

Low latency

Blocking (large contention)

Not easy to scale, need hierarchy



Tree-like

Medium latency

Blocking (blind routing)

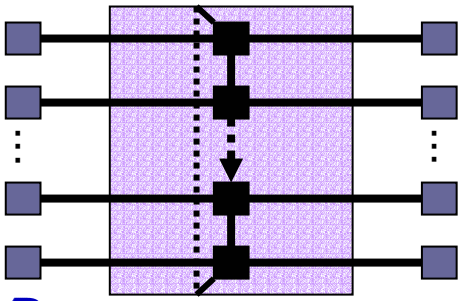
Medium scalability

Ring-like

Large latency

Can be non-blocking

Scalable

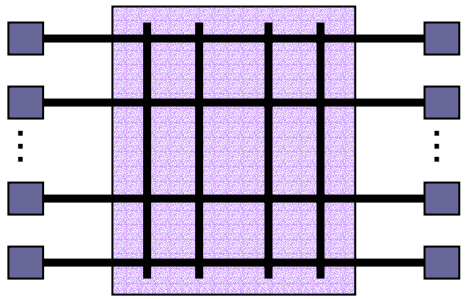


Crossbar-like

Low latency

Non-blocking

Costly, poor scalability



IP Reuse Program

Organization

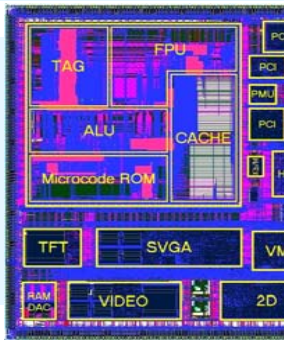
- company program — "Design Methodology & IP Reuse", CEO sponsored
- corporate driven — CR&D + cross-divisional Committee
- domain-specific Work Groups — RTL2Layout, AMS, SLD, DFT, Functional Verif., Power, …
- intranet information site — CAD On Line portal > K9 IP Reuse Pages

Reuse standards

- adherence to industry approach — VSIA; RMM; Quality
- deliverables / views — BlueBook + Unicad Extension
- IP packaging — bbview (mapping from BB logic views to IP physical files)
- HDL coding style — Design Conventions + HAL associated checking tool
- On Chip Bus — VCI-close STBus; AMBA

Methodology

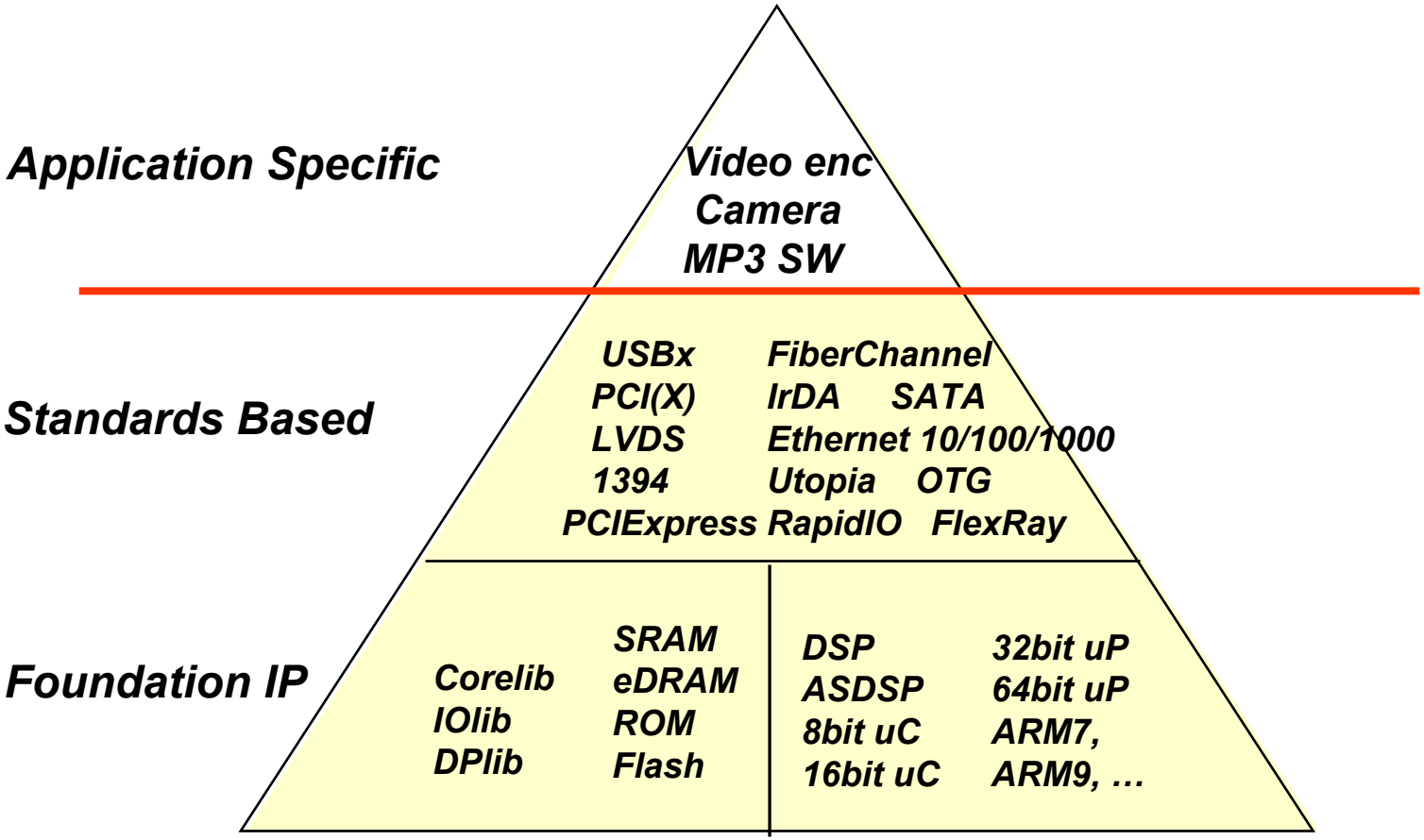
- Development flow — Synopsys based Quartet
- OCB support — STBus, AMBA Platform kits
- System Level — SL model deliverables (TLM, BCA…)
- Verification — dynamic, formal, H/W-S/W, integration



Infrastructure

- Design Data Manag[t]., Bug tracking — Products from Synchronicity, Rational
- IP Quality (IP=Product) — IPScreen Certification; LibYield Maturity tracking
- IP Procurement — IP On Line catalog; Procurement, Exchange procedures

IP categories



IP certification
USB2.0 example

nmary

V functional tests

V functional

igh-Speed sig

ASS
ASS
ASS
ASS

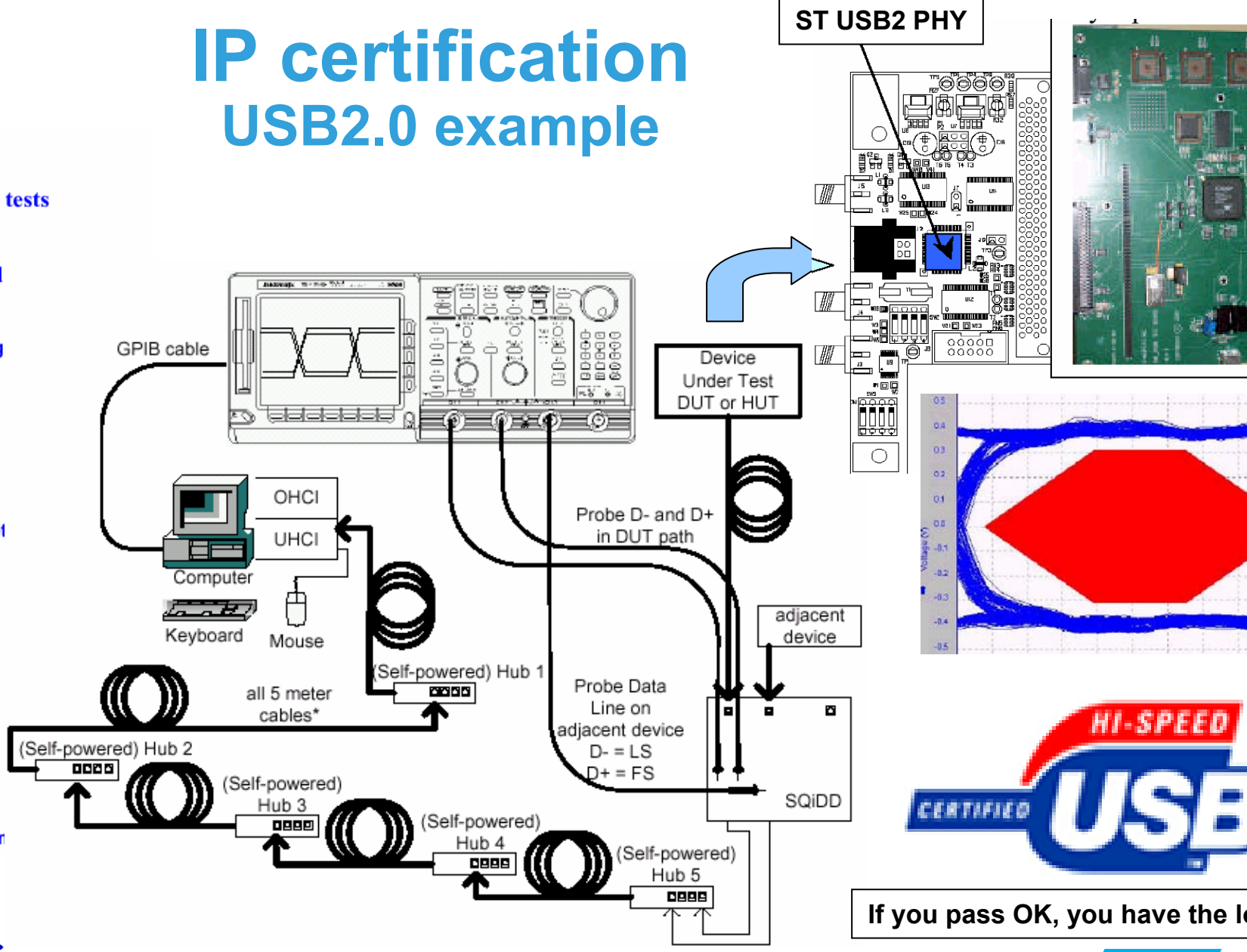
acket Paramet

PASS
PASS
PASS

HIRP Timing

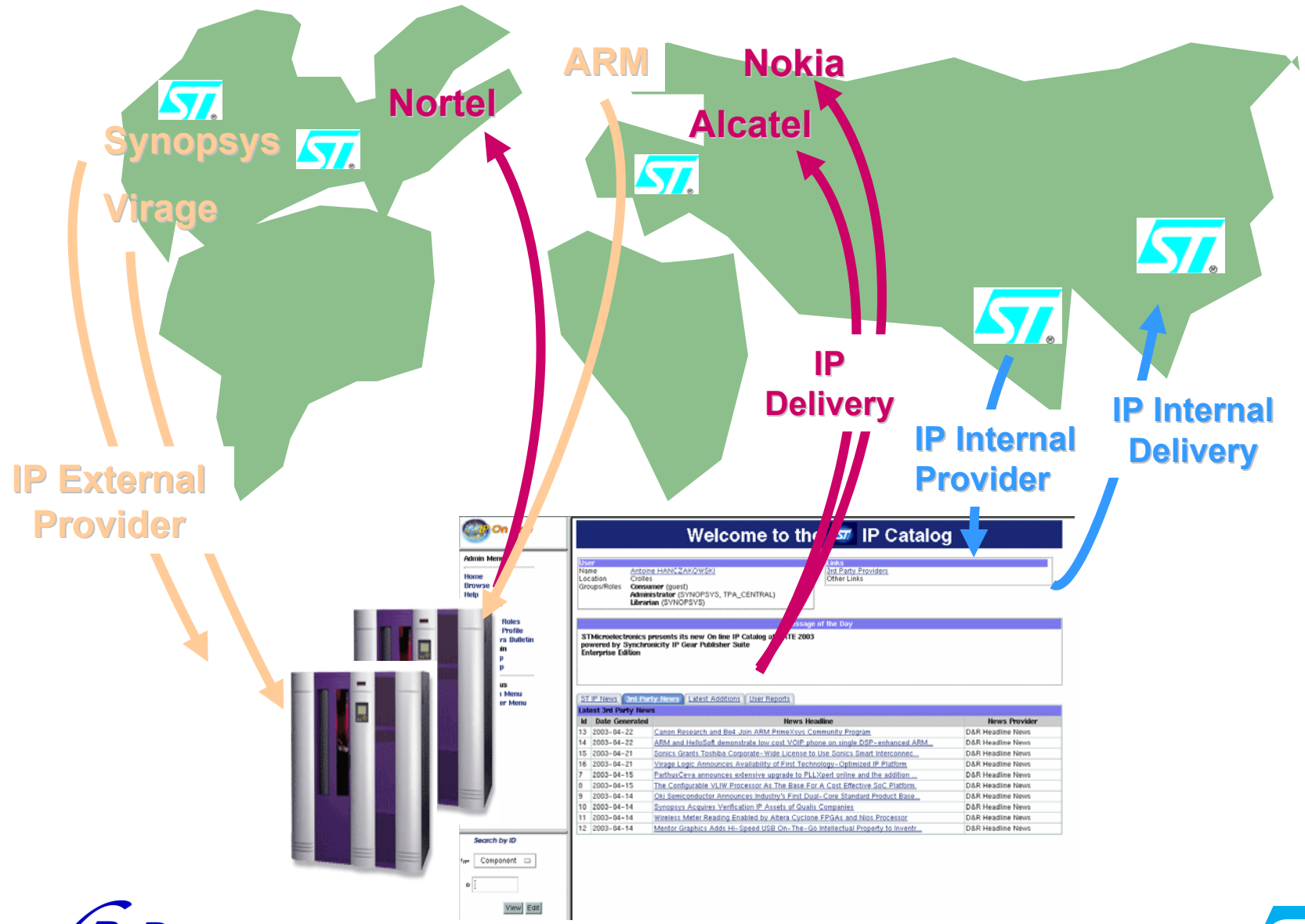
PASS
PASS
PASS

uspend/Resur

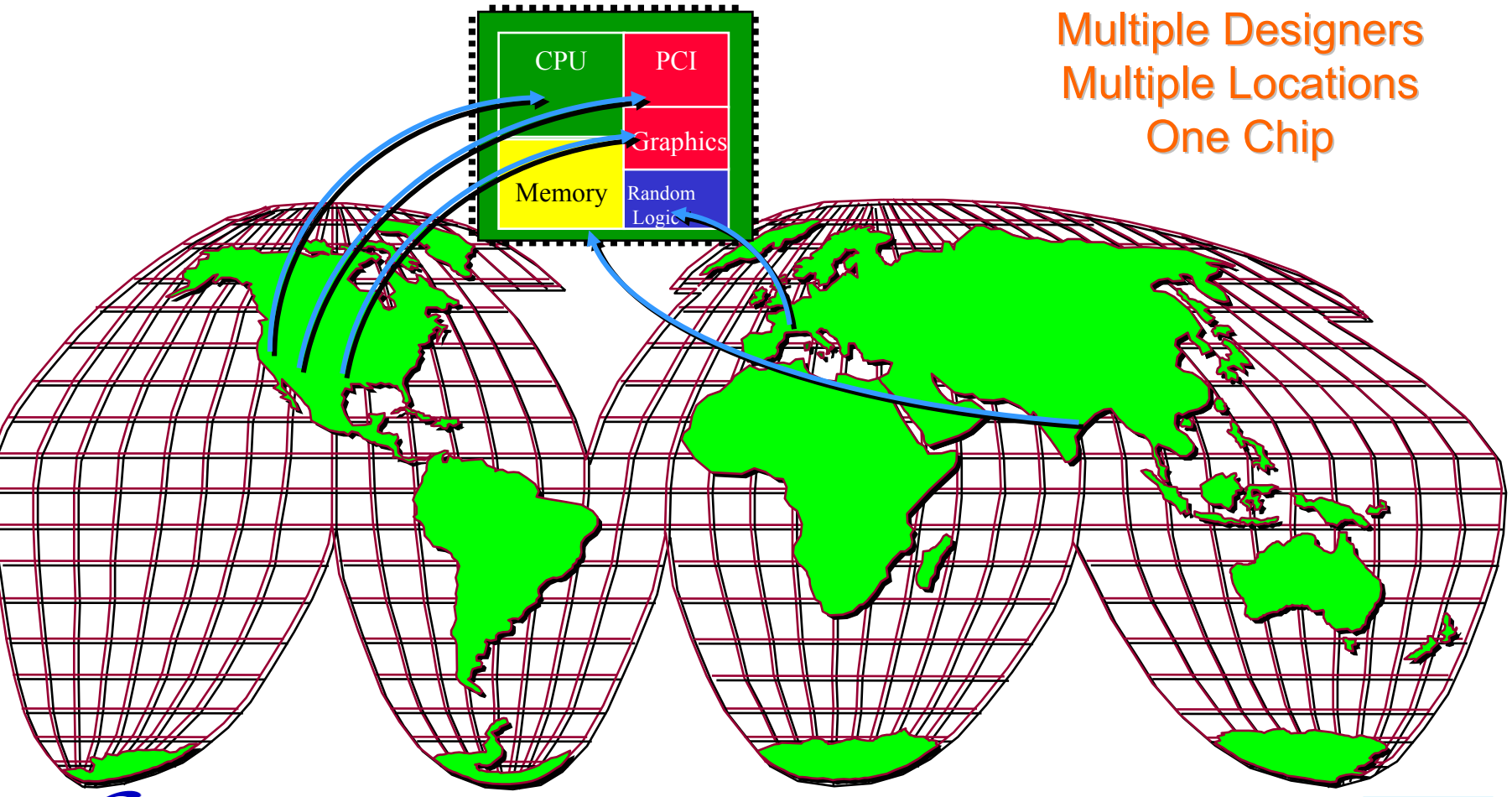


If you pass OK, you have the l

Corporate IP Catalog Project



Multi-Site Collaborative Design (Synchronicity-based)



Agenda

- SoC trends and links with process/design
- RTL-to-Layout and cell Libraries trends
- System-level, IP reuse and HW-SW codesign
- **Off-roadmap activities**
- Conclusions

SOC flexibility and Configurable Logic

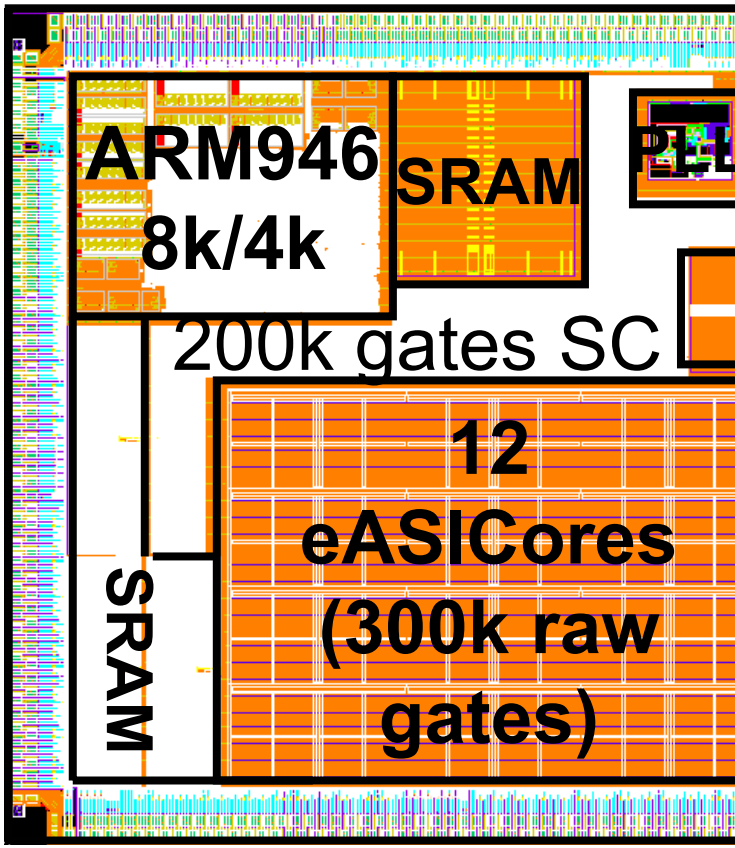
- SOC emerging problems
  - rising cost of masks
  - shorter market windows
  - need to quickly adapt to new customer requirements

→ need of

  - level of programmability
  - flexibility on-chip

- Set of solutions to be provided to our designers
  - Laser-fuses
  - Electrically programmable fuses or anti-fuses
  - Embedded OTP
  - Embedded ROM
  - Embedded SRAM with external ROM/Flash
  - Natural, low-density, embedded Flash in standard CMOS, up to Kbits
  - Embedded FPGAs
  - Embedded mask-programmable sea-of-gates.

Reconfigurable IC with eASIC



0.13um HCMOS9 technology

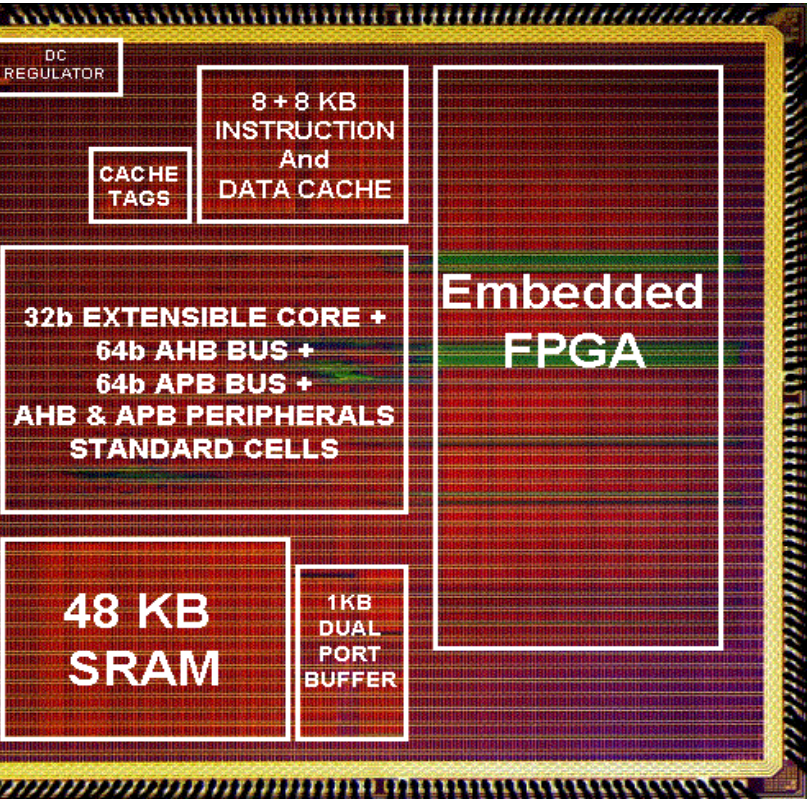
Includes 12 eASICores (300k raw gates)

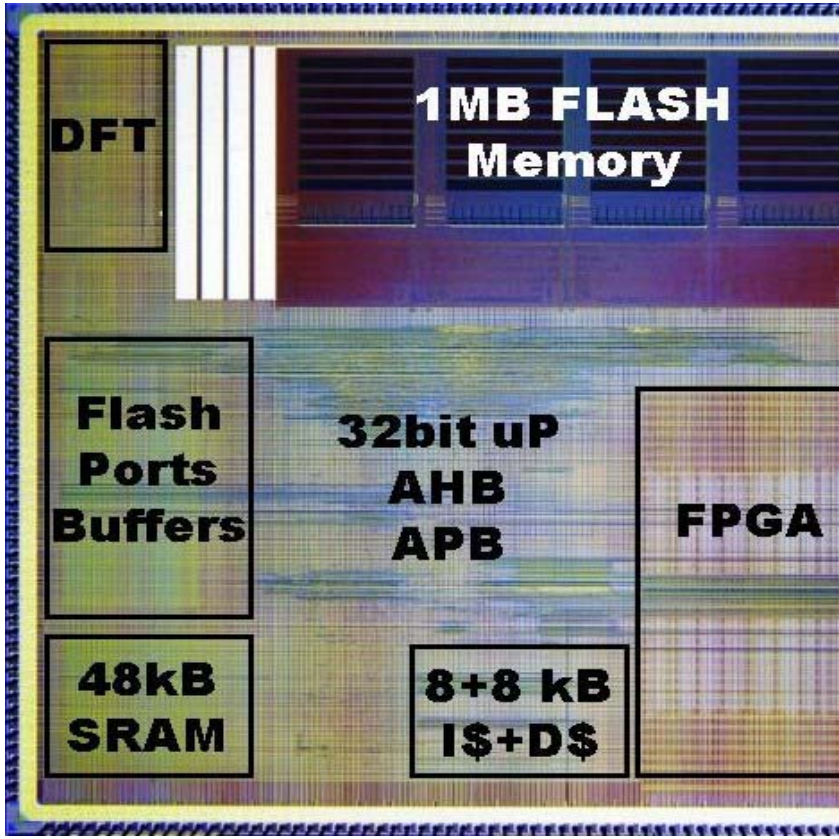
Single-mask configuration

Customization: 110k gates + 28kb DP-RAM

- Area penalty:
- Speed penalty:

eFPGA Reconfigurable SoC's

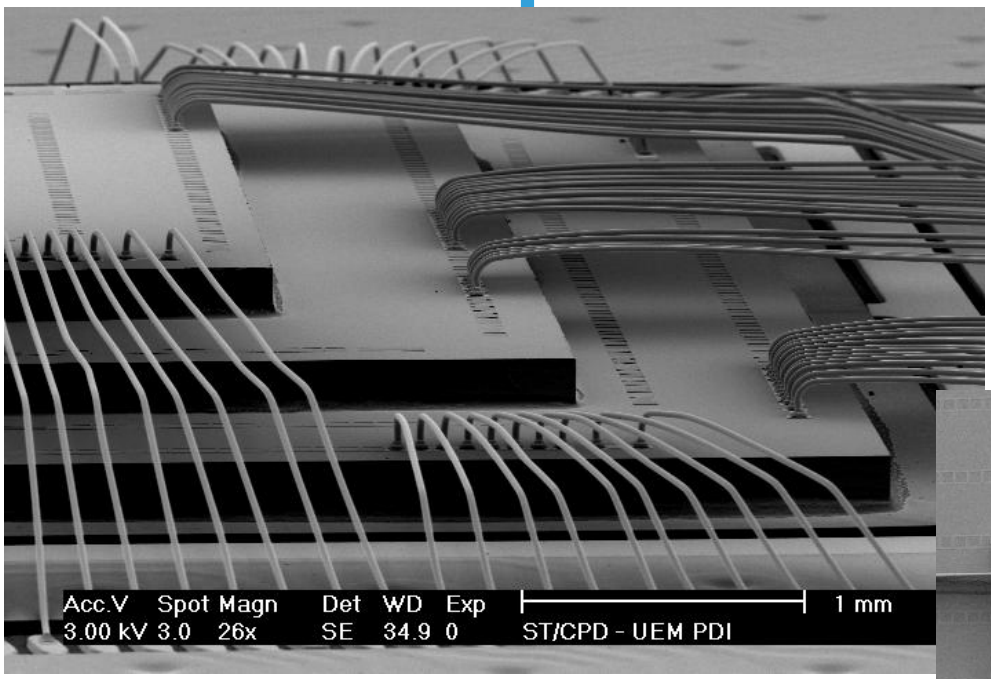




8um Working Silicon
eed: 180 MHz
erage Power @ 50MHz: 140mW
in use in 0.13um

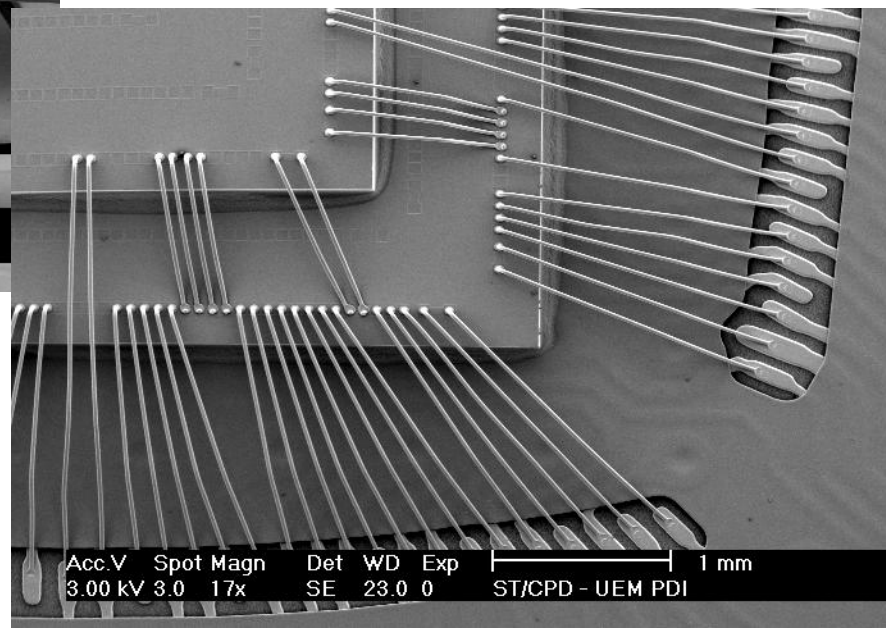
- 0.18um Working Silicon
- Speed: 110 MHz
- Average Power @50MHz: 160mW
- Paper at ISSCC 2003

Triple Stacking for SiP



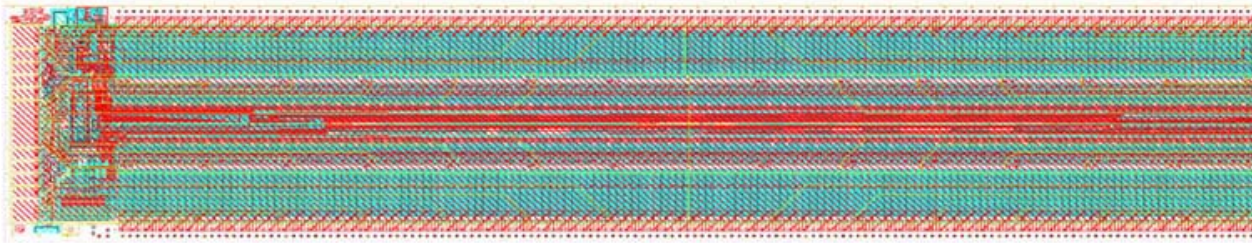
Triple stacked die

Multichip chip wire bonding

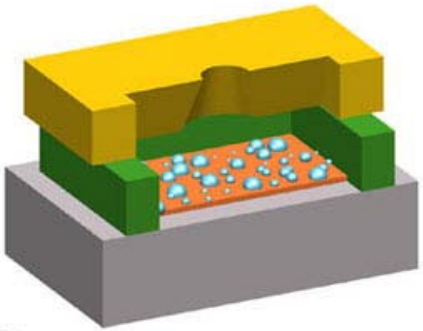


Integrated IC/MEMS Example

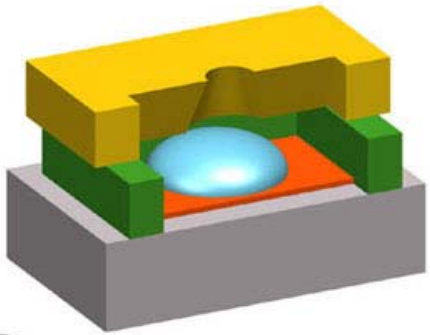
Printer Cartriges



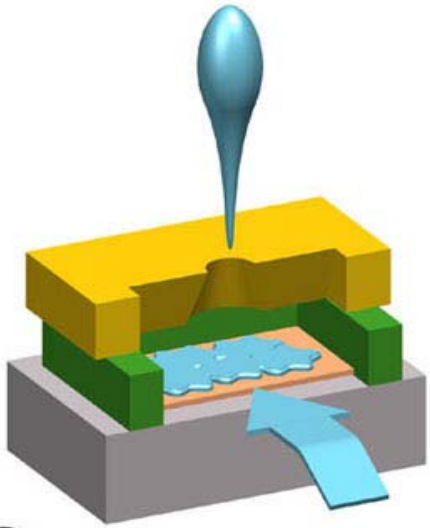
U831A Chip Layout



1 Nucleation

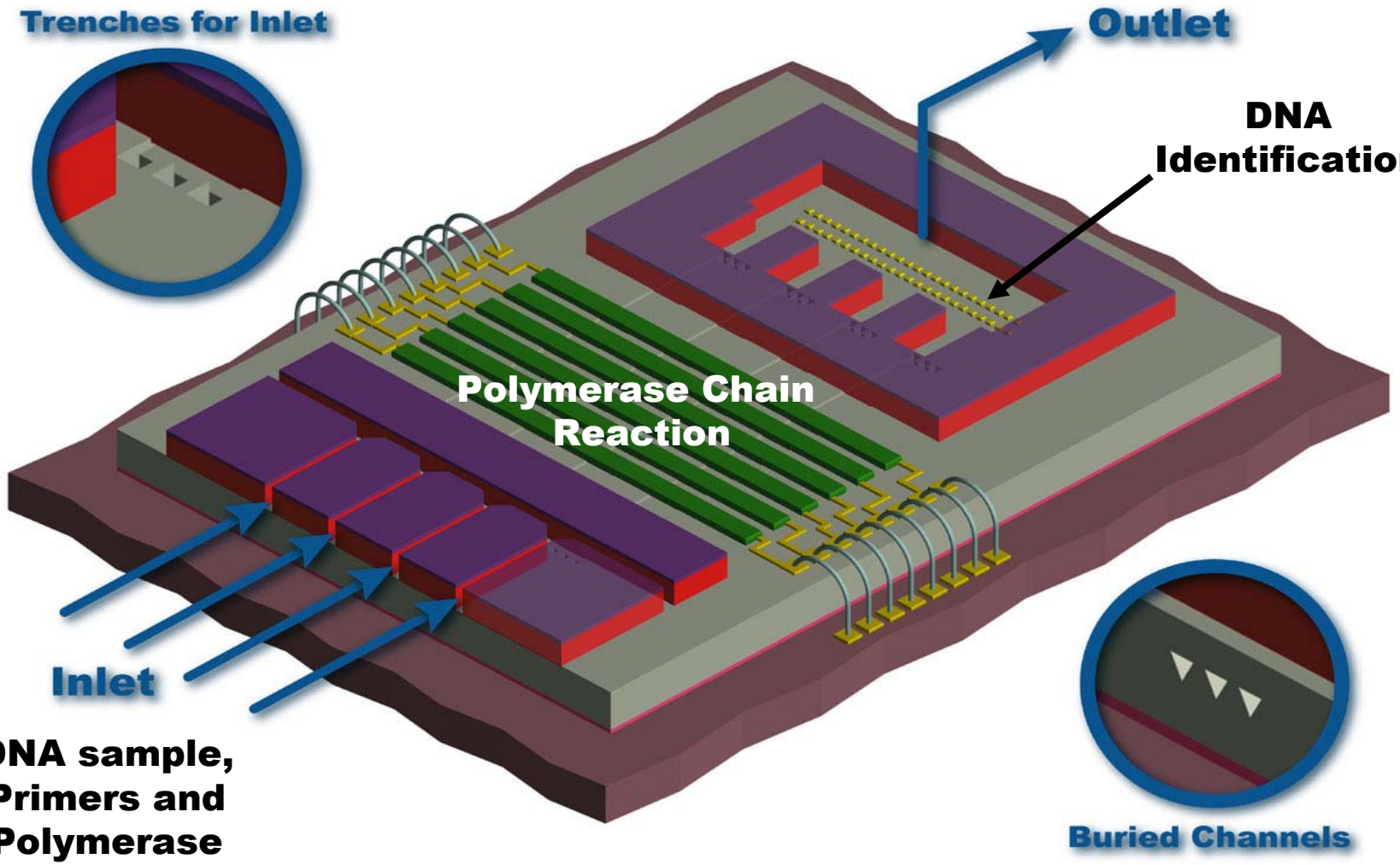


2 Bubble Growth

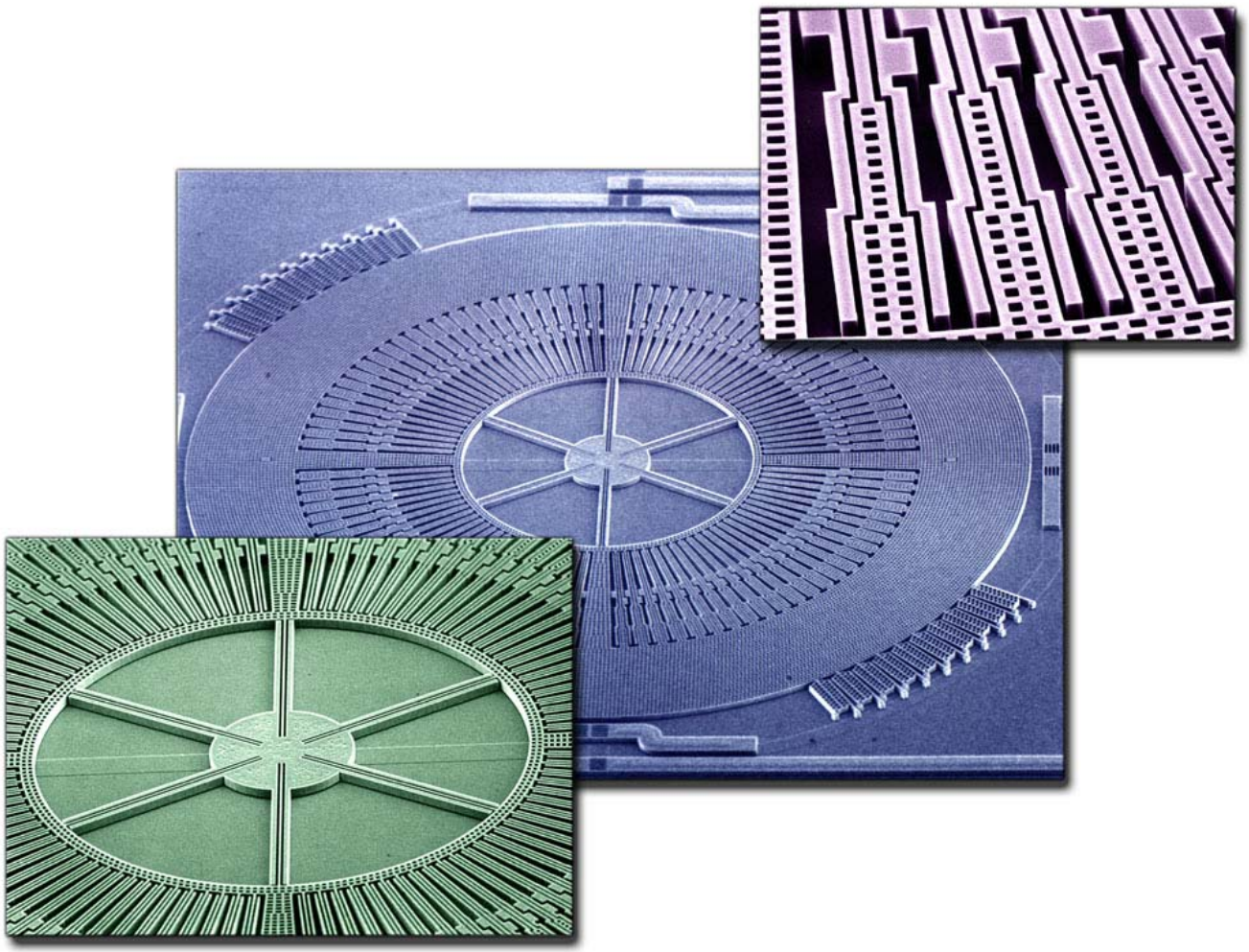


3 Drop Ejection and Refil

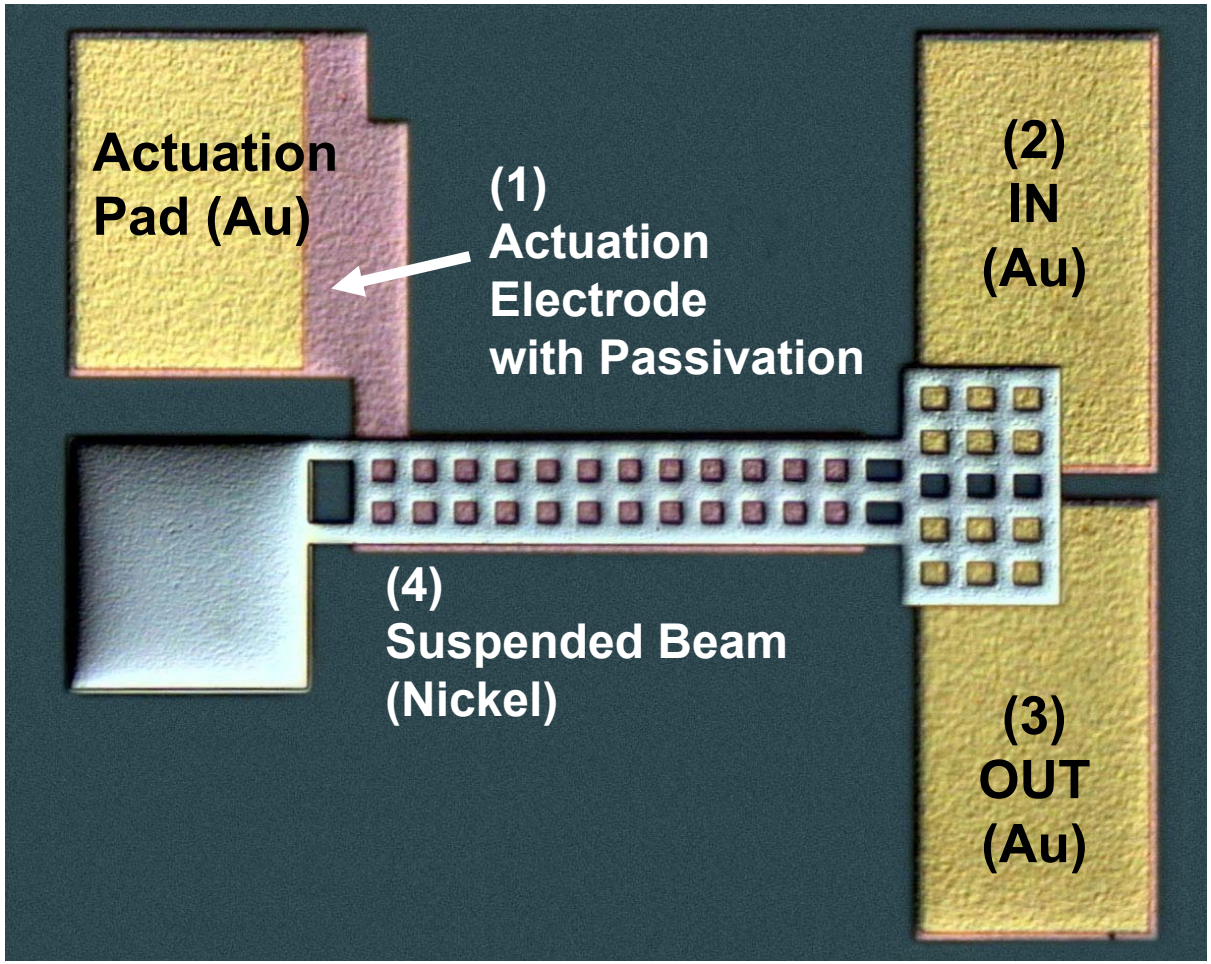
DNA Chip

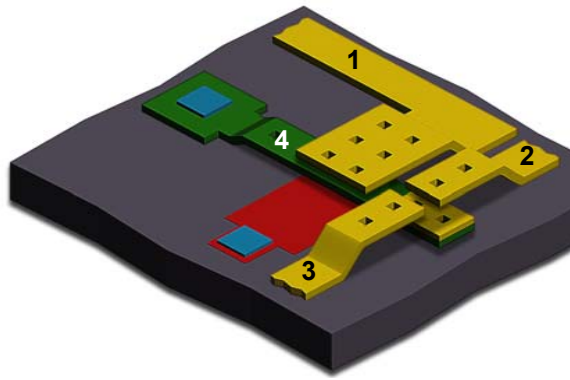

Trenches for Inlet
Outlet
DNA
Identification
Polymerase Chain
Reaction
Inlet
DNA sample,
Primers and
Polymerase
Buried Channels

Rotational Accelerometer

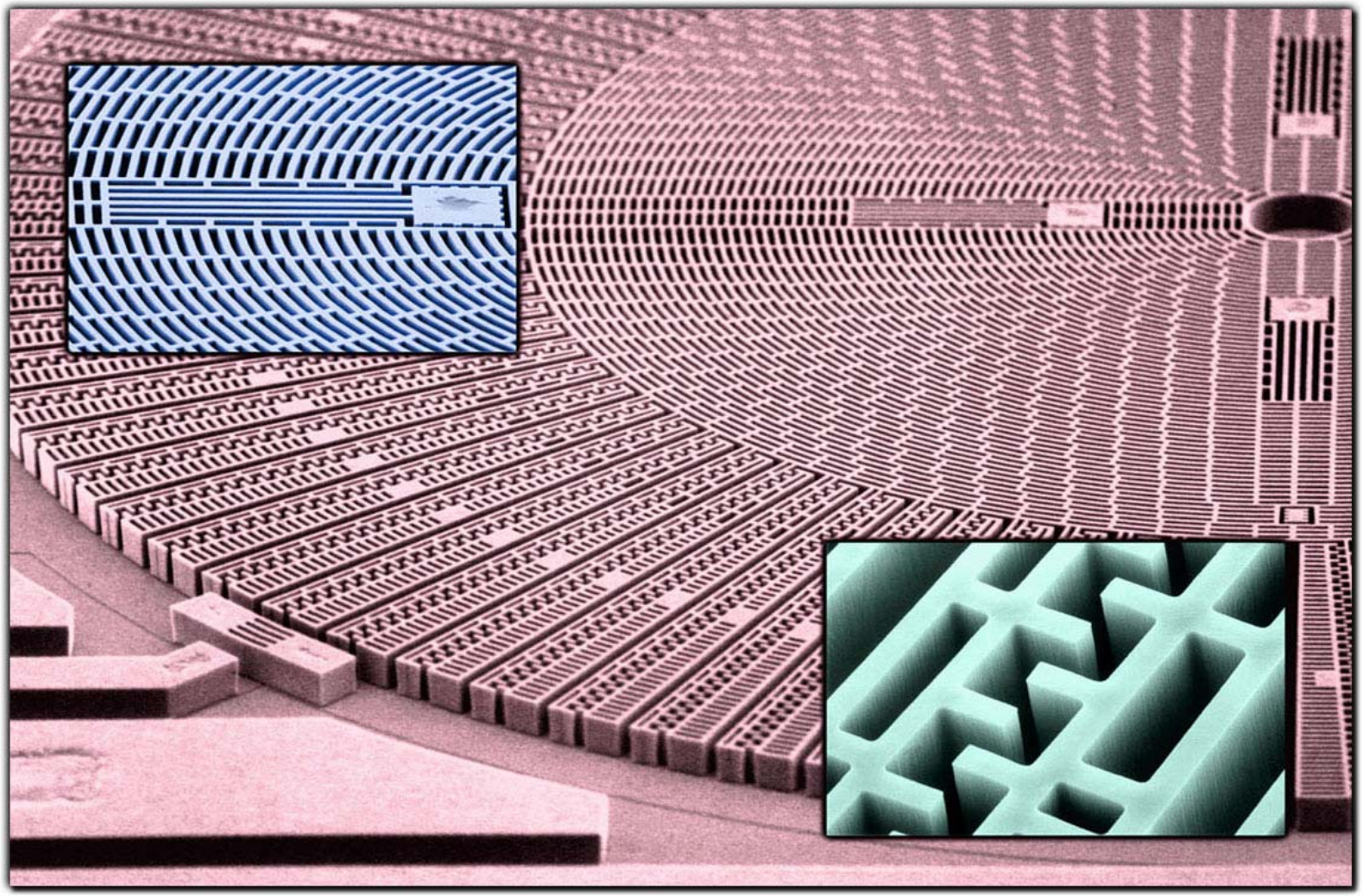


Series RF Switch



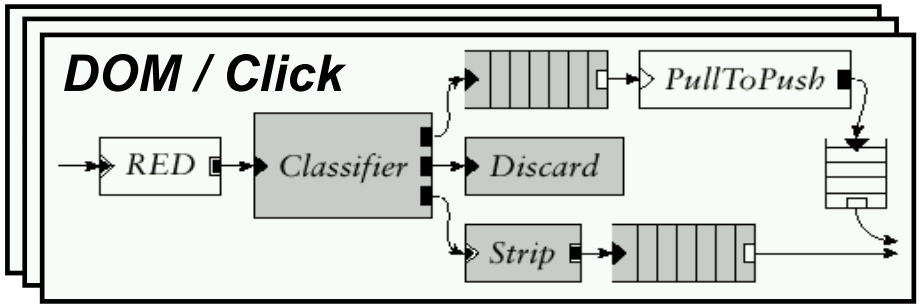


Micromotor



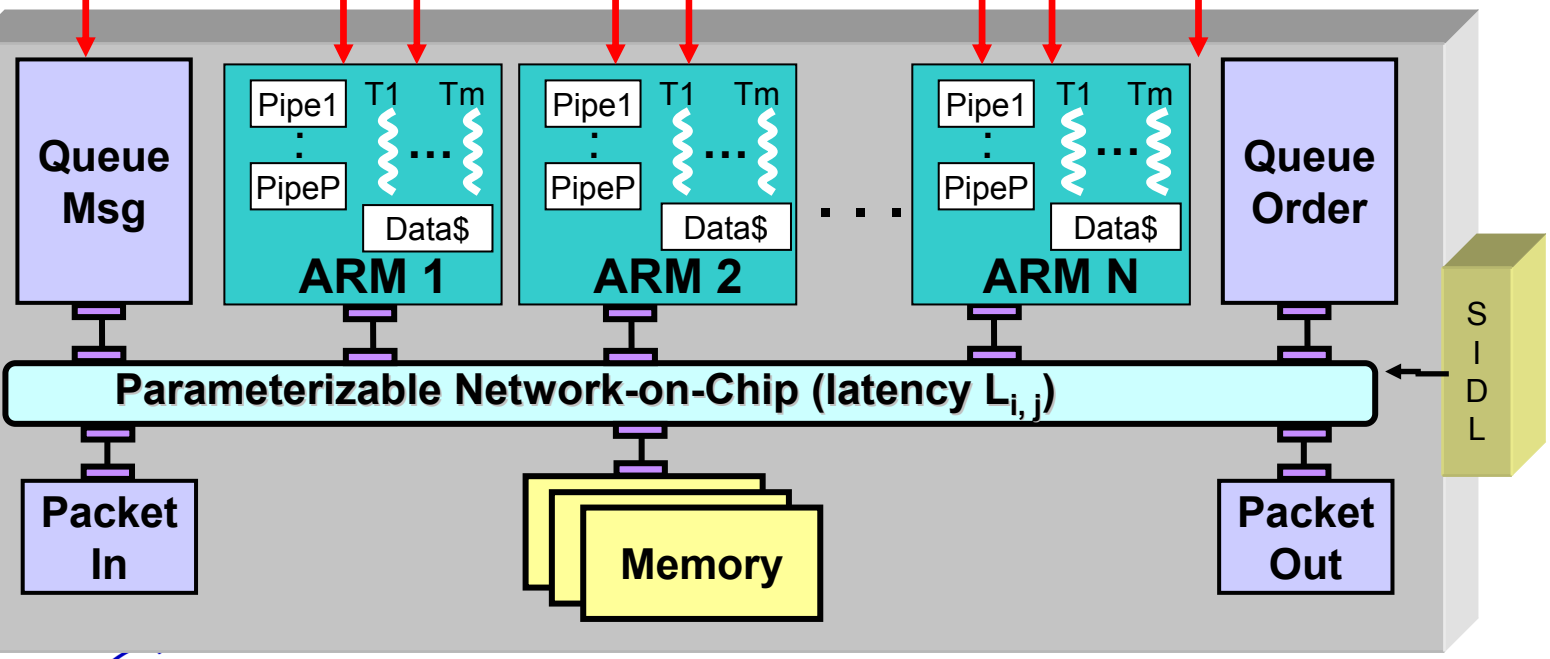
Rapidly rising number of embedded prog'ble cores on-ch

10 Gb/s IPv4 packet forwarding

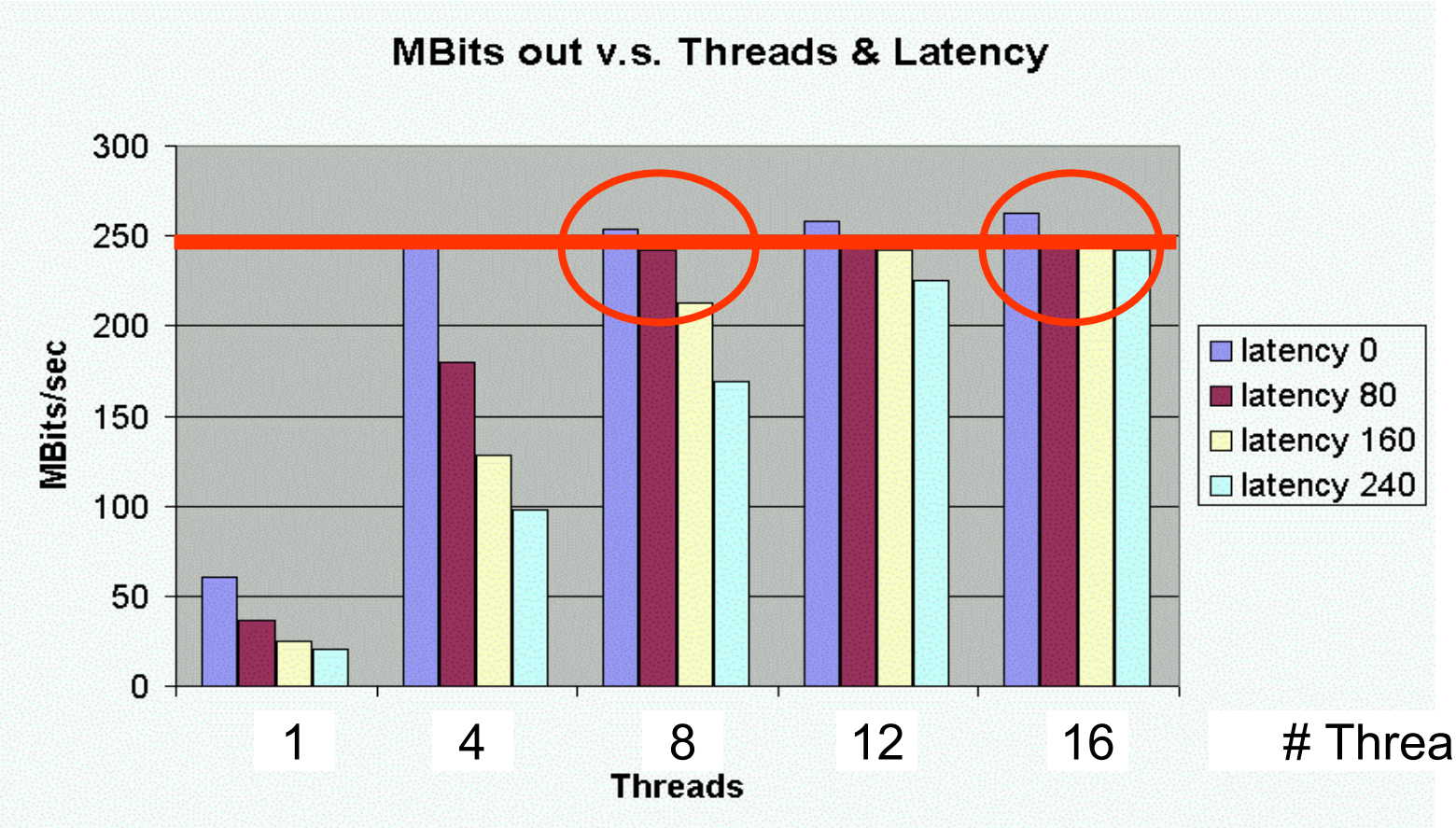


processors N =
clock = 500 MH
pipe stages = 4
threads Tm = 3
D$ sets = 256
D$ size = 4 KB
Latency $L_{i,j}$ = 320

Automatic mapping on MProc architecture



IPv4 Simulation Results

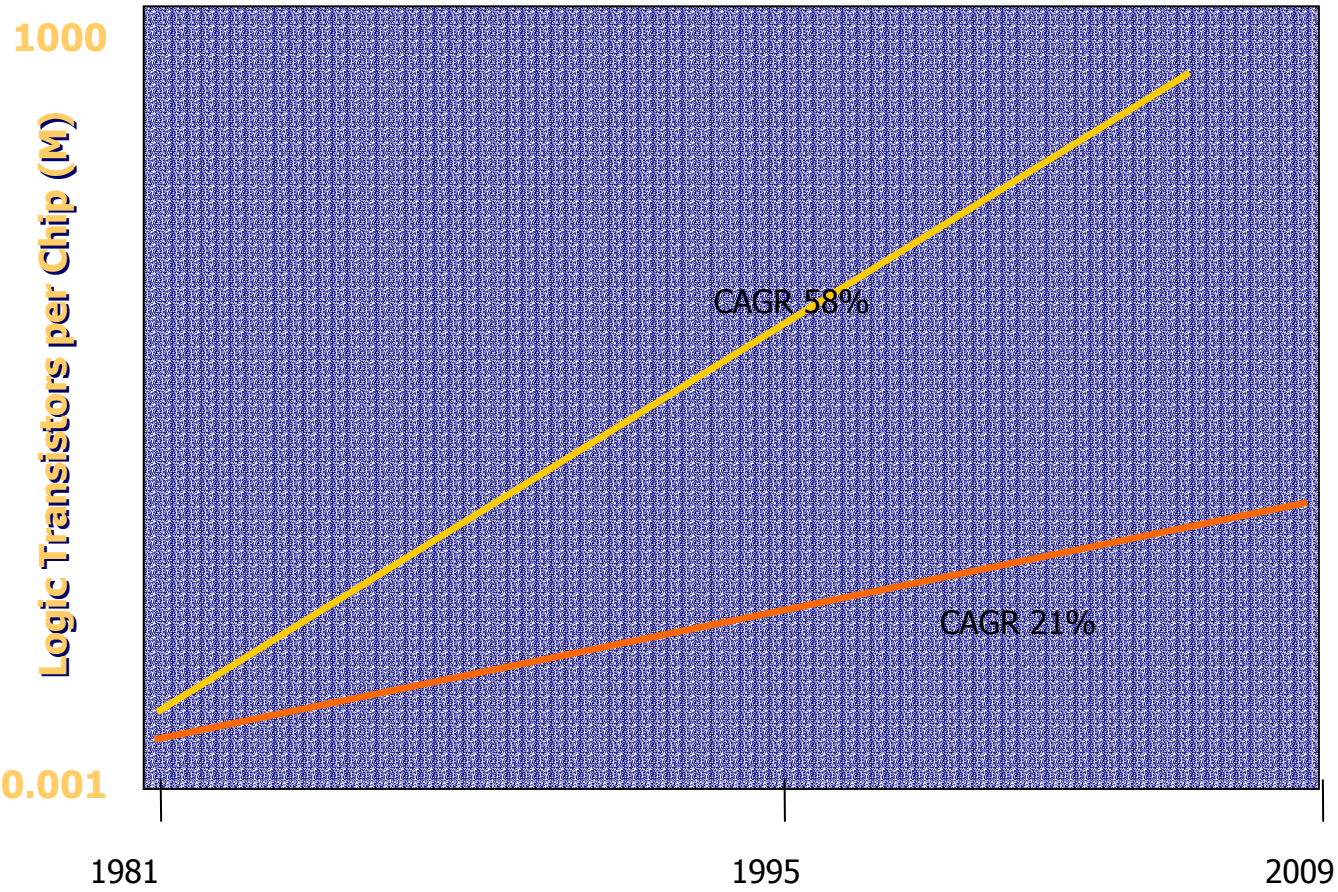


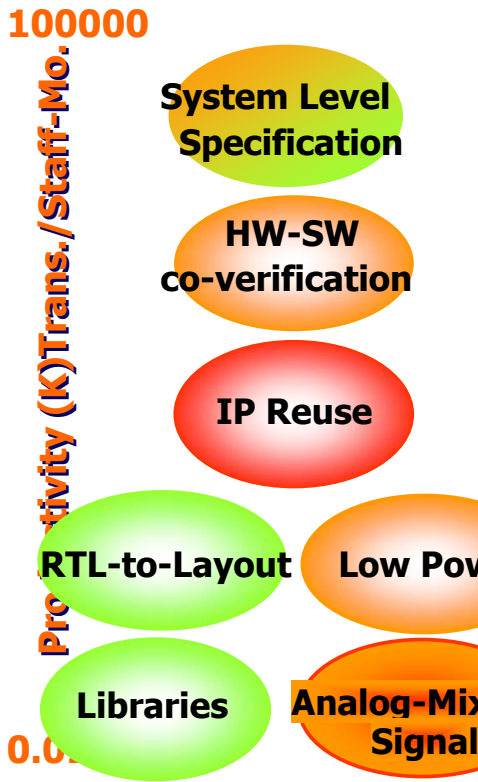
- Normalized results for 1 ARM
- 250 Mbits output: 8 threads absorbs 80ns NoC latency
  16 threads absorbs 240ns NoC latency

Agenda

- SoC trends and links with process/design
- RTL-to-Layout and cell Libraries trends
- System-level, IP reuse and HW-SW codesign
- Off-roadmap activities
- **Conclusions**

Closing the productivity gap





0.13um Nomadik SoC Methodology contributions

System-level design flow:

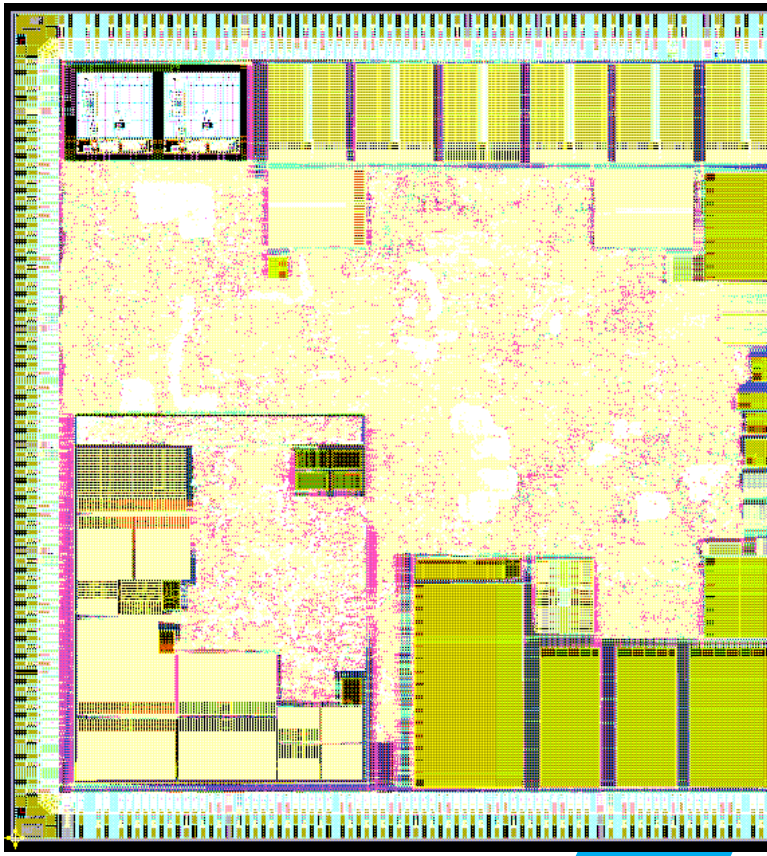
- HW-SW co-sim on Mentor/Seamless
  - Allowing Symbian OS boot on RTL model
- Aptix FPGA-based prototyping
  - For SW development
- Image resizing algorithm synthesis

Test Methodology

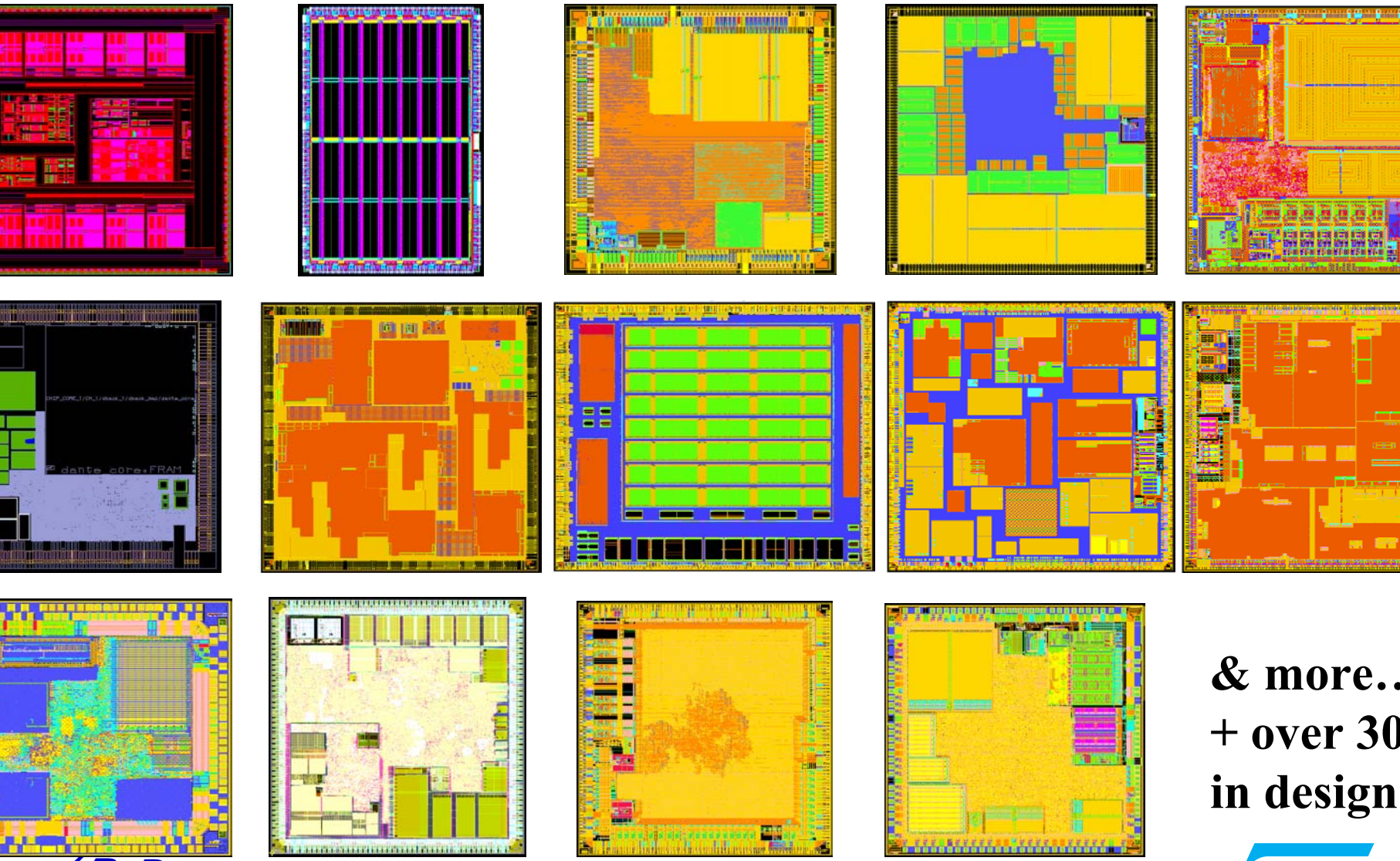
- Design-For-Test latest techniques
  - BIST for e-SRAM
  - BIST for Logic

Low-power Low-leakage methods

- Block Power Shutdown methodology
- Multi-power, multi-voltage regions
- Leakage minimization thru back-bias
- 450MHz Arm926-EJS



0.13µm products taped-out at ST



& more…
+ over 30
in design