Reconfigurable EPGA's Bridging Worlds

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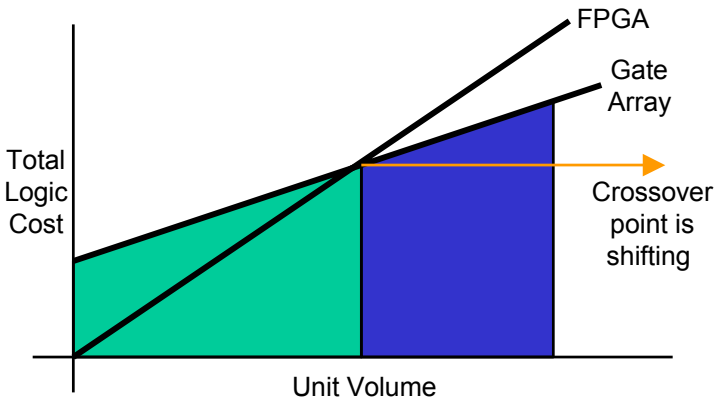
Overview

- What's happening in the world of System on Chip (SoC) ?
- SoC Industry problems
- Compelling reasons for EPGA's
- Challenges in EPGA's
- Applications
- Conclusions and Summary

Why is FPGA Winning?

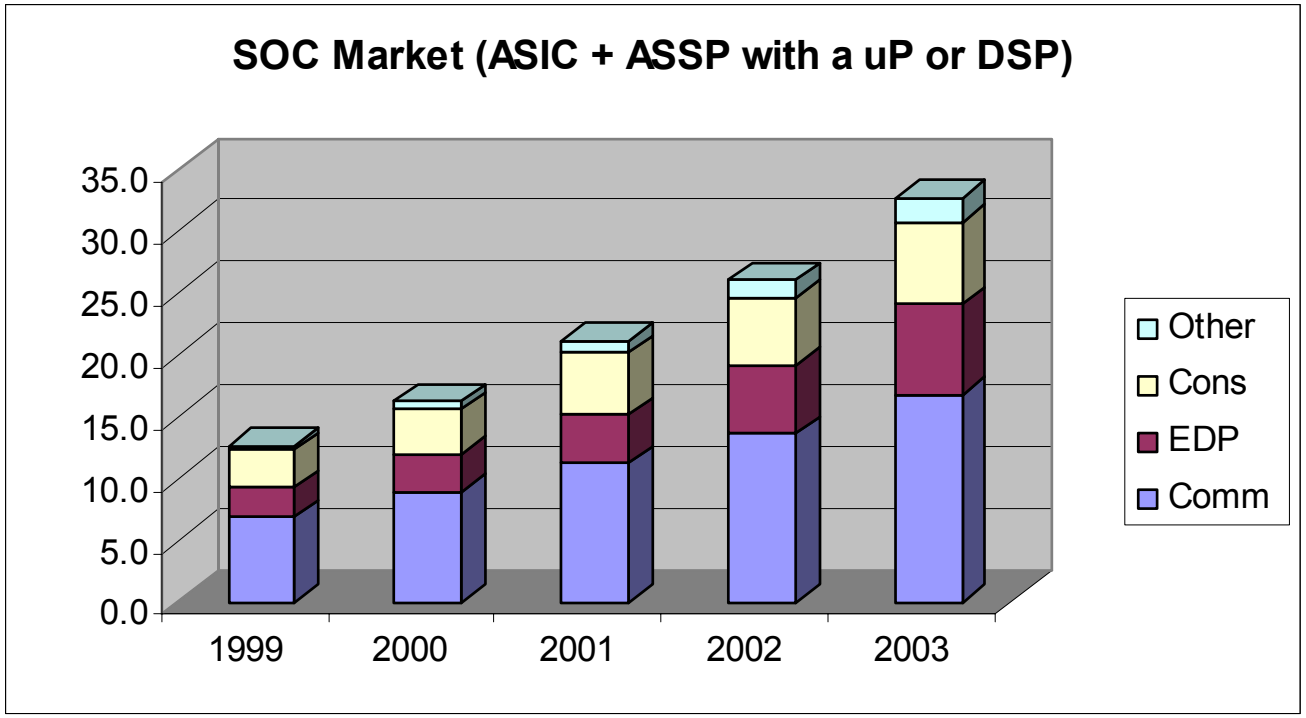
- Product life cycles shortening
  - FPGA reduces development cycle
  - FPGA reduces development cost
- Popularity of reconfigurable systems
  - FPGA allows field upgrade
- Increasing FPGA densities
- Lessening process disadvantage
  - FPGA is a technology driver for independent foundries



What's Happening in SOC ?

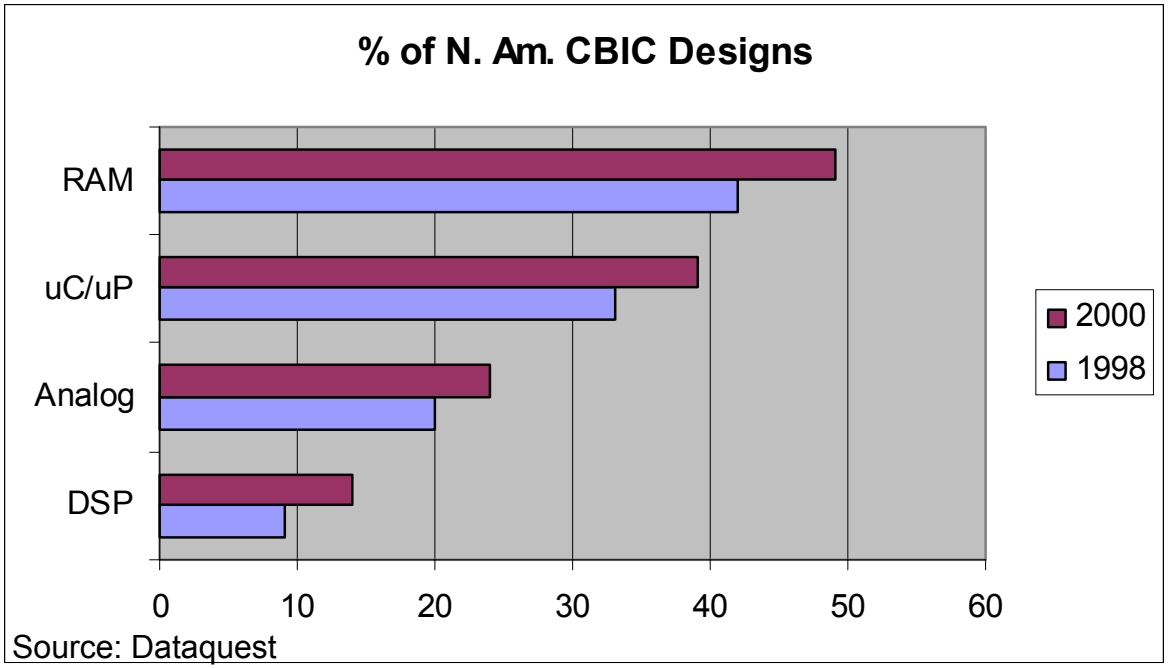
- All logic suppliers (ASIC/ASSP/PLD) are tending toward SOC devices that are specialized for a few applications and targeted toward a small group of customers
- The rich get richer => market share is being concentrated
  - Leverage customer relationships to gain system expertise
  - Large investment needed in IP in order to meet SOC specifications
  - Market share brings economy of scale in unit price
- Time to market is shrinking
  - Revenue and profit impact from delayed entry is immense
  - Communications and consumer lead the charge to 6 month product life
- Development costs are exploding
  - Mask sets cost
  - Complexity of design
- Specialization and partnership rule the day
  - Design services, IP, Software, Tools, Foundries, Packaging, Test

System on Chip - The Most Significant Trend in the Industry



Source: Dataquest

When Will SOC Impact FPGA?



- SOC has already taken significant share from every type of IP that can be manufactured on a standard CMOS process
- Modular processes will enable embedded DRAM and Flash markets

SoC Industry Problems

- Silicon re-spins becoming increasingly expensive
  - Both in development time and cost -- 2 re-spins is the standard
- For OEMs, system complexity is staggering
  - High risk of design errors, product delays, added costs
- Internal and external pressures to cut time to market
  - Every week of delay is 1% of market share lost
- Need to enable the next-level of platform-based design
  - 6-12 months product lifecycles require design reuse
- Industry standards and product features are continually emerging and changing
  - All first MPEG4 chips were non-compliant. What will happen with RapidIO, Fiberchannel, Bluetooth, etc.?
- Need to add design flexibility and reconfigurability to SoCs
  - Field updates will be part of the game plan
- Ongoing push to integrate functionality and scale down size

Compelling Reasons to Embed FPGAs

- Save SoC development cost and time via flexibility
  - EPGA cores allow debugging anywhere in the design cycle
  - Reduce risk of additional NRE and mask set costs
- Avoid expensive re-spins
  - Mask set costs are headed toward multi-million $$$ each
- Enable next-level of platform-based design
  - Rapid Prototyping and Productization
  - ASIC designs can start before the application is stable
  - Time-to-market and cost advantages gained as each application or board is re-targeted
- Keep up with evolving standards and changing features
  - Extend the life of ASICs/ASSPs with field reconfigurability

Challenges of Embedding FPGA

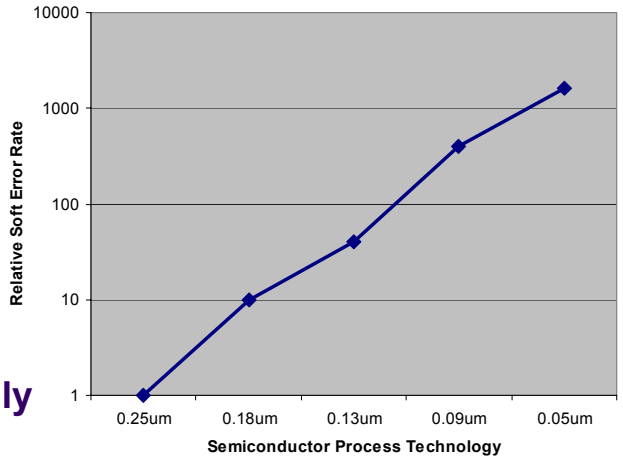
- High barriers to entry for FPGA architecture development
- Support of the existing SOC design methodology
  - Modeling/Verification at many levels of abstraction
  - Support for SOC tools: static timing analysis, formal checking, power analysis
  - Merged test methodology
- FPGA Core related challenges
  - Software that can cascade FPGA blocks on the fly
  - Pin fixing required
  - Access to the core for programming and test
  - Interface between the FPGA and the rest of the SOC
  - Debug with limited core access
- Process compatibility / porting

ASIC Designer Expectations

- Board-Level Expectations
  - Single-chip solution
  - Live-at-power-up
  - Non-volatile
  - Well-behaved power-up profile
  - Firm Error immune
  - Some level of design security
- Design-Flow Expectations
  - Deterministic design flow
  - Incremental capability
  - Heavy simulation based
  - Min-Max timing analysis

How Serious are Soft Errors?

- New processes increase the risk of soft errors
  - Greater percentages of neutrons can generate charged particles with sufficient energy to cause soft errors
- When SRAM cells are used to configure an FPGA, configuration soft errors can potentially cause serious system impact
  - At a minimum, the configuration data must be reloaded to recover
    - *Can take many clock cycles before configuration loss is discovered*
  - In many cases, the device must be power-cycled to clear the error
    - *May involve a complete system reset*
  - High current due to contentions in a mis-configured device may damage device or board
    - *Simultaneously-enabled tie-offs to power and ground, for example*
- Mitigation methods rely on redundancy with monitor circuits
  - Increased board space, BOM cost, power consumption, system complexity, design time, ...

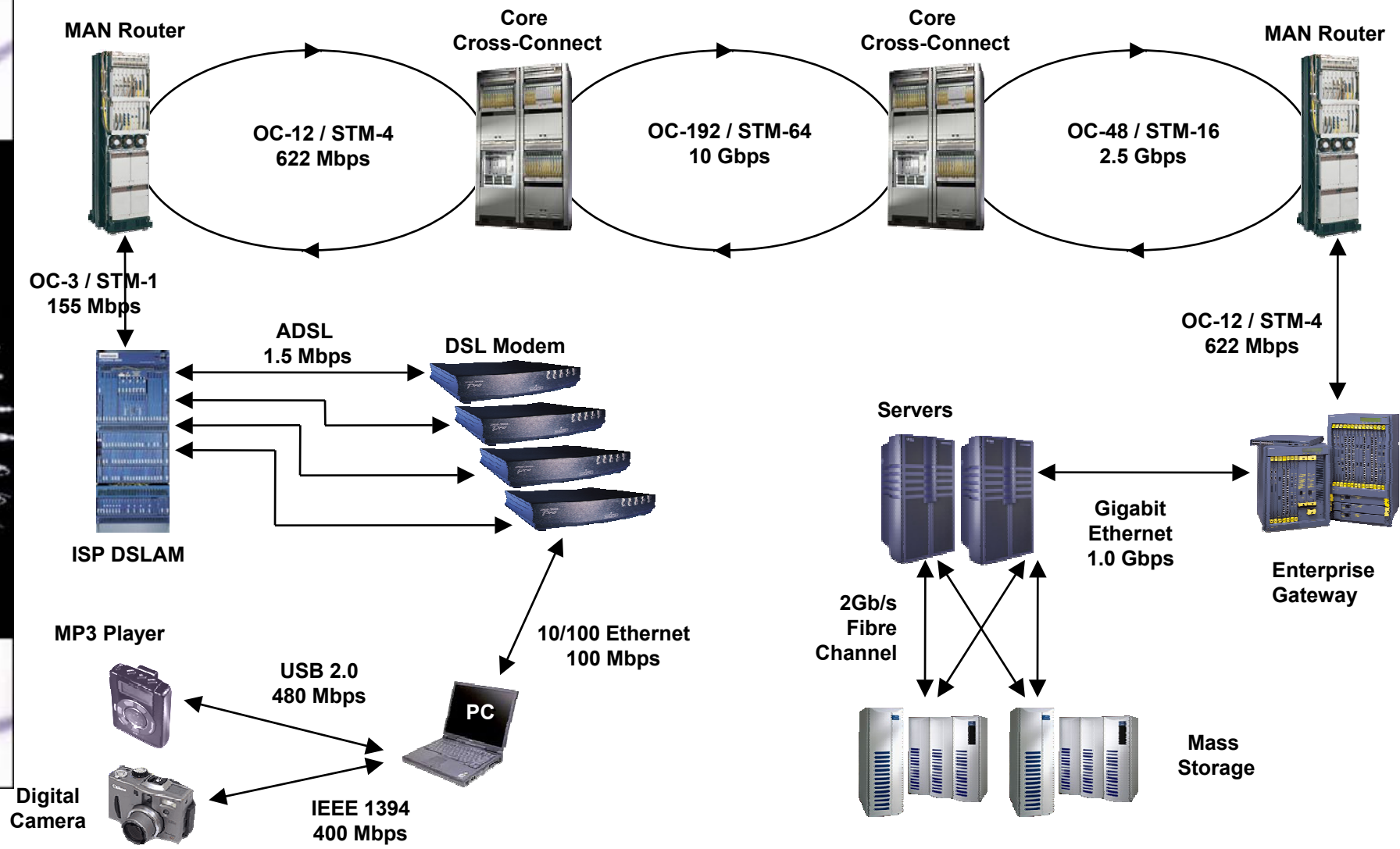


Source: iRoC Technologies / Semico Research Corporation

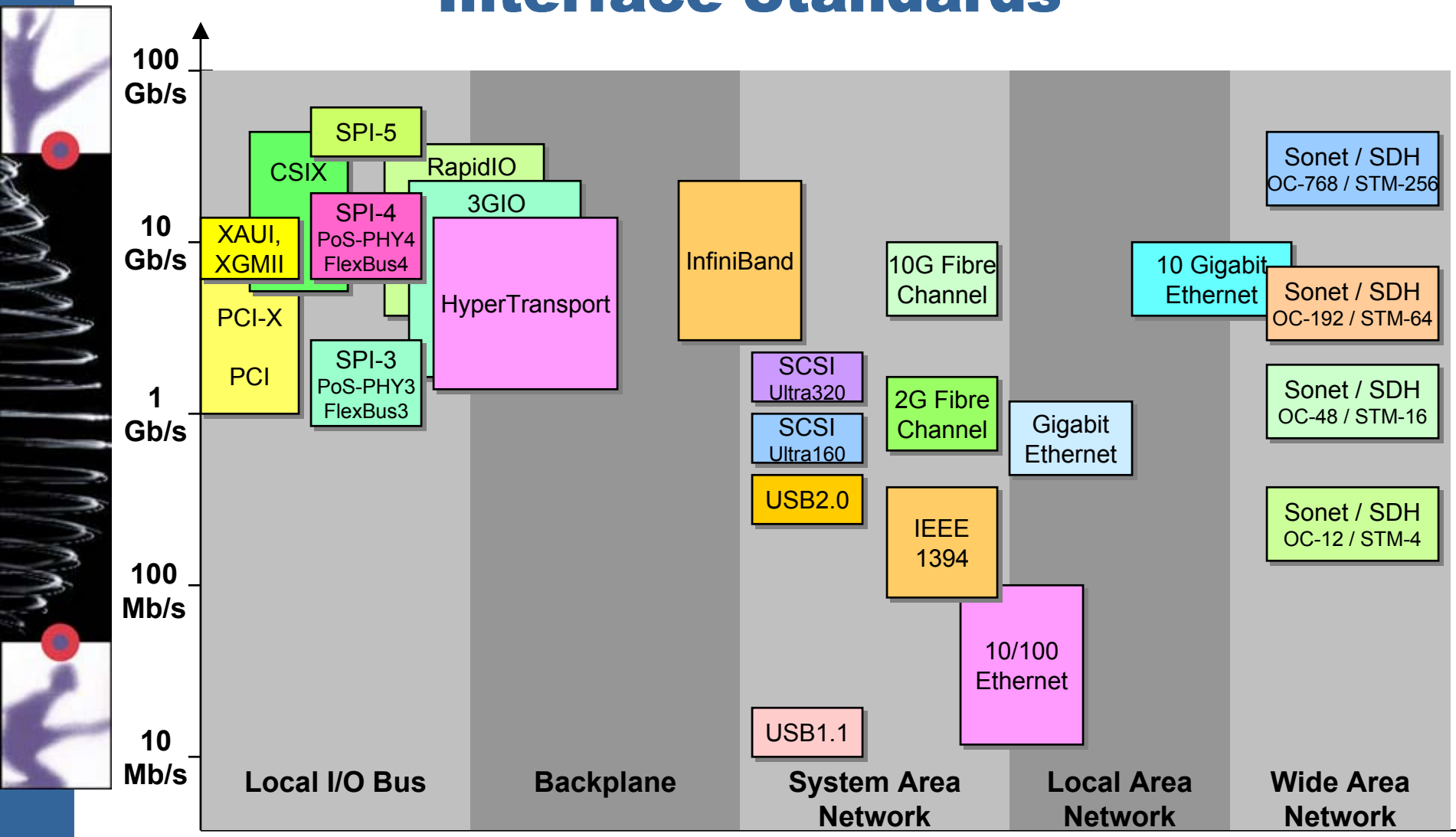
EPGA Application Opportunities

- ASIC and ASSP suppliers see the advantage of reconfigurable SoCs
  - Anywhere a superset of functionality can offer bigger market penetration
    - Networking example: combining an SDH/Sonet interface with a Gigabit Ethernet port
  - Anywhere small changes trigger the design of new versions and variants
    - Such as copiers, LCD controllers, automotive electronics
  - Anywhere the reach of MCUs and DSPs can be broadened by designing one device to fit many interfaces
    - Interface example: USB, PCI, CAN, I2C, PWM, Ethernet, etc.
- As main drivers in networking and communications

Increasing Bandwidth at All Levels of the Network

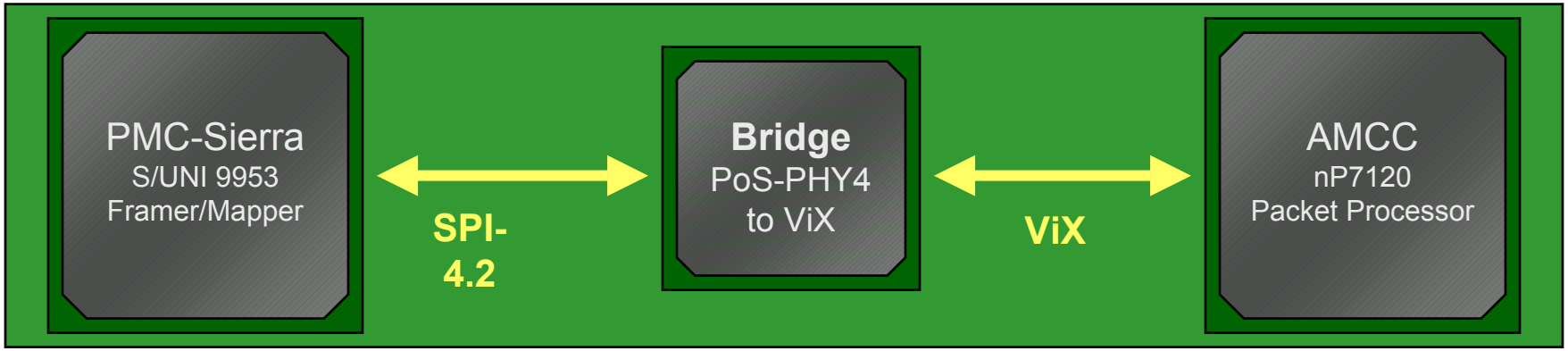


Exploding Number of Communications Interface Standards

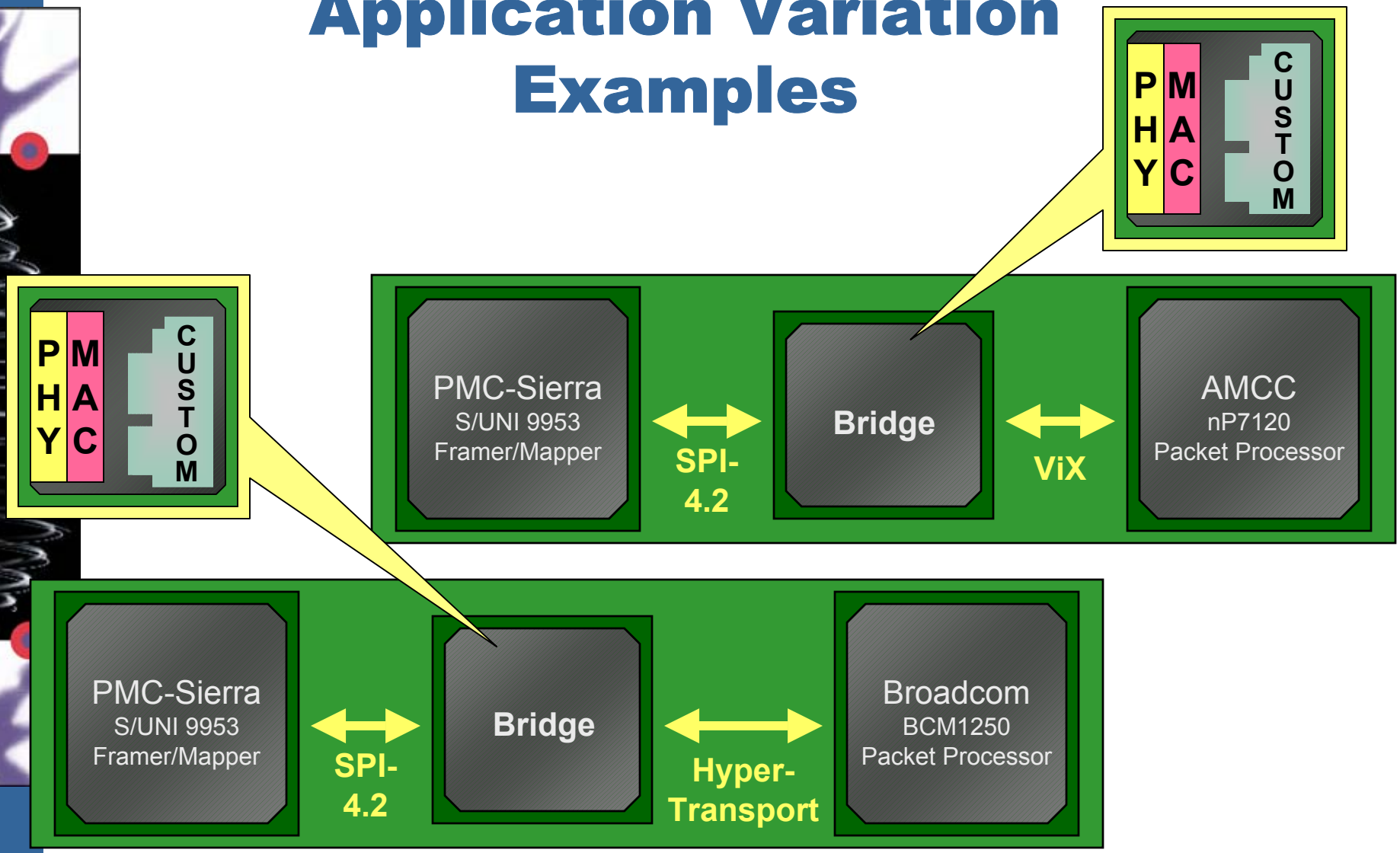


Interface Standards !?

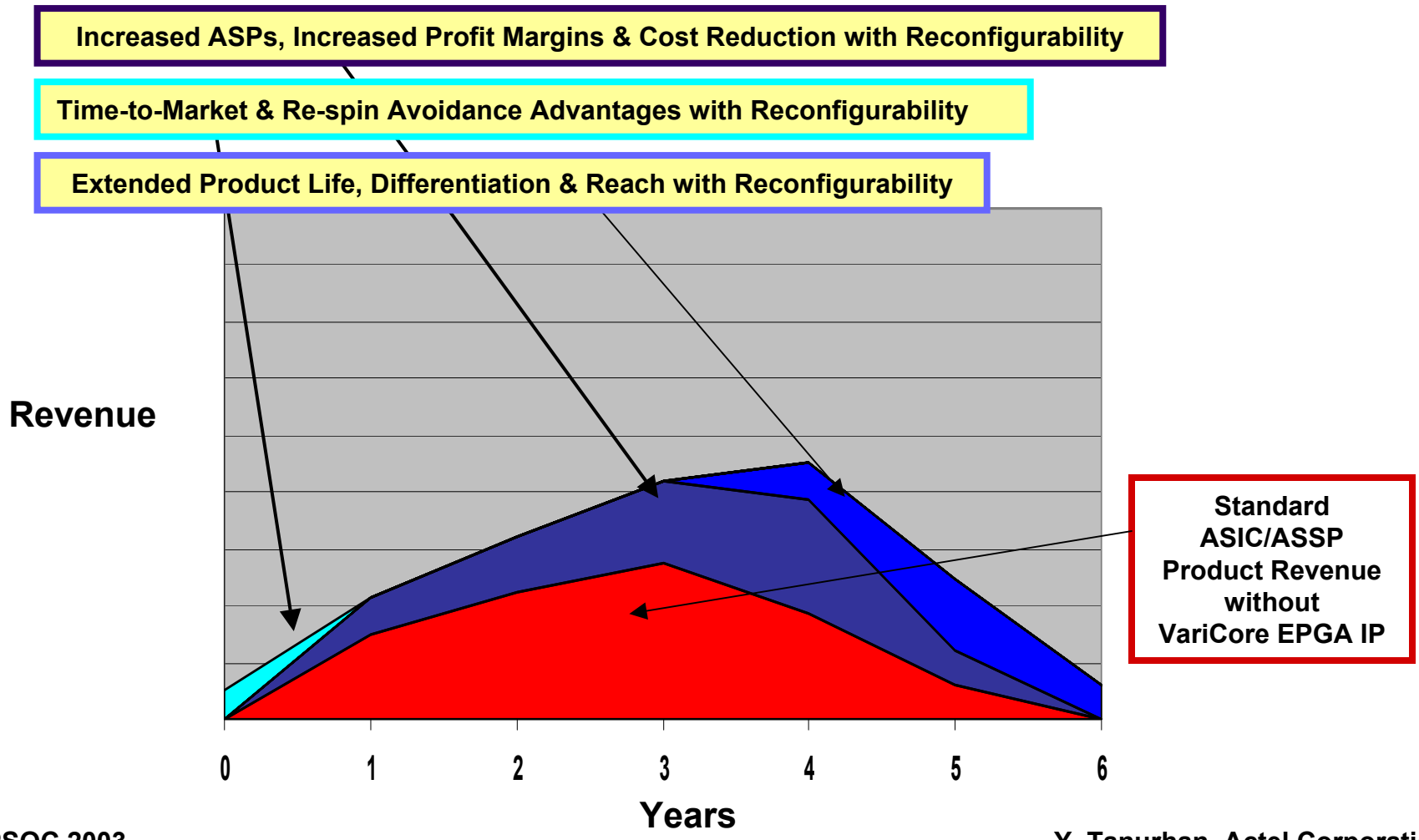
- **Designers need devices to BRIDGE these interfaces so that they can make their standard parts communicate with each other**



Application Variation Examples



What does EPGA Reconfigurability Enable



How EPGA based Bridges Solve Interoperability Problems

- Bridges include a combination of . . .
  - Dedicated high-speed I/O circuits
    - Banks of 3.1875 Gbps CML Transceivers
    - Banks of 1.0+ Gb/s LVDS Transceivers
  - Embedded interface protocol controllers
    - For example XAUI, SPI-4.2, Fibre Channel, 3GIO, RapidIO, HyperTransport . . .
    - Implemented in ASIC technology
      - *High density = lower cost*
      - *Fixed timing = easier verification and faster timing closure*
      - *Standard cell = lower power*
  - High-speed, high-utilization user programmable logic
- Three elements united in a single device
  - Includes seamlessly integrated I/O circuits and protocol controllers

Designers Need to Meet the Demands for Higher Bandwidth

- Profusion of New High-Performance Interface Standards
  - Source-synchronous switched-packet interfaces
    - *SPI-4.2 - up to 12.8Gb/sec*
    - *CSIX - up to 32Gb/sec*
    - *HyperTransport - up to 3.2GB/sec*
    - *RapidIO parallel - up to 4GB/sec*
  - Serial switched-packet interfaces
    - *XAUI - 10Gb/sec*
    - *RapidIO serial - up to 10Gb/sec*
    - *3GIO - 2.5Gb/sec and higher*
  - High-speed serial system-level interfaces
    - *IEEE 1394 / iLink / Firewire - 400Mb/sec*
    - *USB 2.0 - 480Mb/sec*
    - *InfiniBand - 2.5Gb/sec and higher*
- Vendors of Standard parts are not all choosing the same interface!

Embedded FPGA Content for a NetWorking BridgeFPGA™

- Rapid productization through exchangeable IP blocks
  - SPI-4.2
  - 10GE MAC
  - 3GIO
  - HyperTransport
  - RapidIO
  - CSIX
  - Infiniband
  - PCI-X

Key Factors for Success

- A credible FPGA playesr emerges with an EPGA IP core
  - More than 7-10,000 ASIC gates/mm2 in .13 Family
  - Up to 400MHz clock speed with a sweet spot between 75-150MHz
  - Competitive FPGA power consumption / die area
  - Fully integrated with state-of-the-art SoC design methodology
  - Commitment to IP core architectural features
  - Complete and unlimited reprogrammability
- Broad availibility

Key Take Aways

- Frontal attack in the traditional market sector is not always a good path to success
- Disruptive technologies can open new growth potentials and rapid prototyping eases that path
- EPGAs help to reduce design risk and shorten design response
- EPGAs can act as a shield and sword
  - Protects users against the effects of evolving standards
  - Protects users from the effects of market shifts
  - Protects ASIC/ASSP suppliers from FPGA platform competitors
  - Helps rapid productization

Enabling ASIC and ASSP suppliers to get to market faster and stay there longer