65nm: Business As Usual?

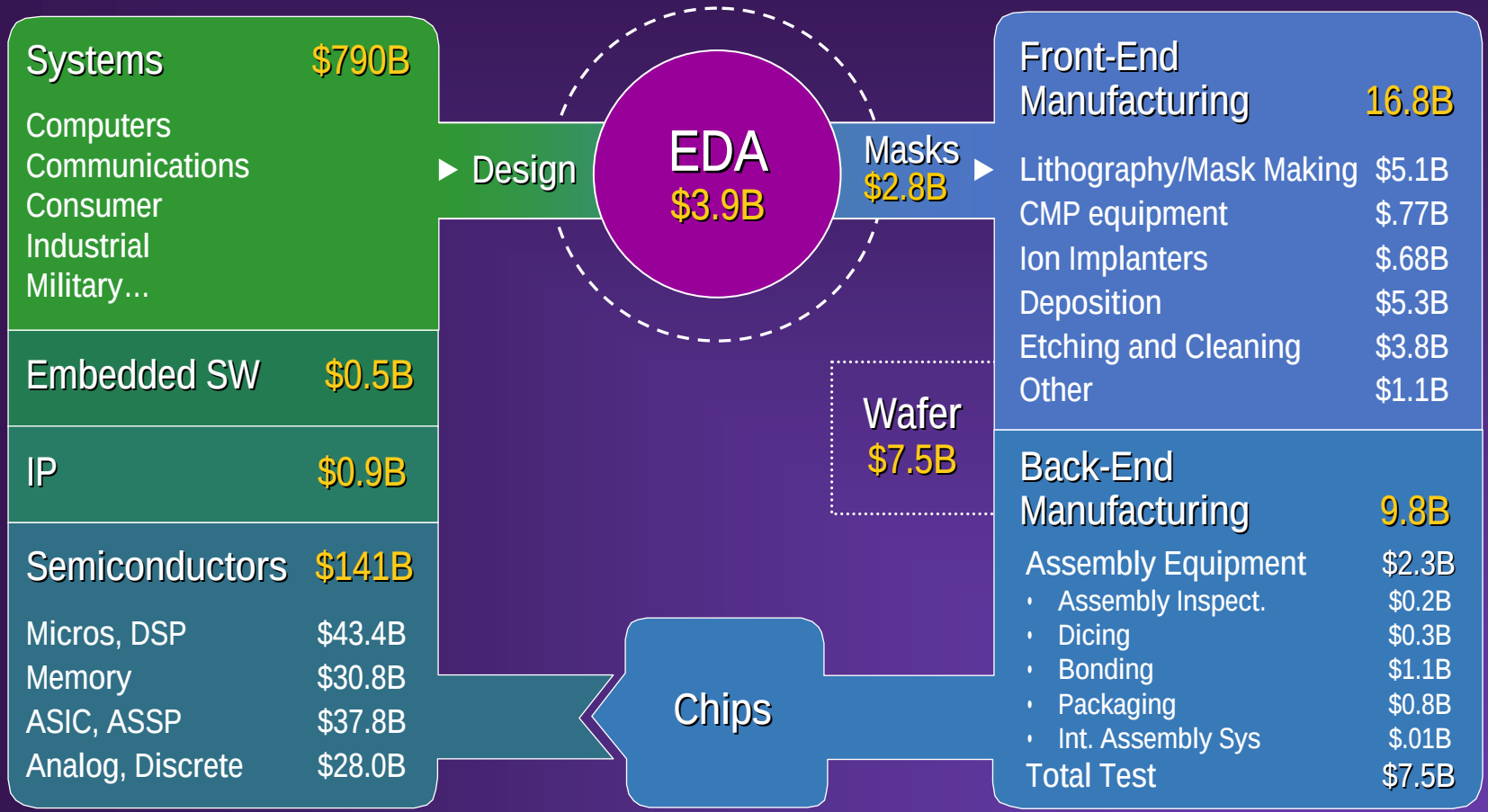
Dr. Raul Camposano

Senior Vice President,

Chief Technology Officer

Synopsys, Inc.

Semiconductor Process Flow



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Market size for 2003 Sources: VLSI, Dataquest, Synopsys Estimates

Technology Roadmap

Smaller, Cheaper

Increasing Design Cost

Faster

Parasitics
CD Variability

Less Power

Leakage
Power Density

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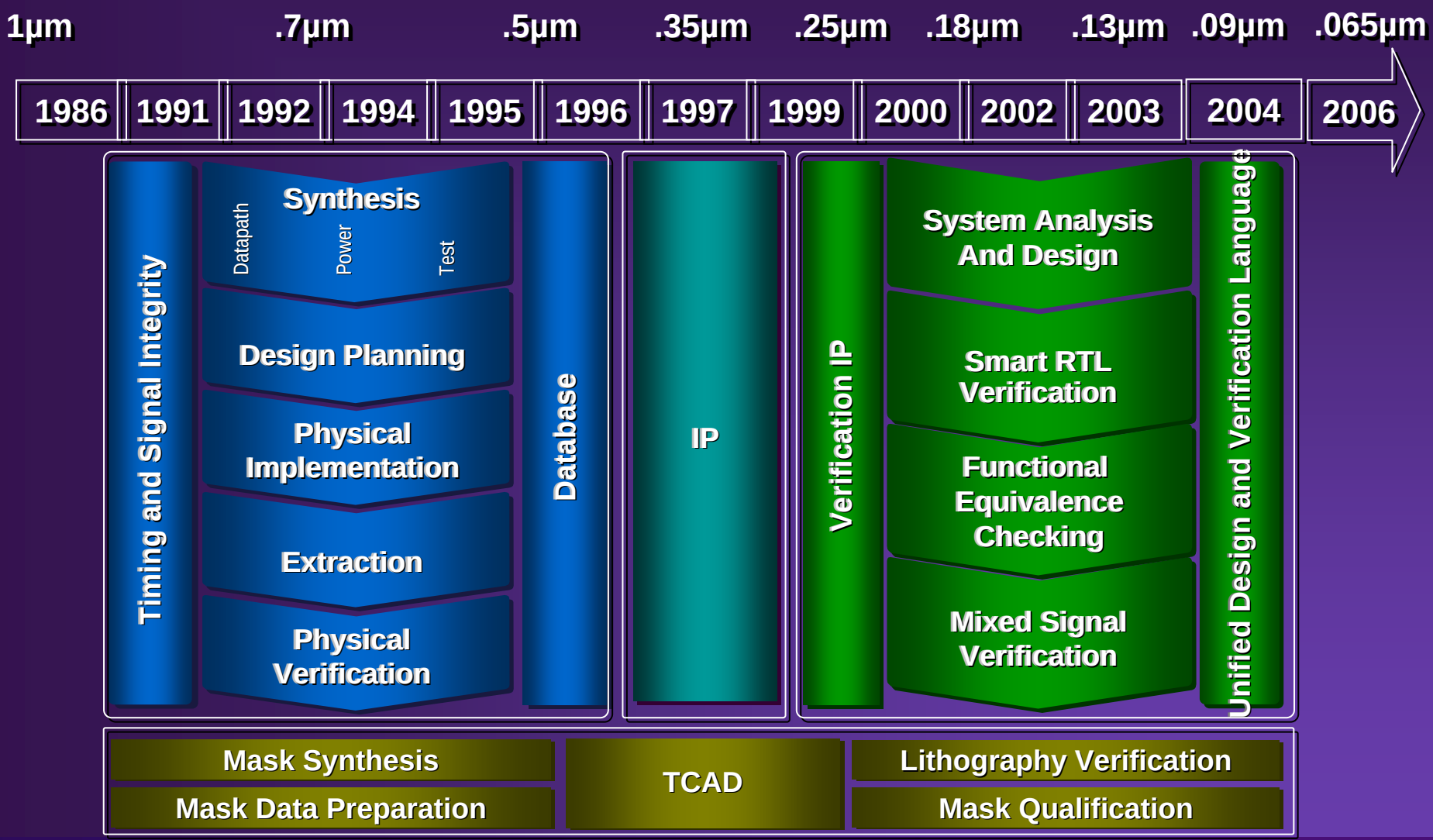
Technology Roadmap



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Cost

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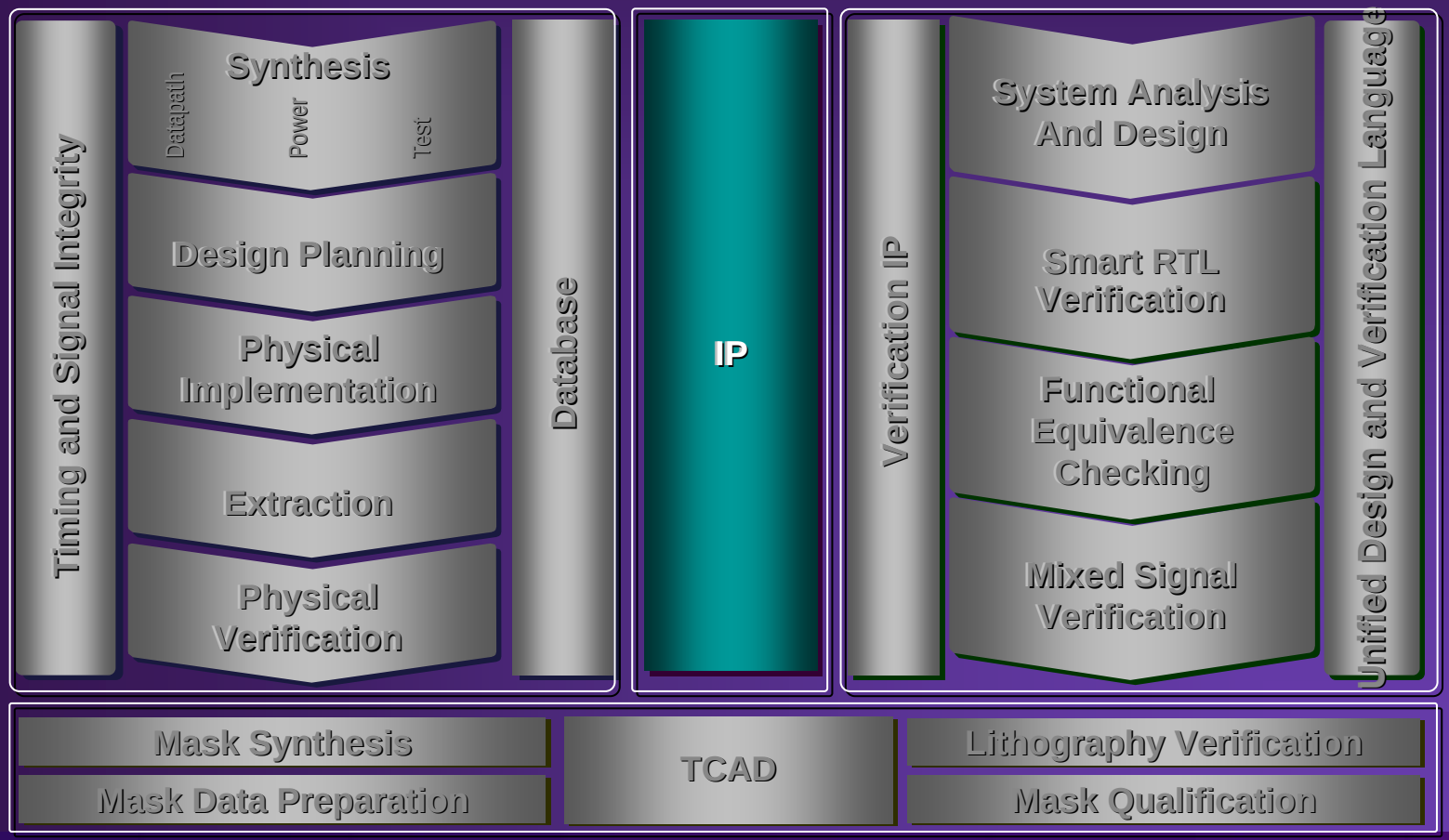
IP Based Methodology



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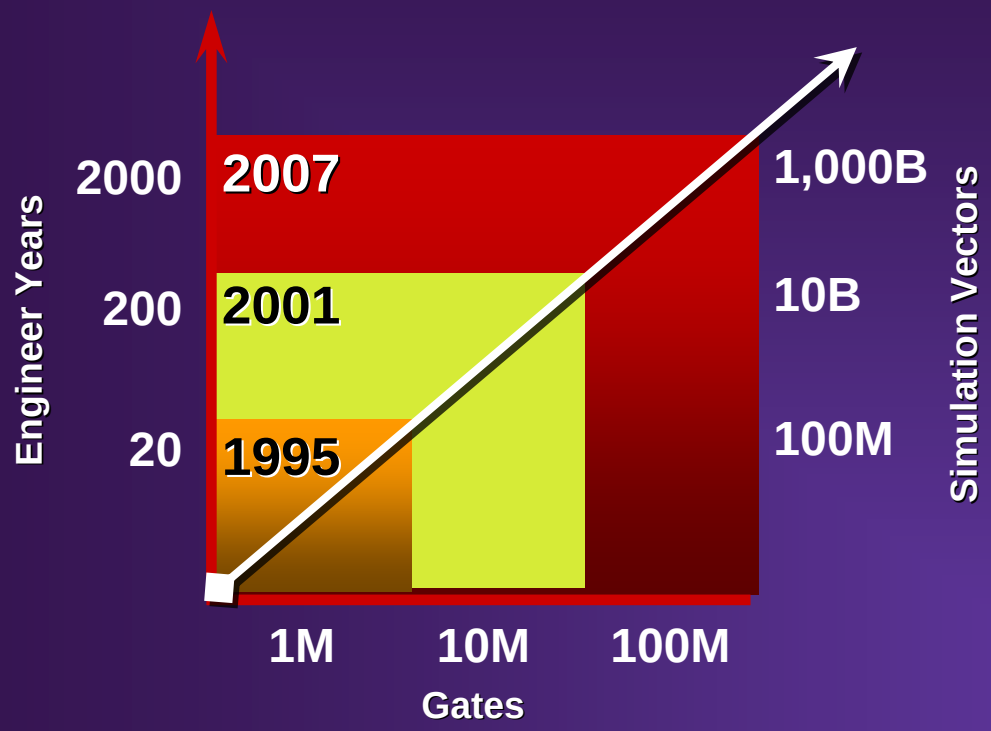
The Designer's Escalating Problem



2,000
engineer years to write 25M lines of RTL

1,000B
simulation vectors to verify

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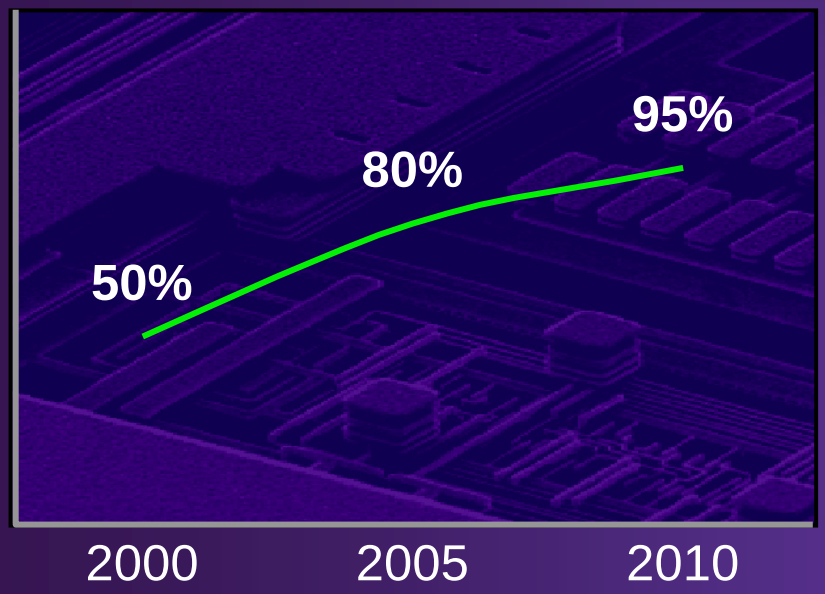
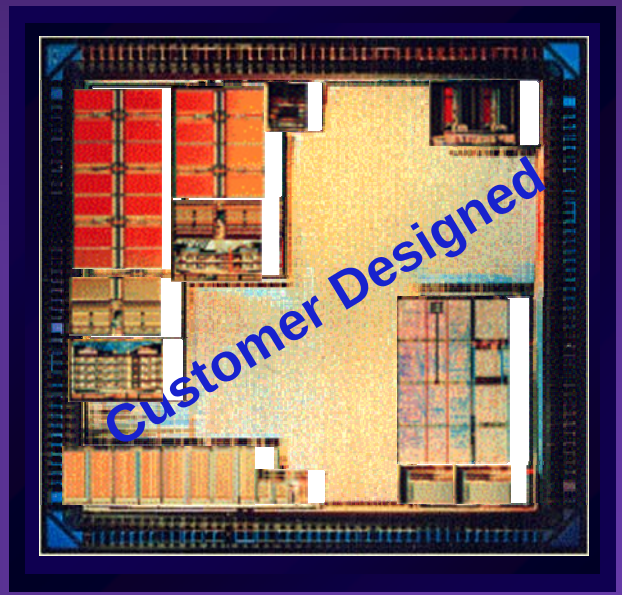
The Solution: IP Reuse

Pre-designed Blocks as % of an SoC



Source: Dataquest, 2000

IP, Memory and SW Increasing



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What Works

Semiconductors	$141B
Micros, DSP	$43.4B
Memory	$30.8B
ASIC, ASSP	$37.8B
Analog, Discrete	$28.0B

Standards enable large volumes

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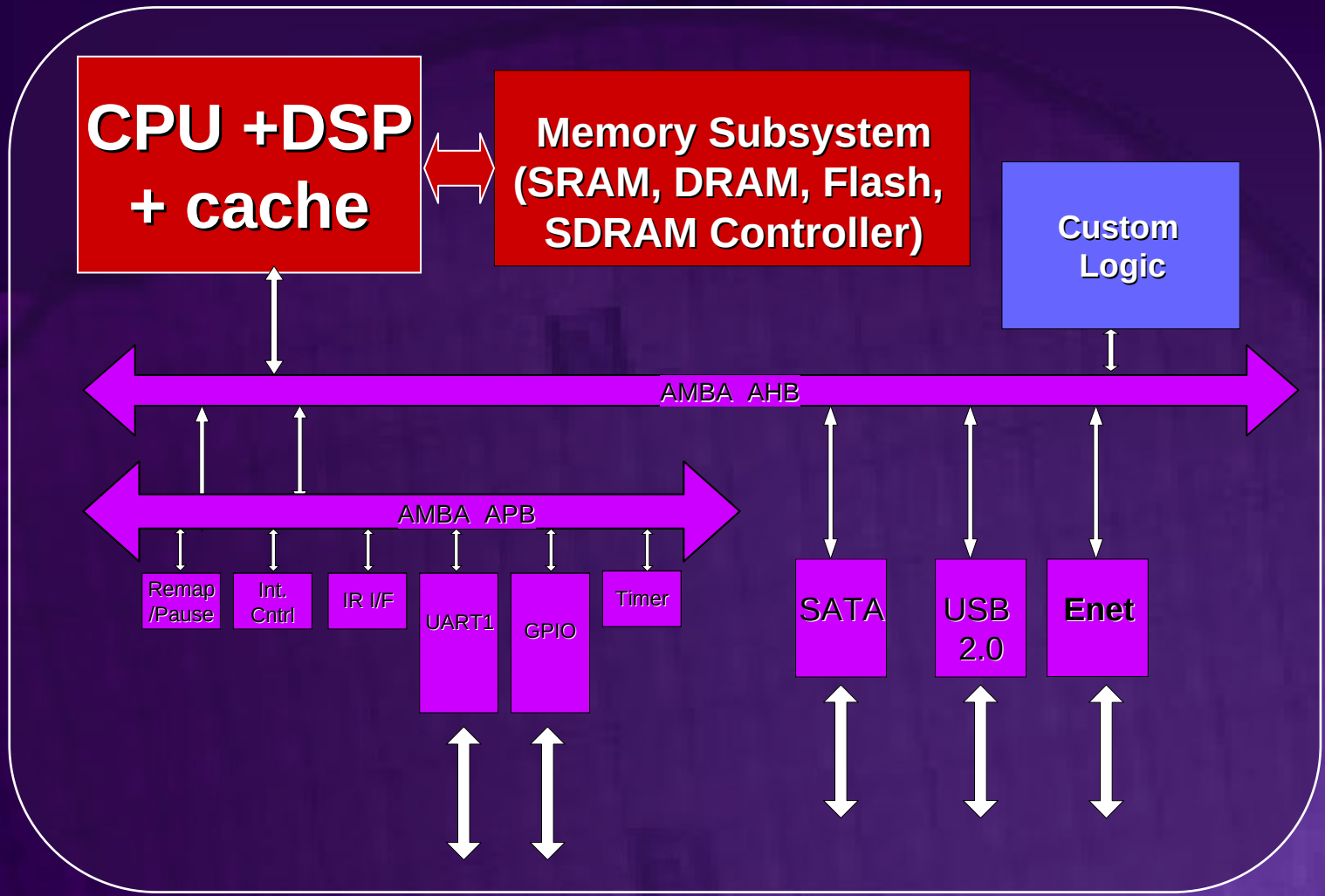
What's In An Soc?



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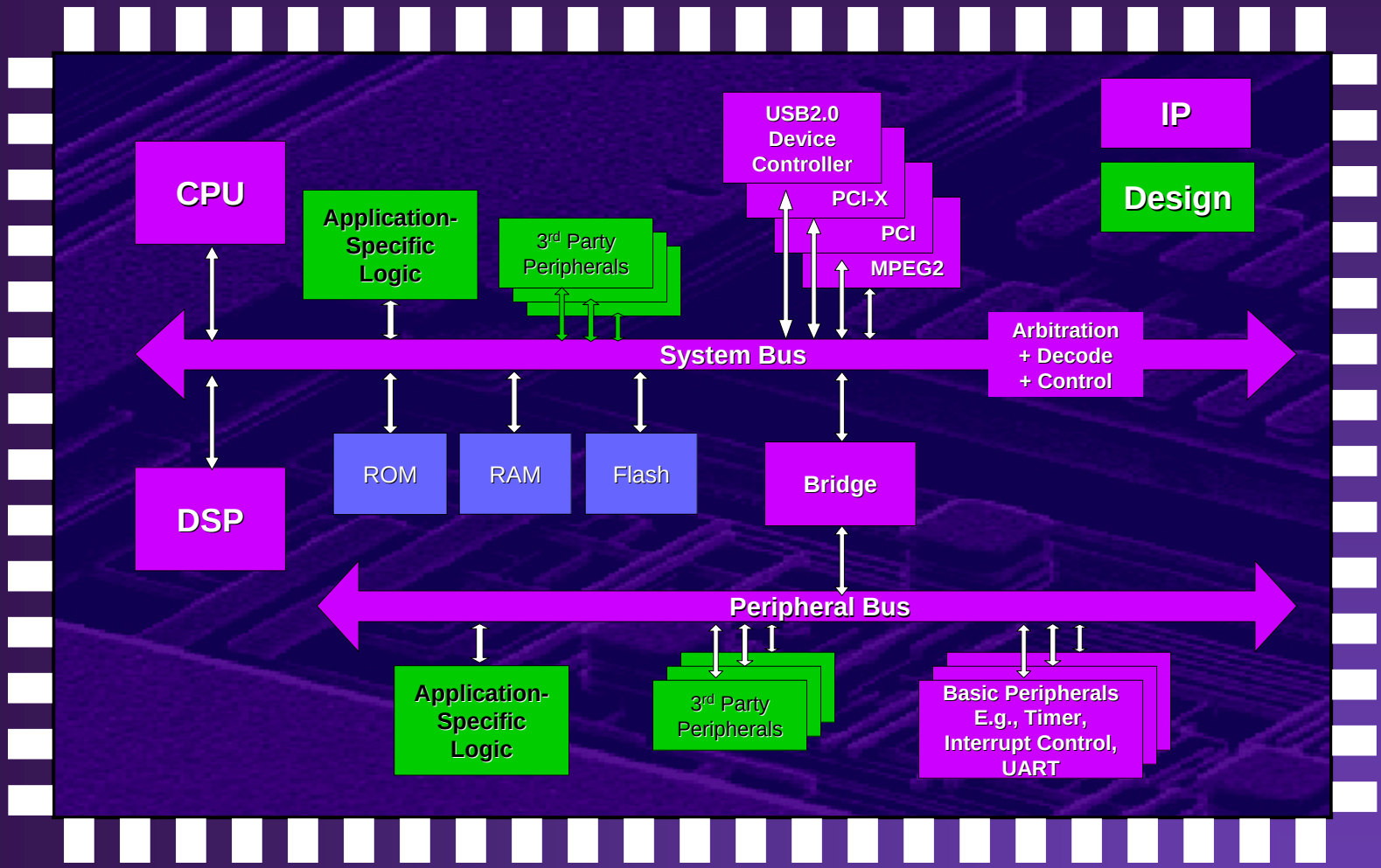
From IP to Platform-Based Design



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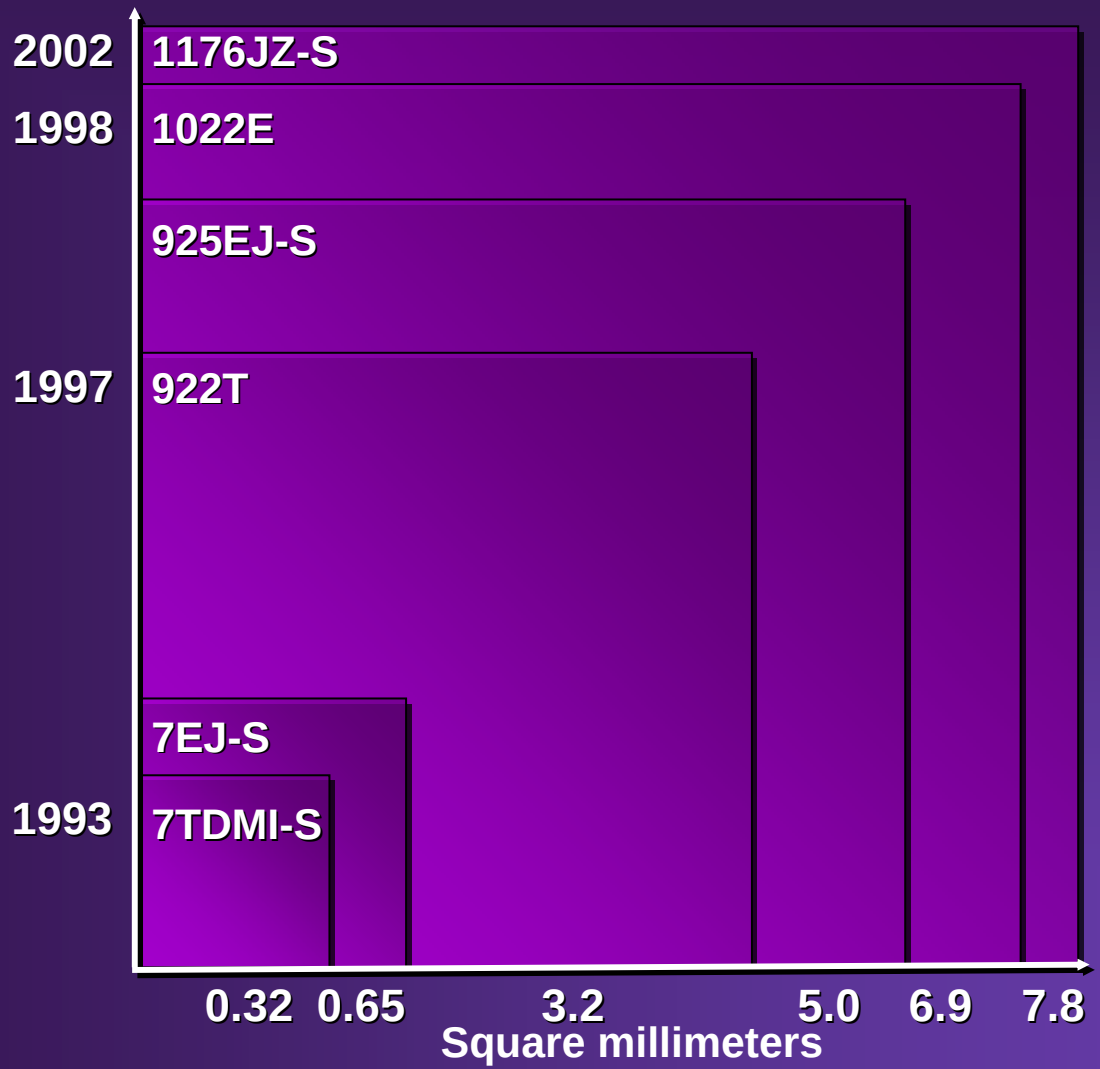
Increasing Size of Cores



Source: www.arm.com

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Future Trends

- IP reuse to increase to over 90% by 2010
- IP based design methodology
- IP diversity matters
  - It is kept in check by standards
  - Processors, memories and busses define platforms
  - IP needs to work together – platforms
- IP vendor size matters
  - IP needs to be certified by the vendor
  - The user certifies the vendor
  - Consolidation is unavoidable

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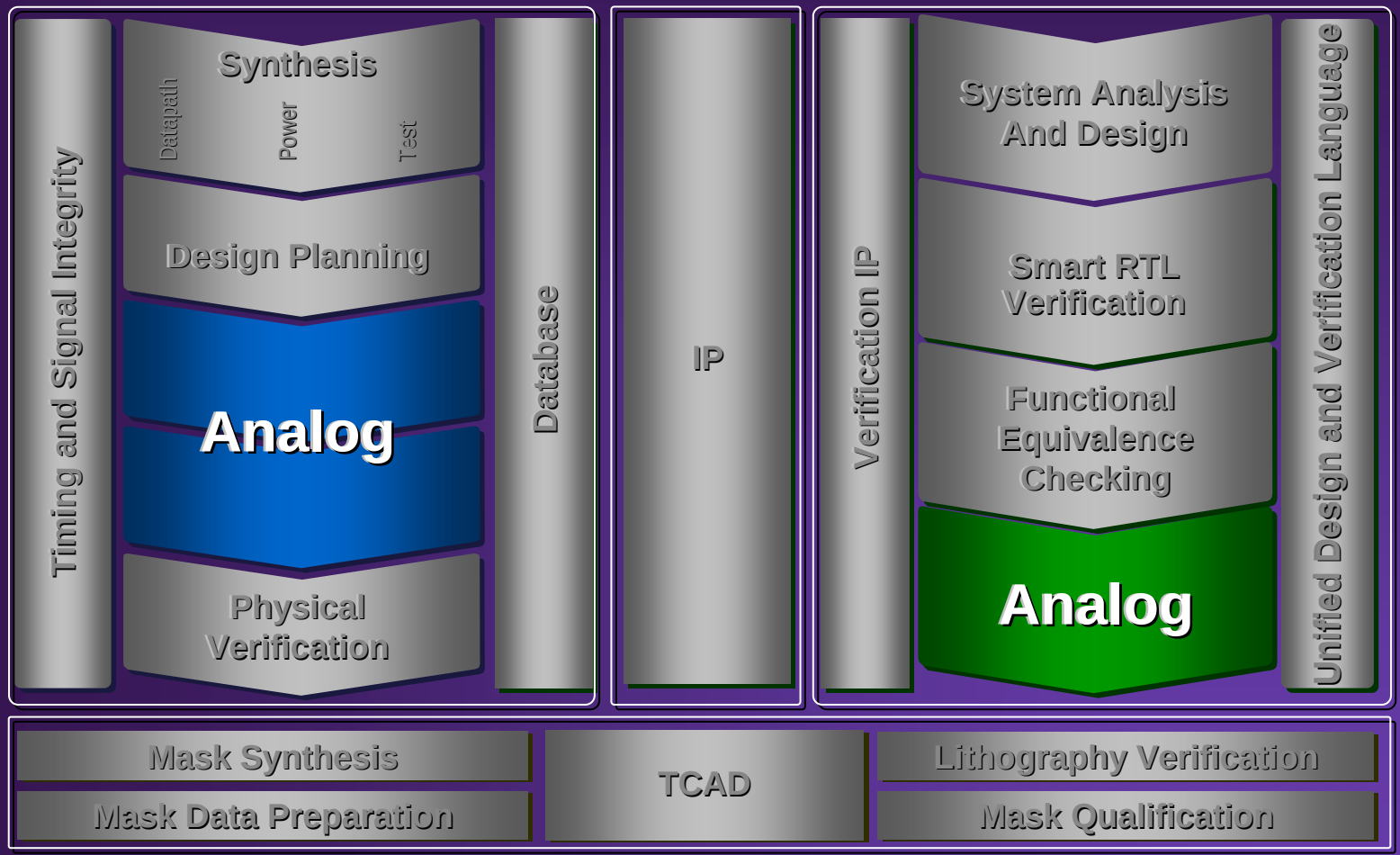
Analog Design Flow



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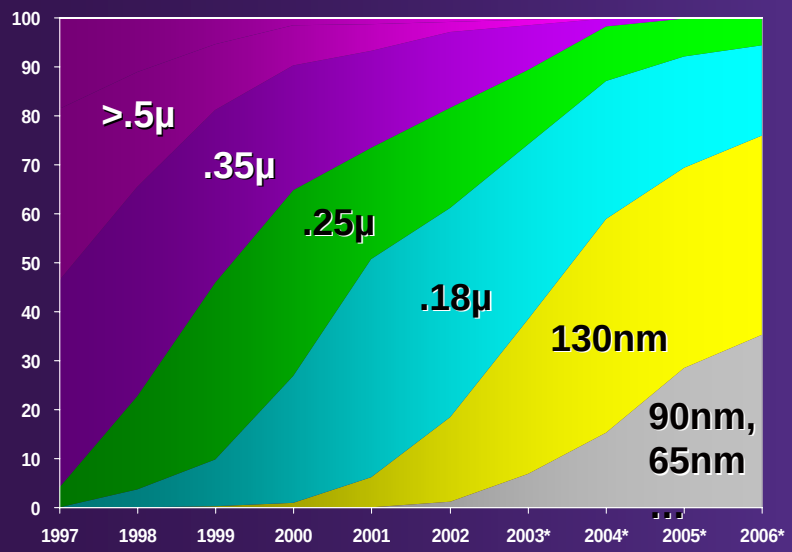
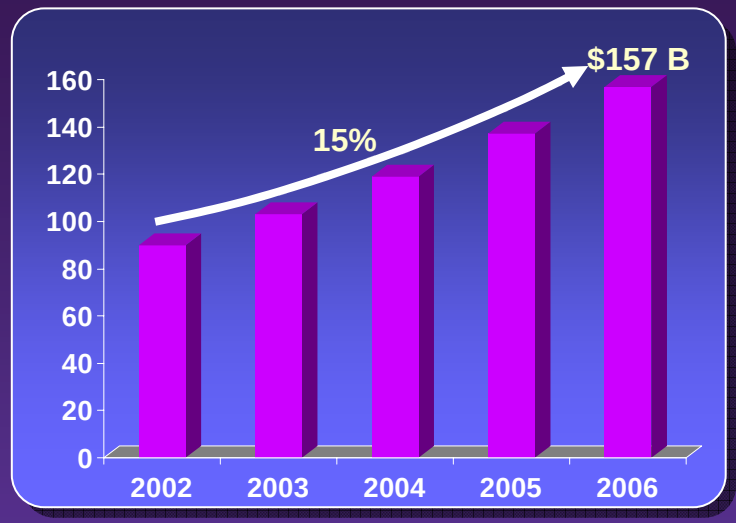
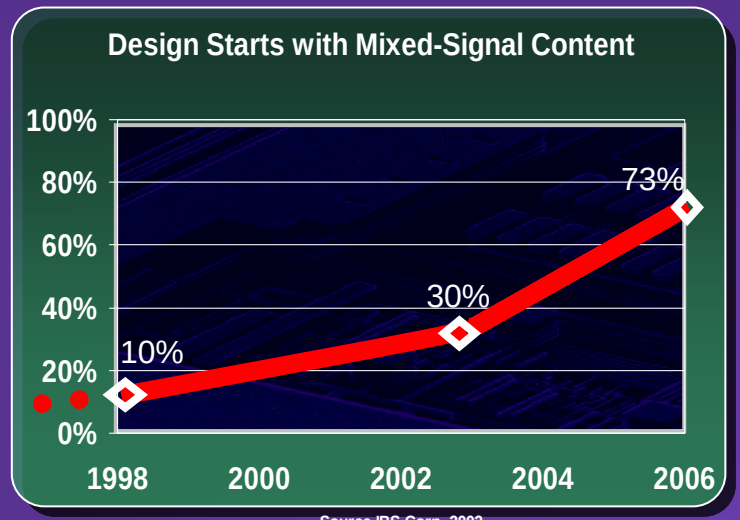
Mixed-Signal Design Trend

Fastest Growing IC Applications







Source IBS Corp. 2002

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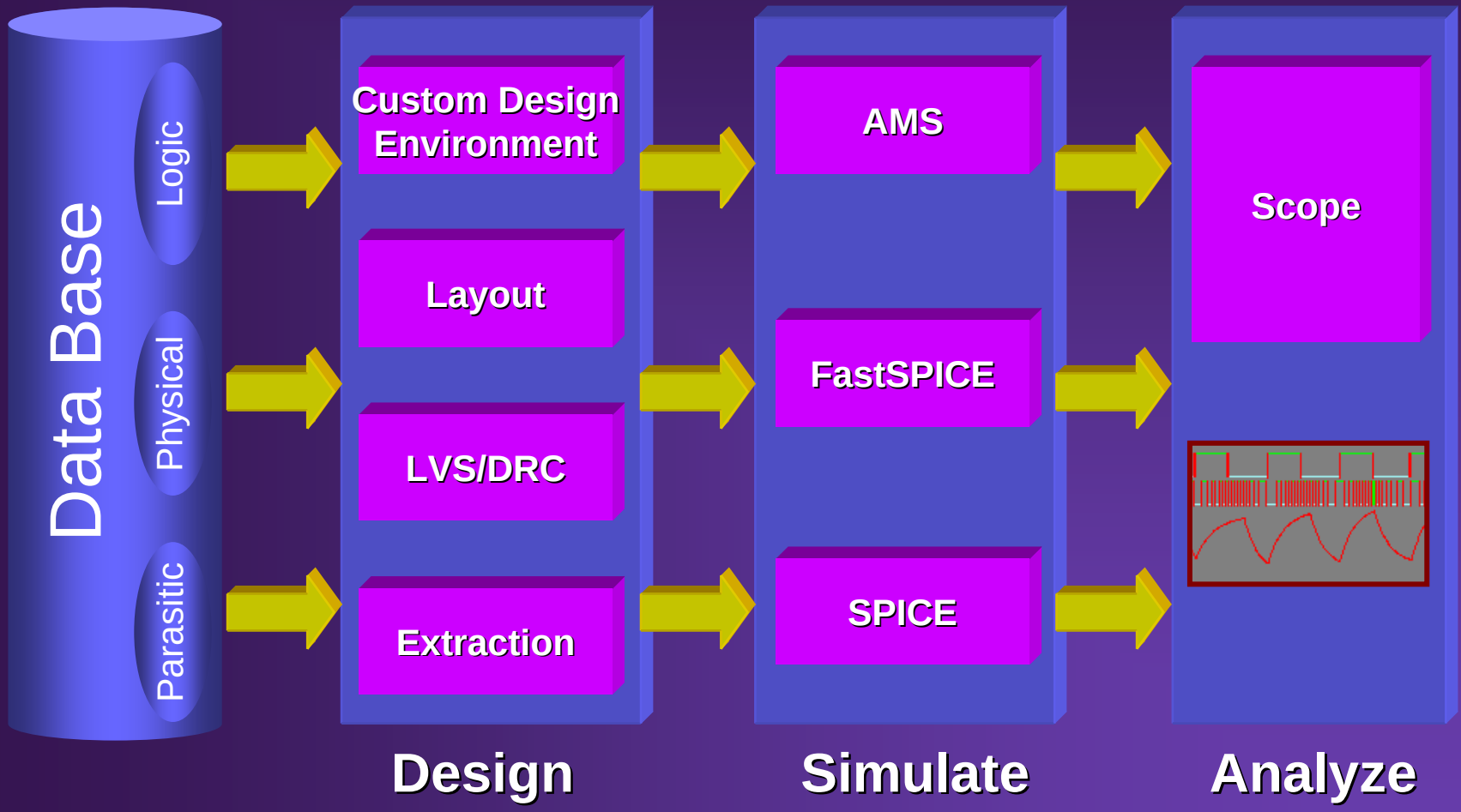
Integrated Custom & Mixed-Signal Analog Design Tools



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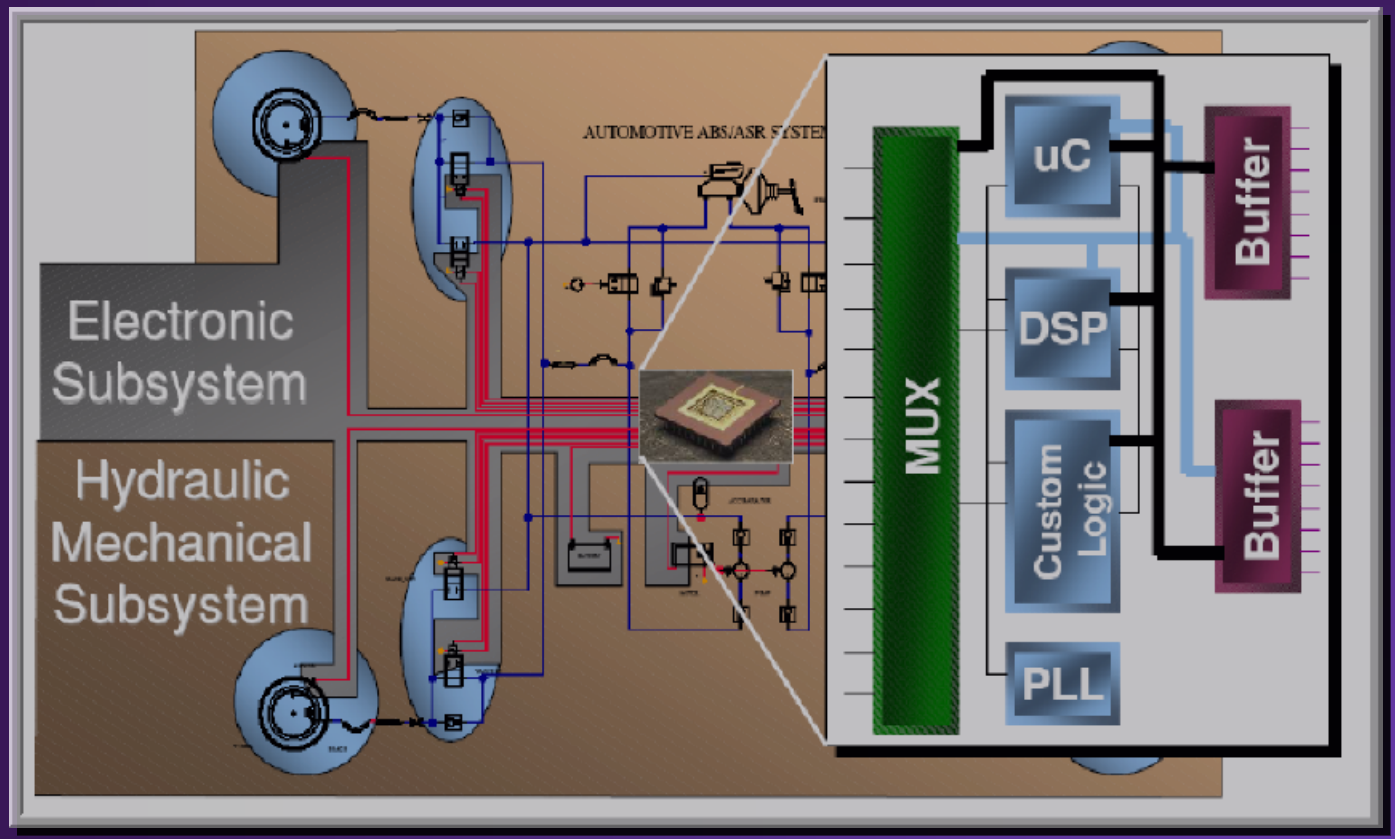
Example: Saber



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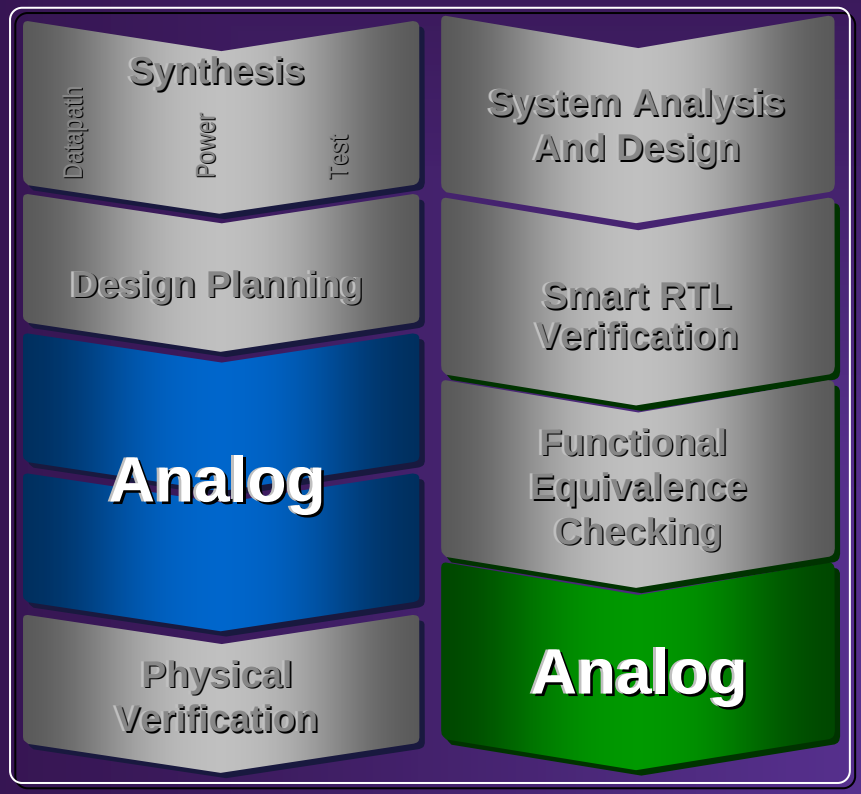
Future Trends



- More mixed signal design
- Includes also electromechanical, hydraulic, …
- More analog design automation
  - Sizing
  - Physical design

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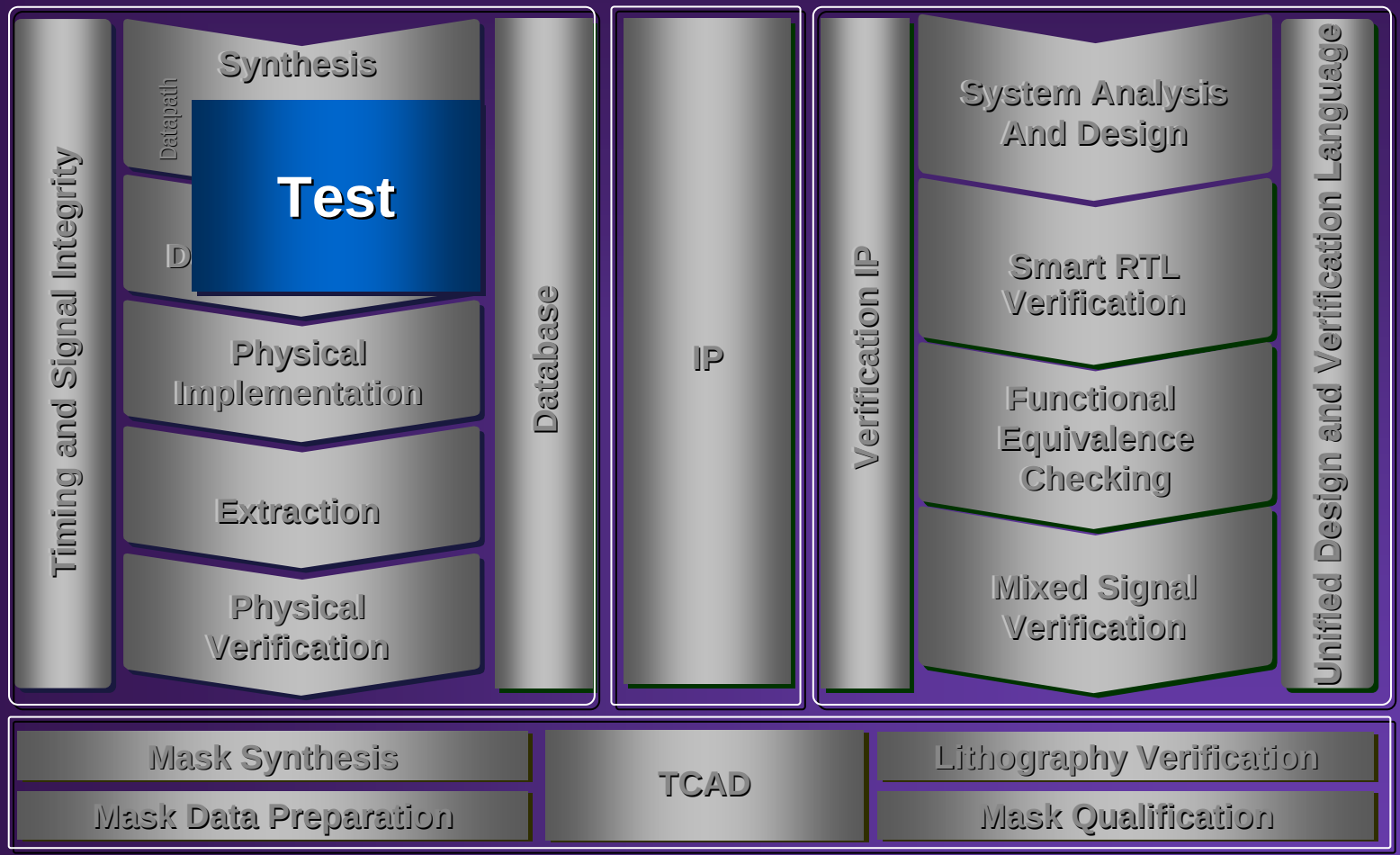
Built In Self Test (BIST)



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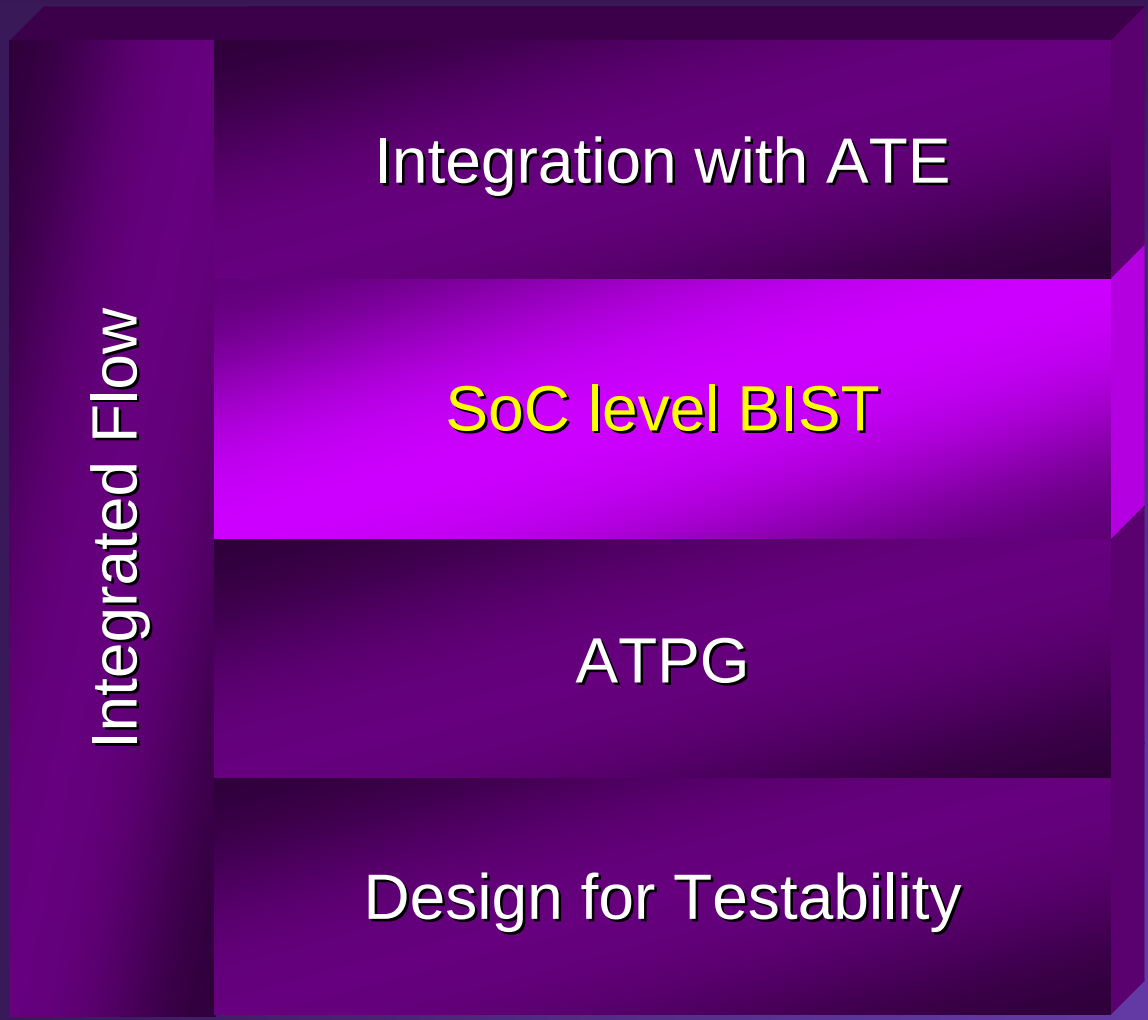
Design for Test



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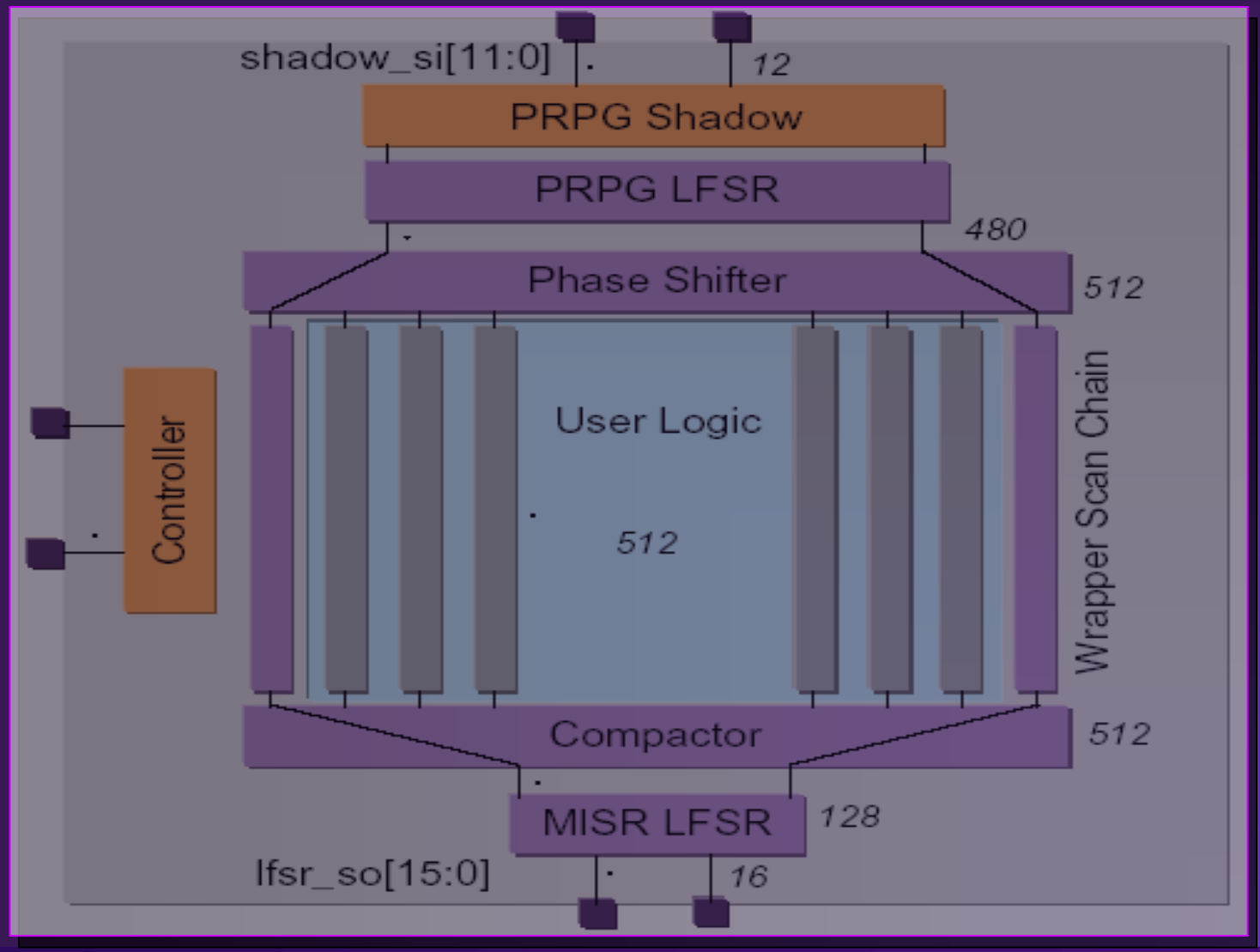
Synopsys SoCBIST Solution



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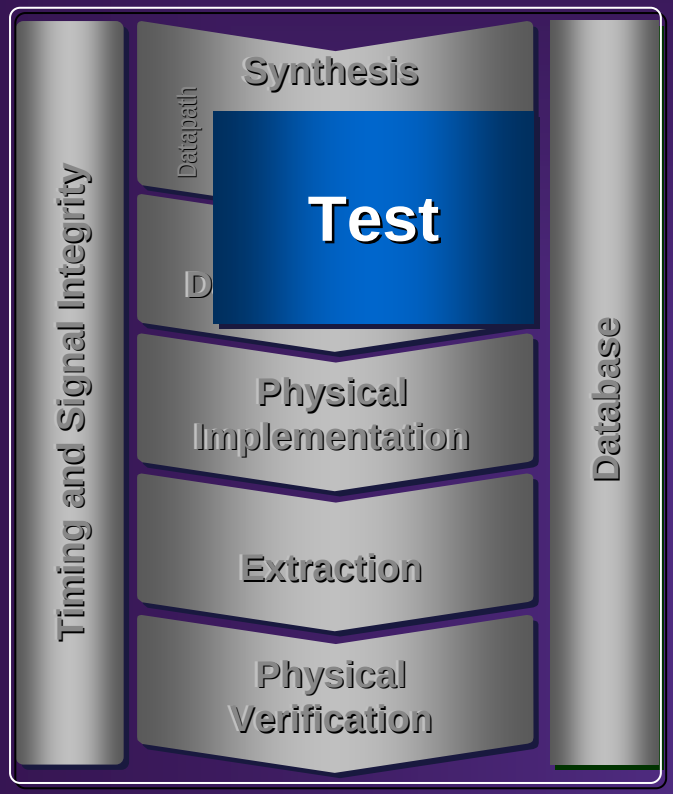
Future Trends



- Lower cost testers (structural test)
- Built-in self test
  - Memory
  - Logic
- Design for debug
- Fault tolerance

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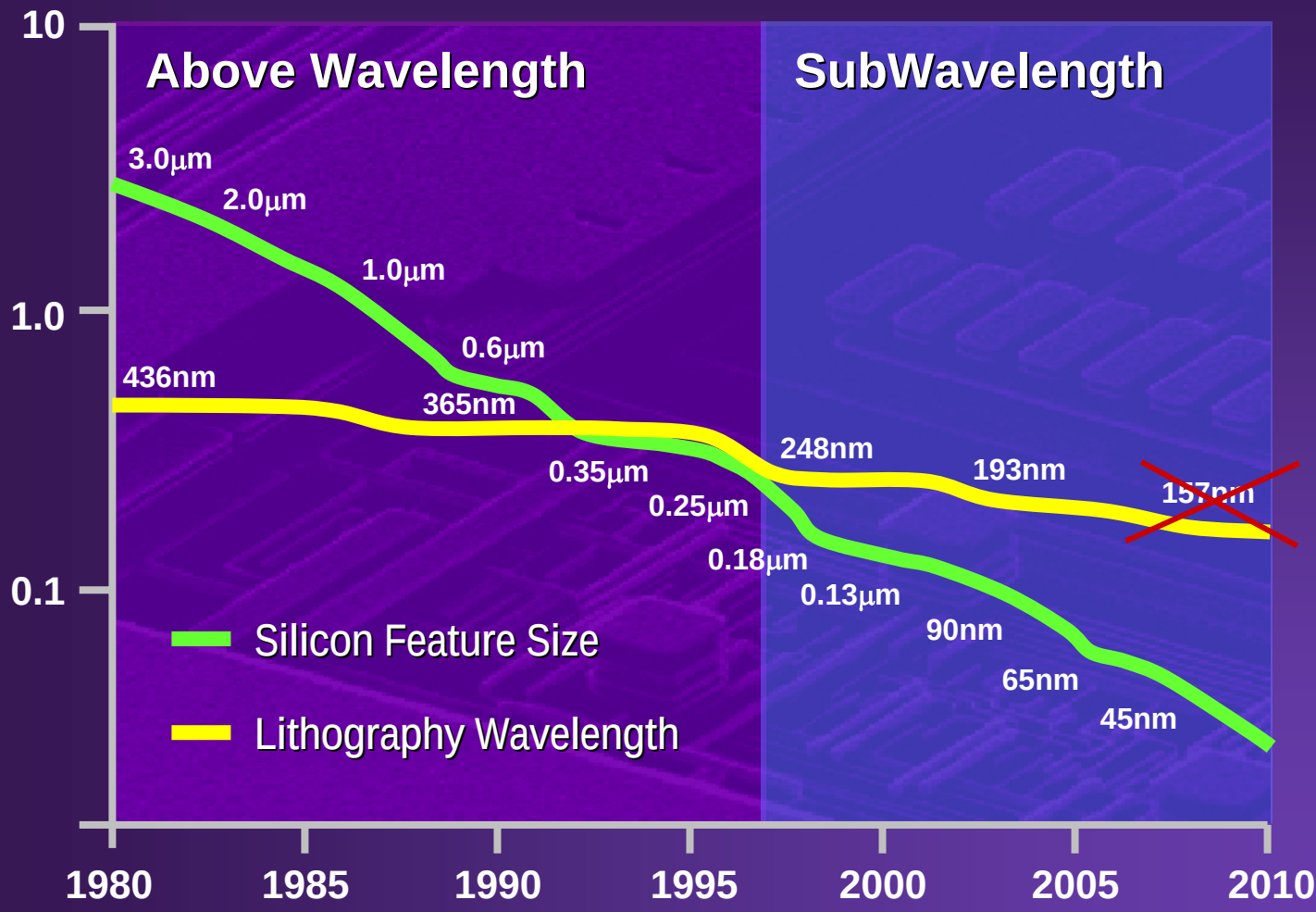
Subwavelength Lithography
Main Cause of Complexity



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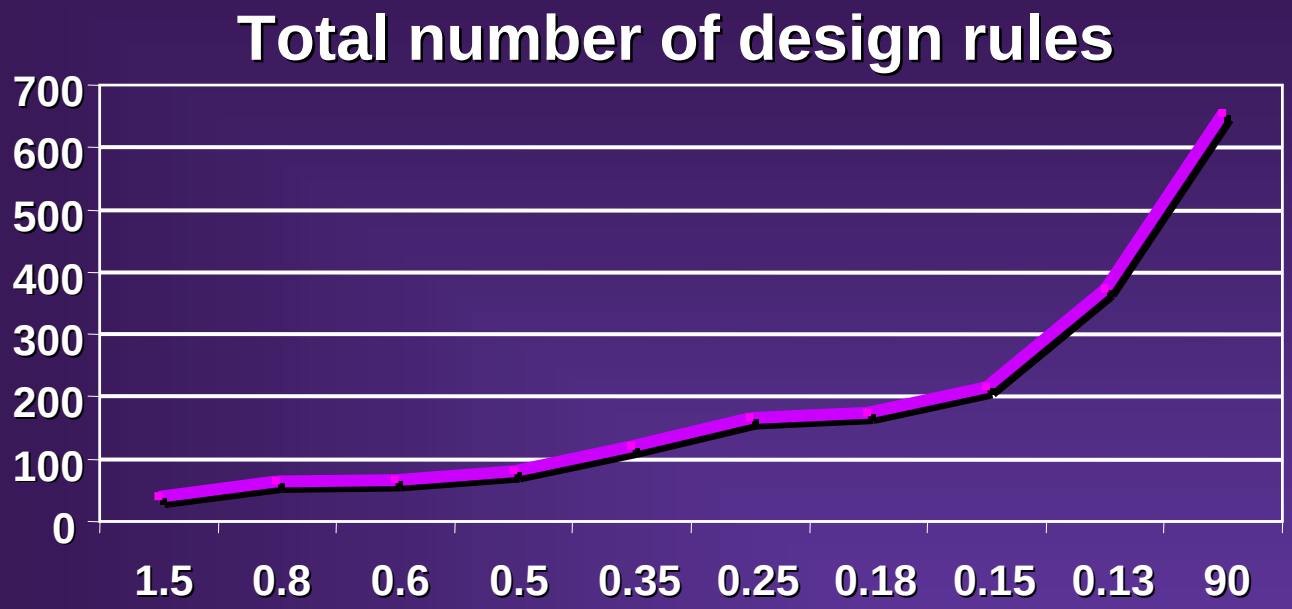
Subwavelength Design Rules



- OAI/OPC/PSM create extremely complex, context-dependent design rules
- Design Rule Paradigm may be breaking down

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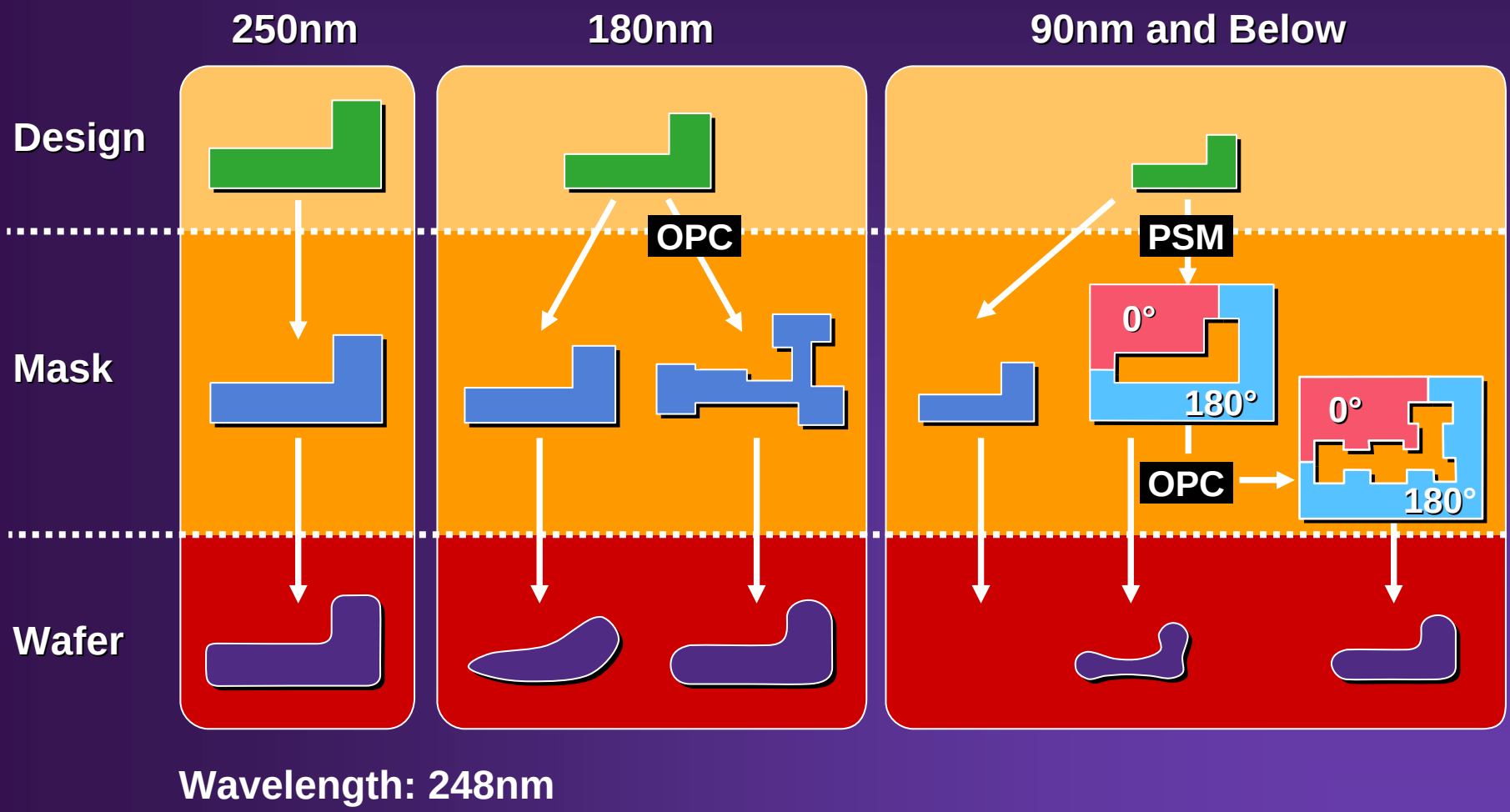
Mask Synthesis - RET

248nm Stepper



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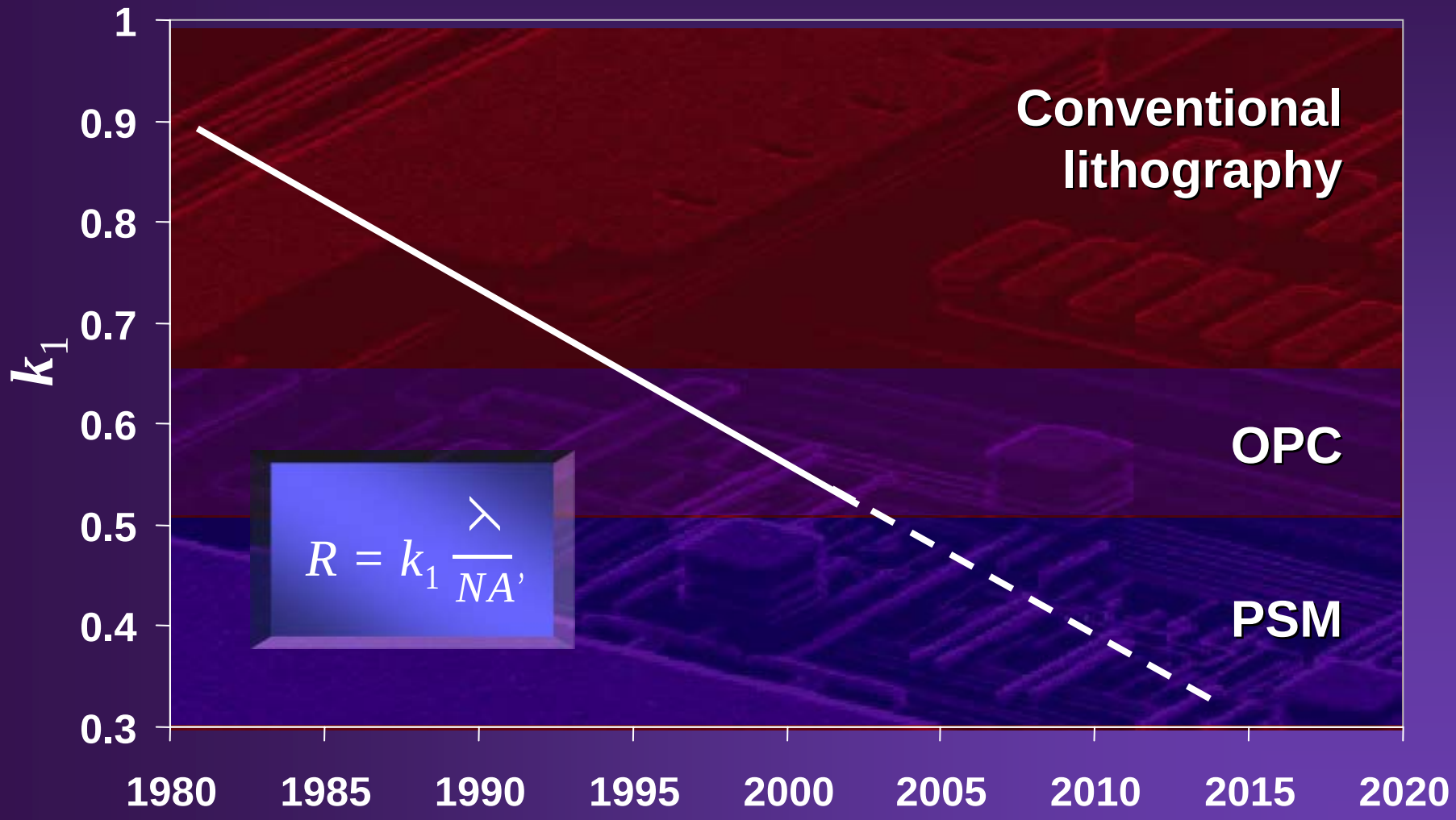
Evolution of RET



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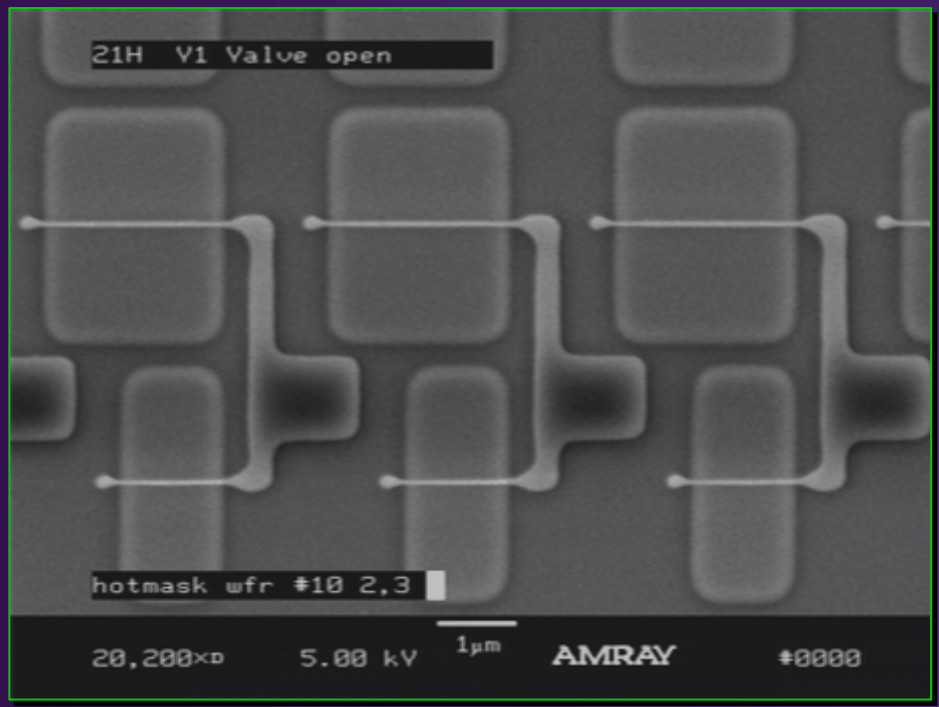
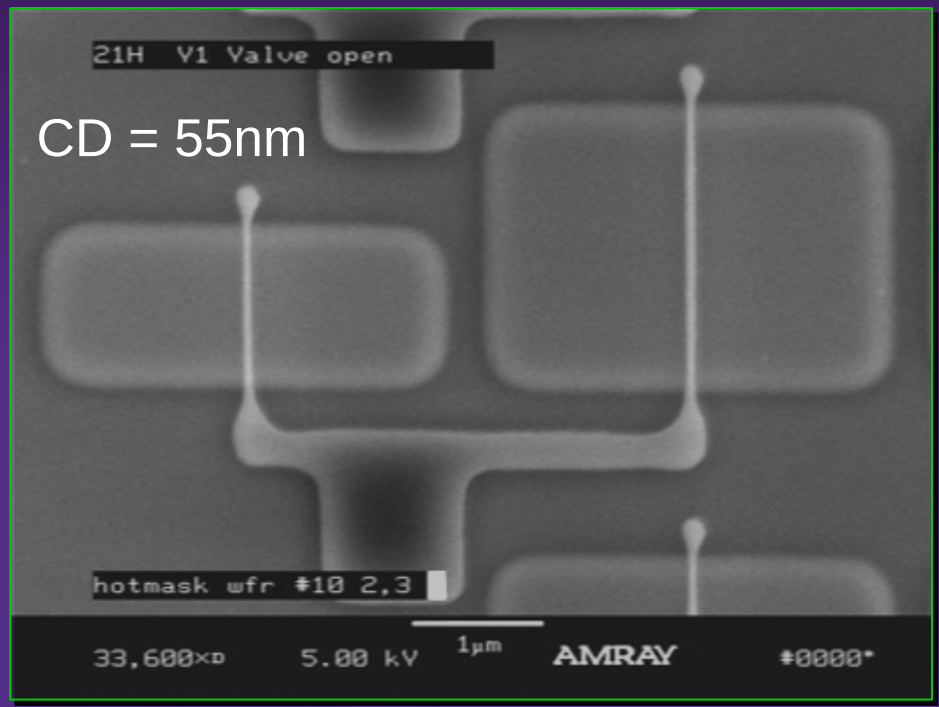
50nm Transistor Gates
Using Dark-Field Alternating Phase-Shift Mask (SNPS)





Resist on poly on patterned 600A islands
Canon EX-4 248 nm Stepper 0.6 NA 0.3 s
UV-5 on AR-3

Courtesy: Dr. M. Fritze
MIT Lincoln Laboratory

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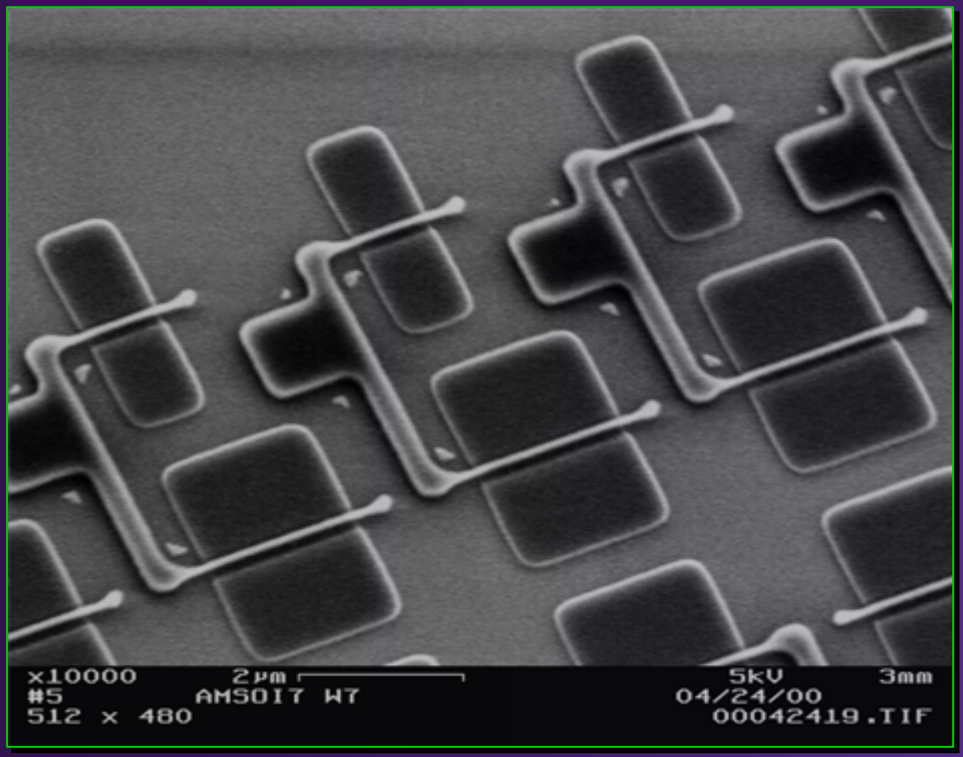
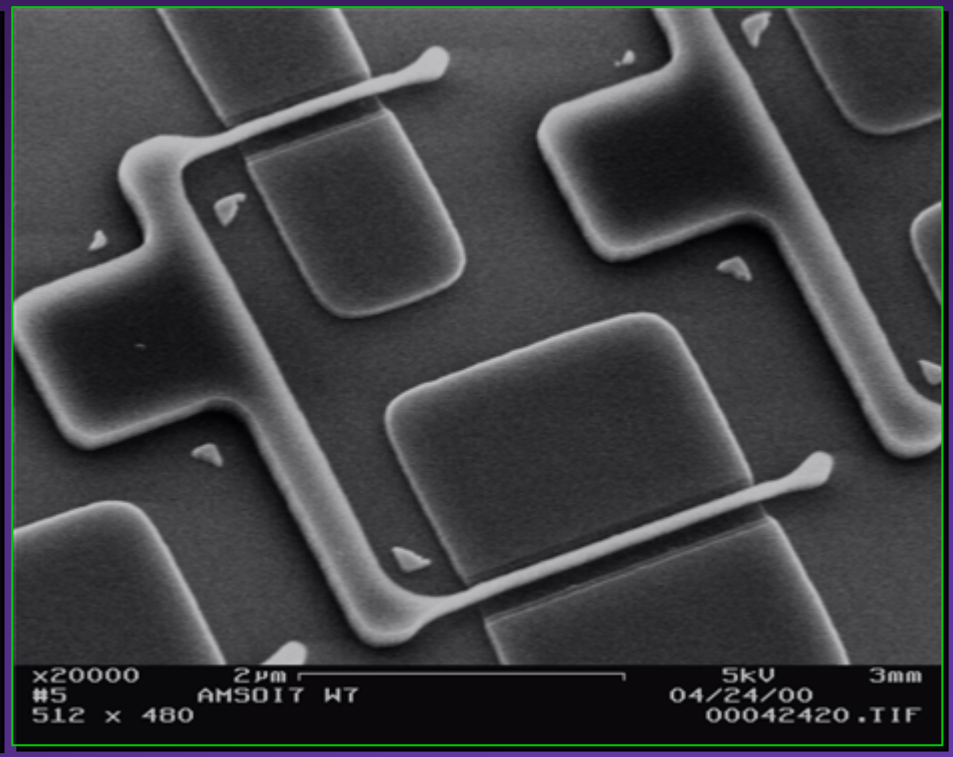
25 nm Transistors!





25-nm transistors produced with 248-nm lithography and AAPSM + OPC

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SEM Courtesy MIT Lincoln Laboratories

Timing

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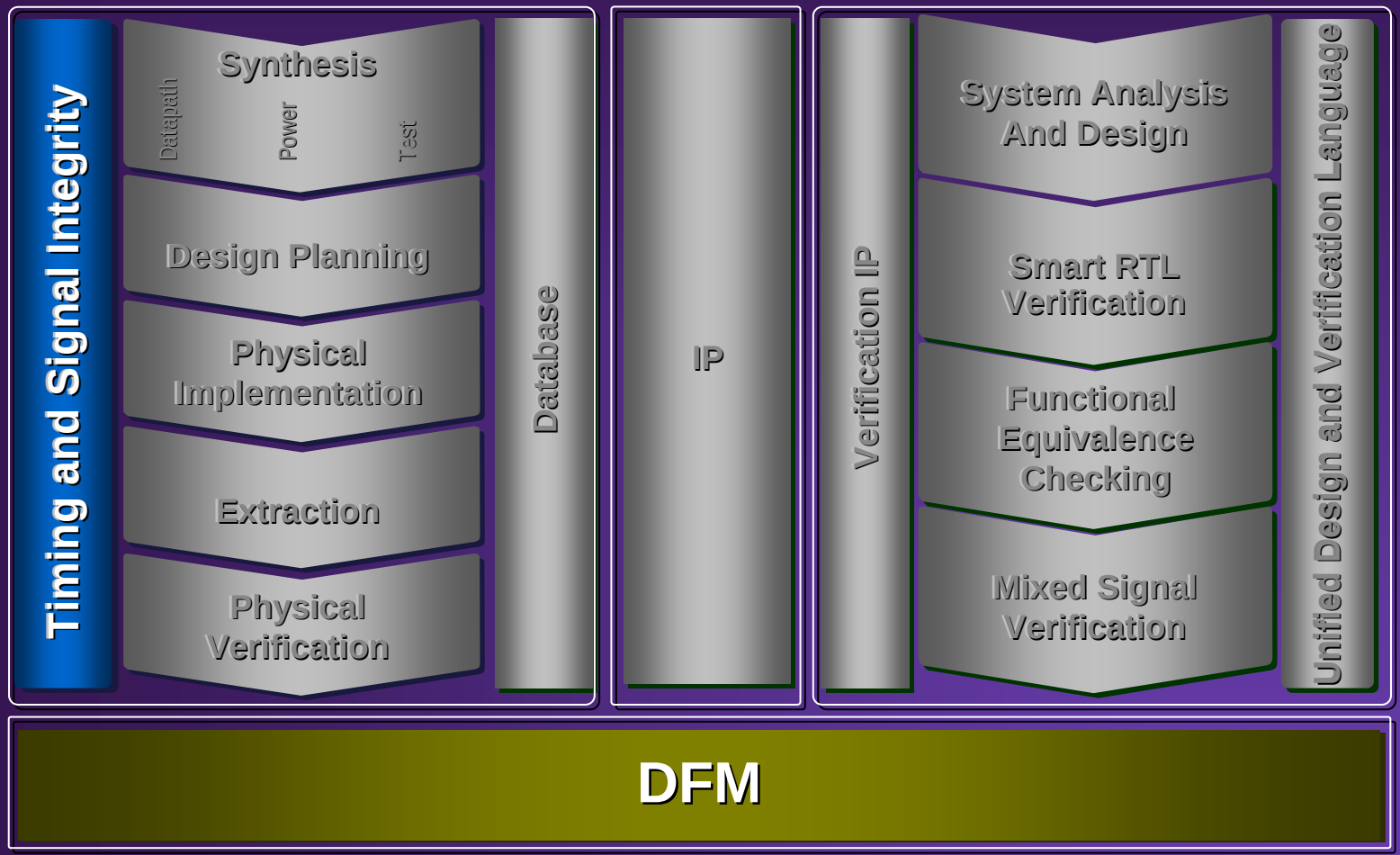
Timing In the Design Flow



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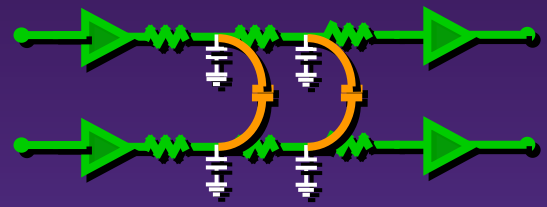
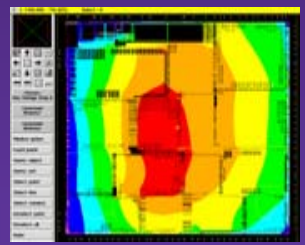
Shrinking Geometries Make Timing and Signal Integrity A Growing Problem

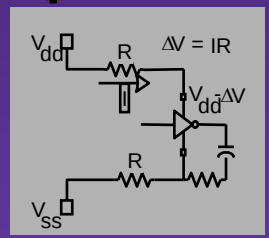
- Shrinking noise thresholds
- Increasing coupling capacitance
- Increasing current density
- Inductance
- More statistical variation

Crosstalk

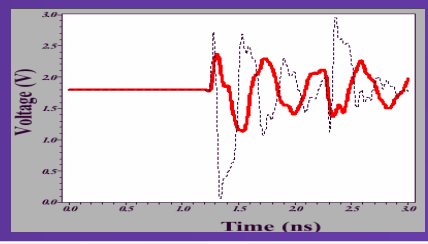


IR Drop





Inductance



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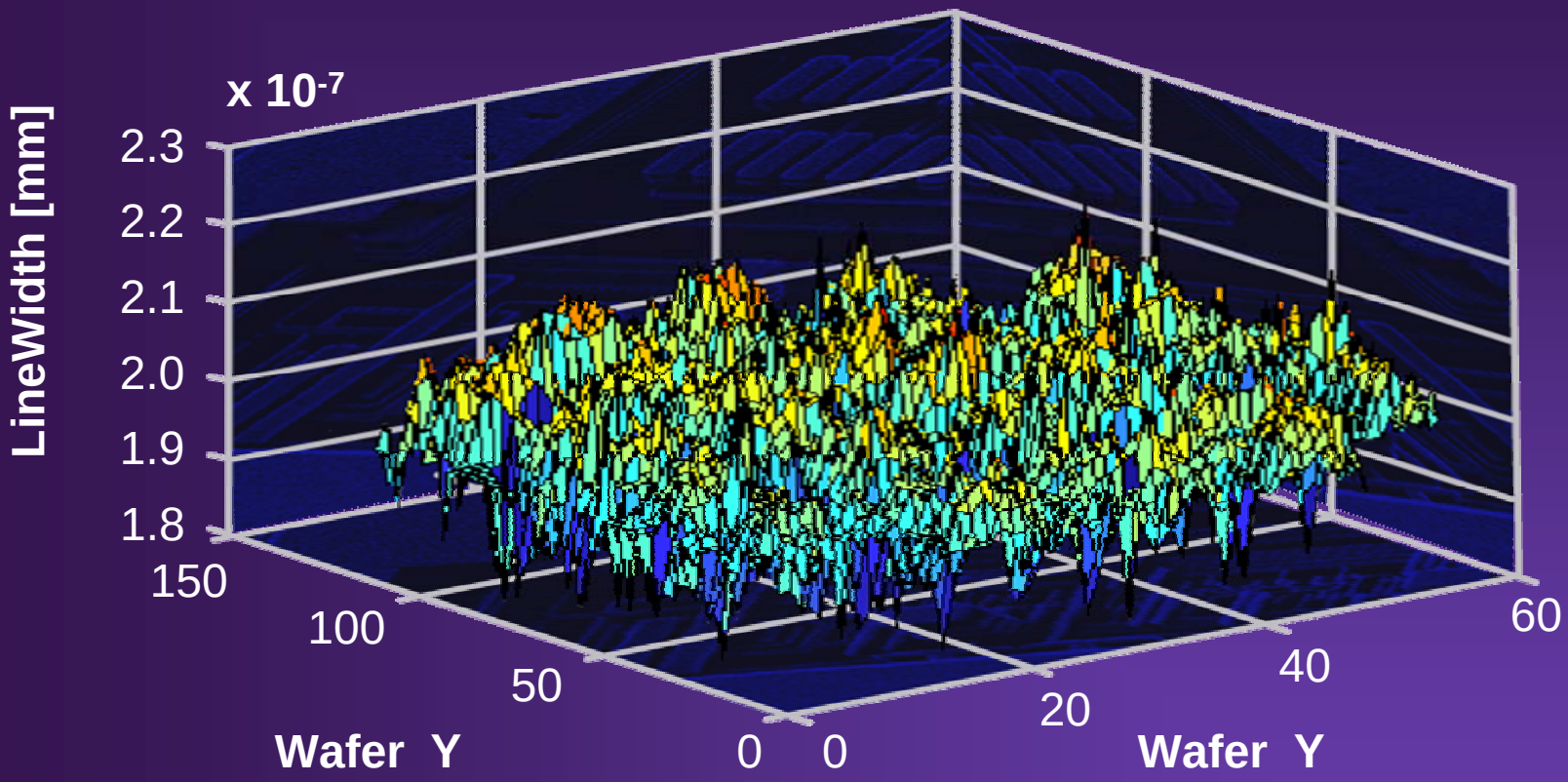
CD Variation Across a Wafer

Wafer Map for No-DPC Horizontal Isolated Structures



Incorporate analysis of timing variation into statistical timing analysis

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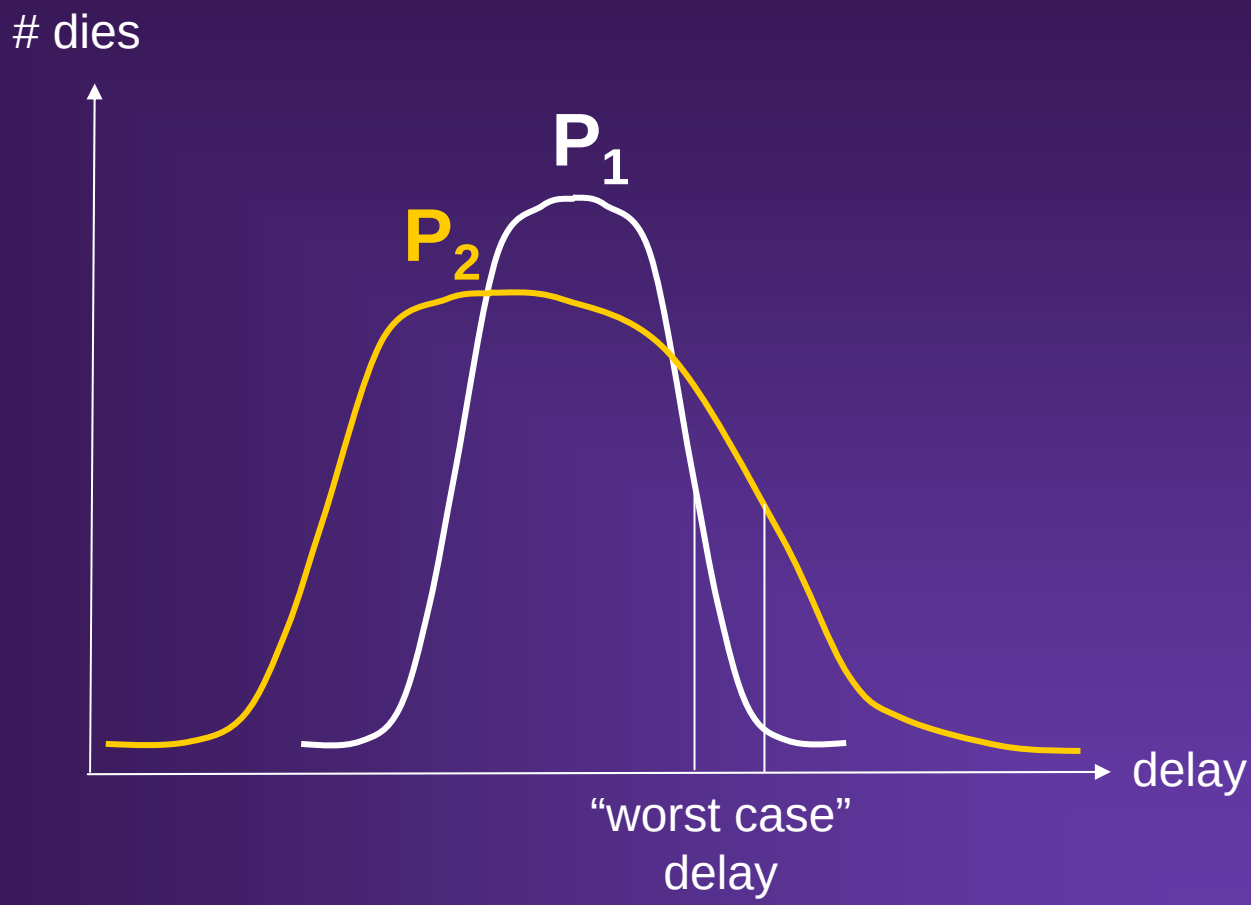
Variability



- **Requires statistical timing analysis?**

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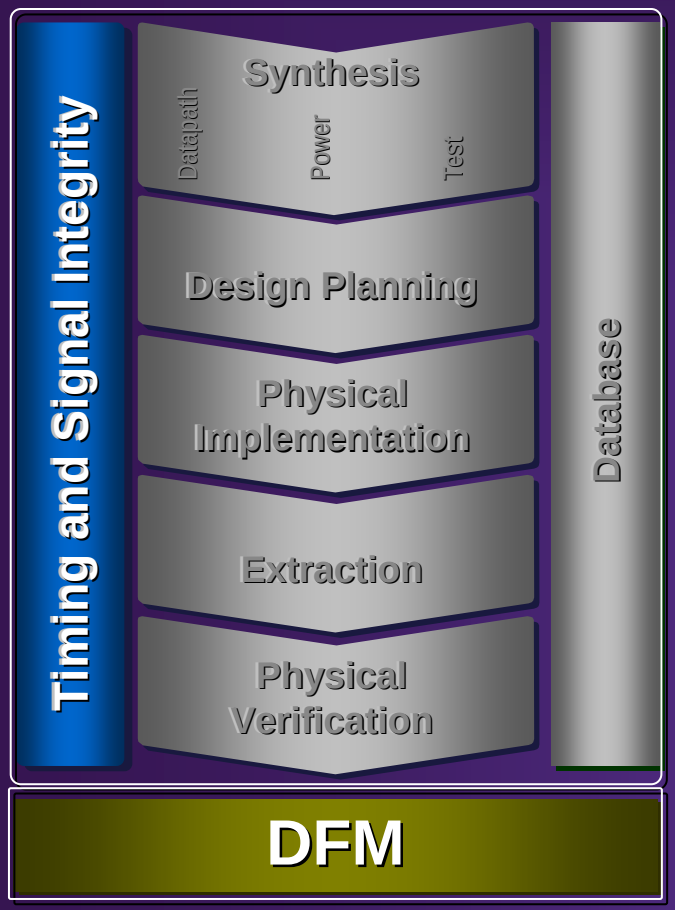
Future Trends



- Tools need to consider parasitics
  - Cross-coupled capacitance plus the Miller effect
  - IR drop (static leakage and dynamic IR drop)
  - Inductance
  - EM
- CD variation requires statistical analysis

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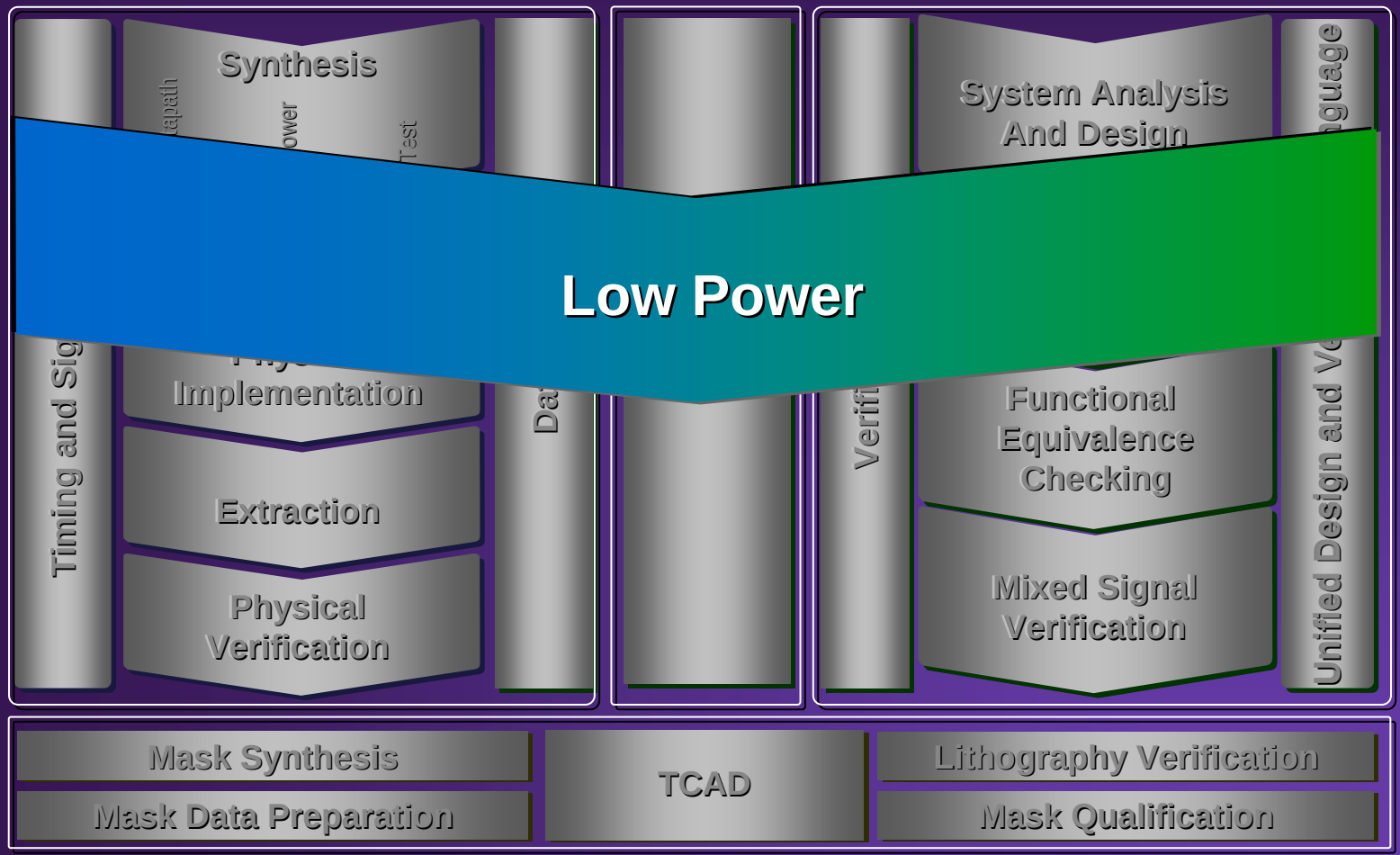
Low Power Design Flow



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Power

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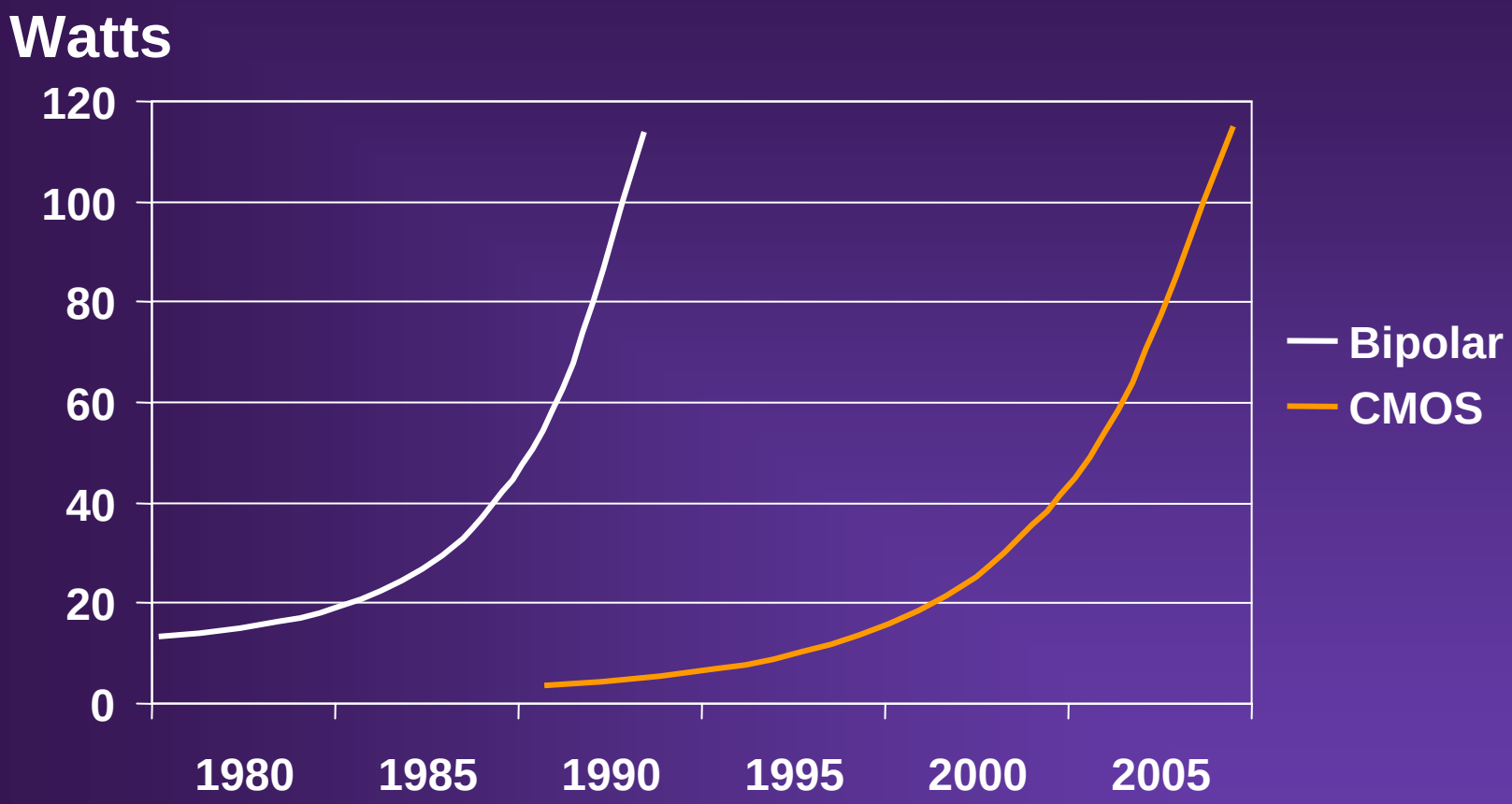
Power Consumption



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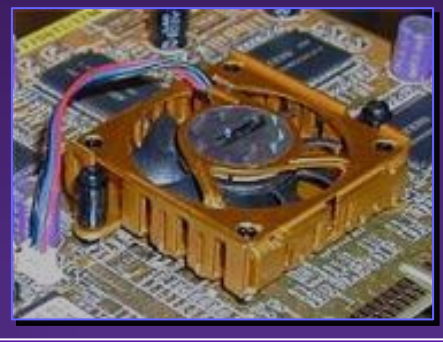
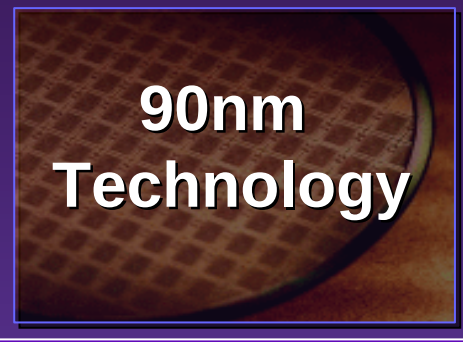
Key Power Management Areas

	Low Power	Thermal Management	Physics
			
Application	• Wireless • Handheld • Embedded systems	• Microprocessors • Graphics/multimedia • Networking/telecom	• Every design @ 90nm
Concern	• Battery life • Lowest leakage &/or dynamic power	• Thermal management • Packaging, cooling cost	• Leakage power • IR-drop • Electro-migration

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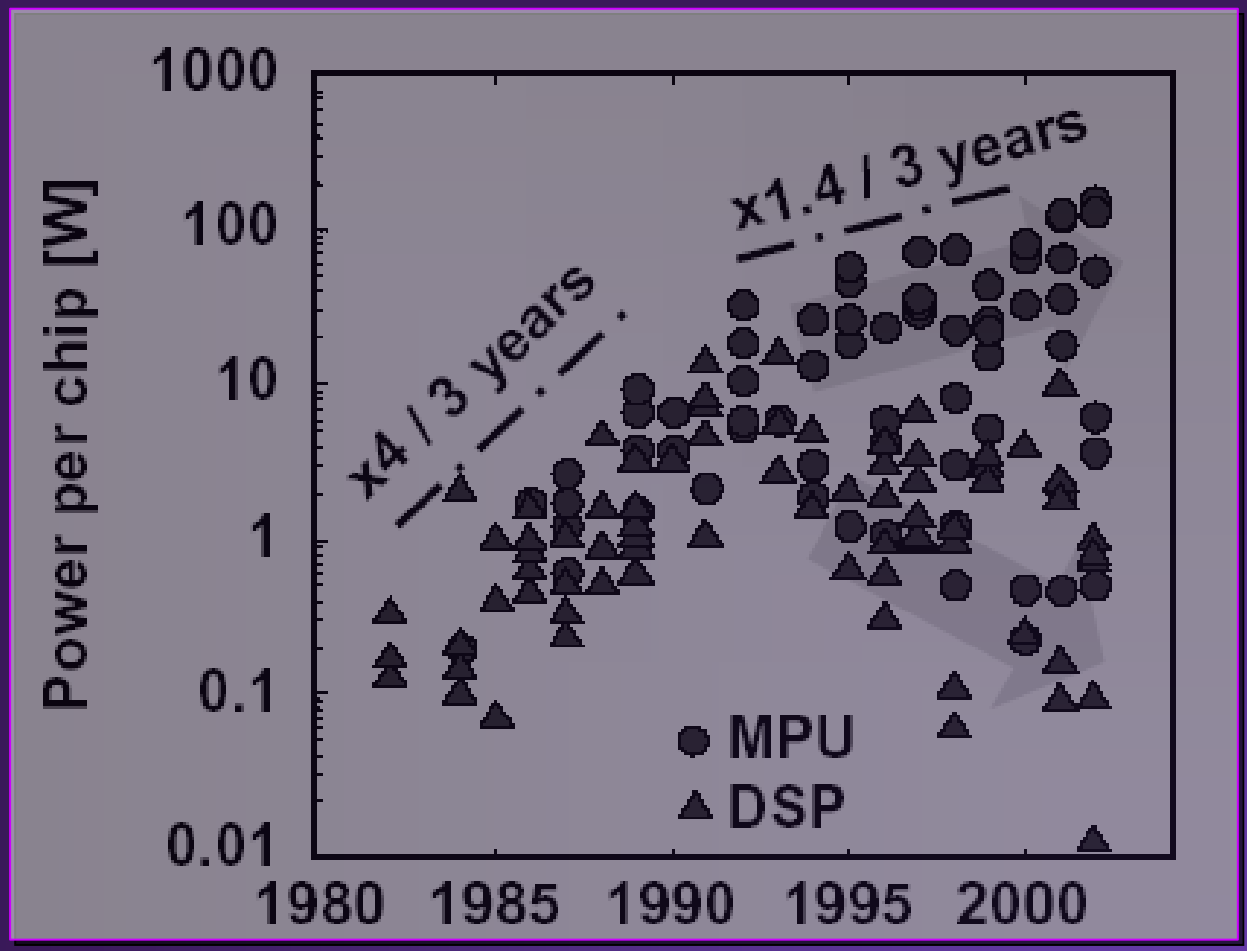
Hottest Chips in ISSCC



T. Kuroda, Keio Univ.

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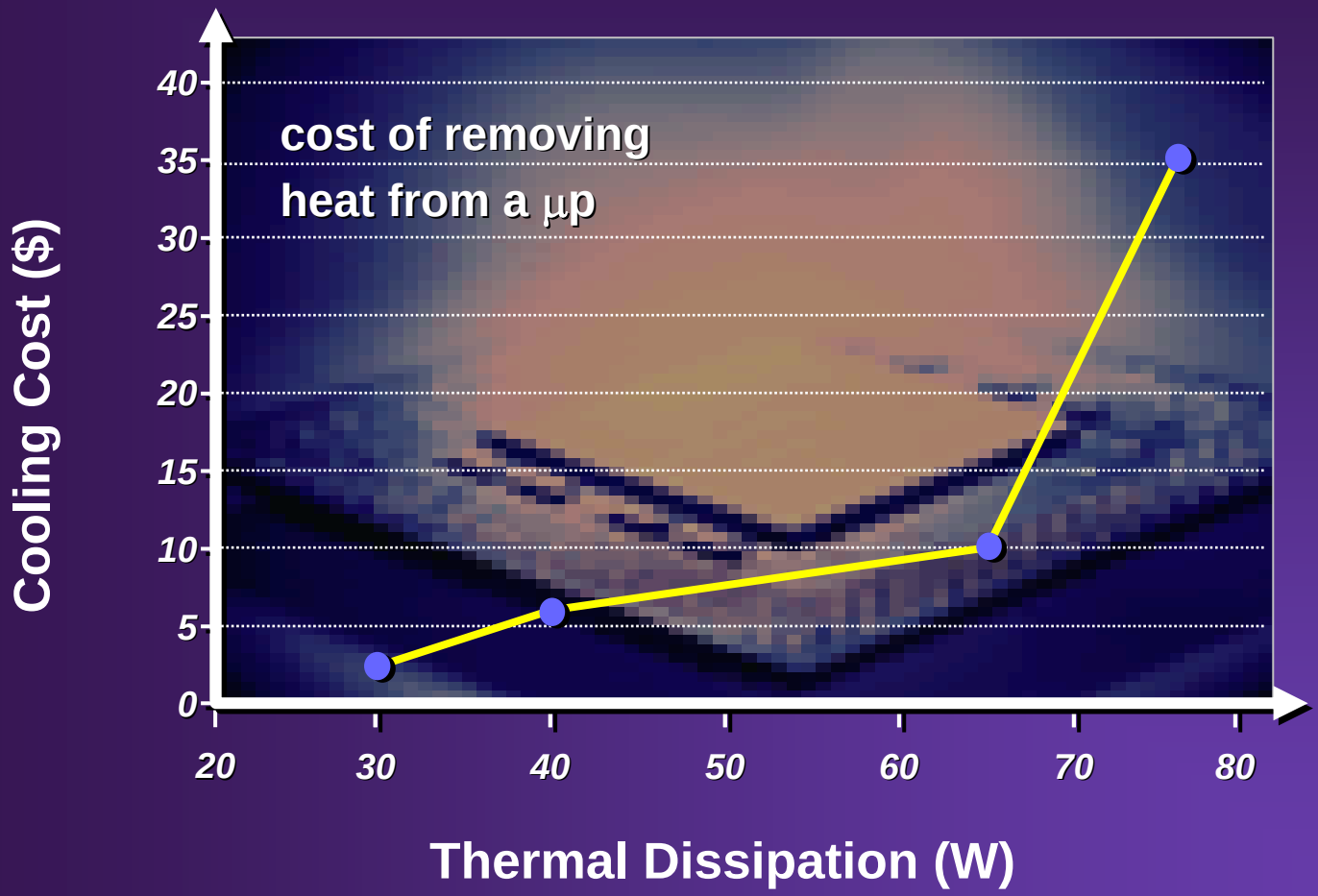
The Rising Cost Of Power



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Source: Intel Technology Journal, 1st Quarter 2001

The Power-Saving Spectrum

- *Multi--V_{th}*
- SOI
- Materials
- Multi-gate (FinFet)

- *Low-power circuits*
- *Operand isolation*
- *Clock-gating*
- *Voltage scaling*
- *Asynchronous design*
- Power-gating
- Body bias
- Stacked transistors

- Algorithm trans.
- Parallelism
- Memory architecture
- Cache partitioning
- Thermal monitor

- Power aware OS
- Compilers
- Memory access

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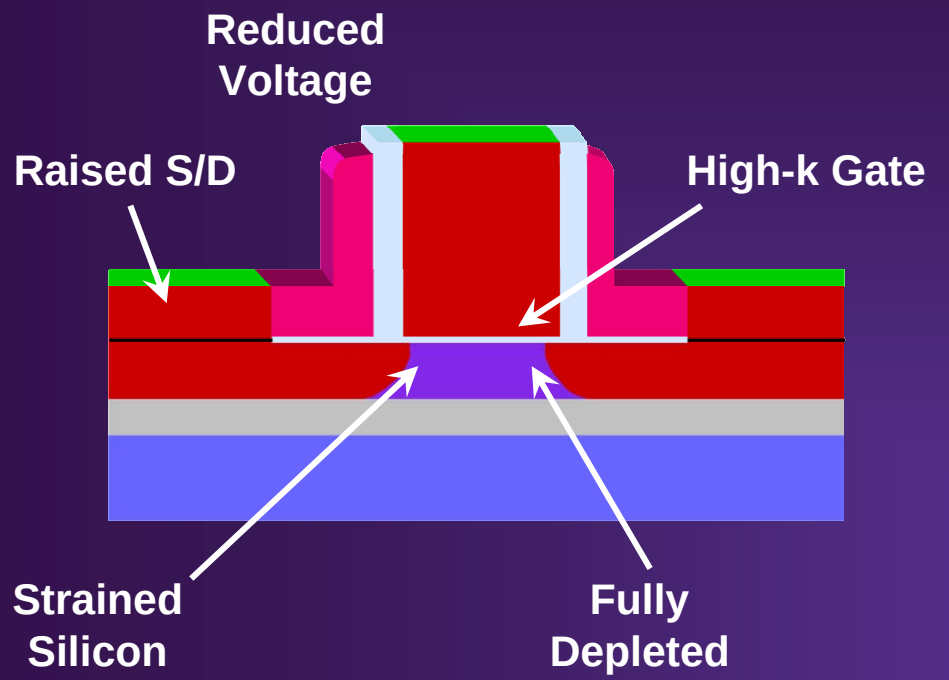
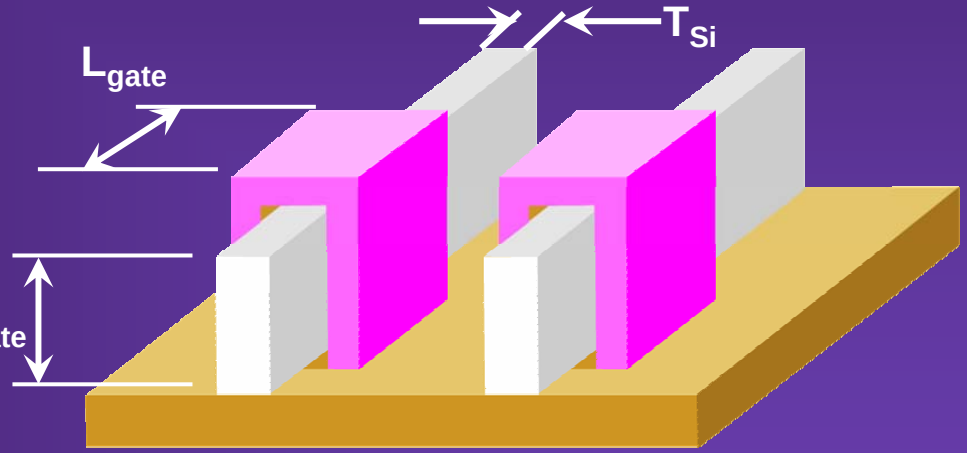
Devices for High Speed / Low Power



Fin height = 1/2 W_{gate}



I α 2 Fin height / L_{gate} x N_{fin}

Vertical dimension not litho limited

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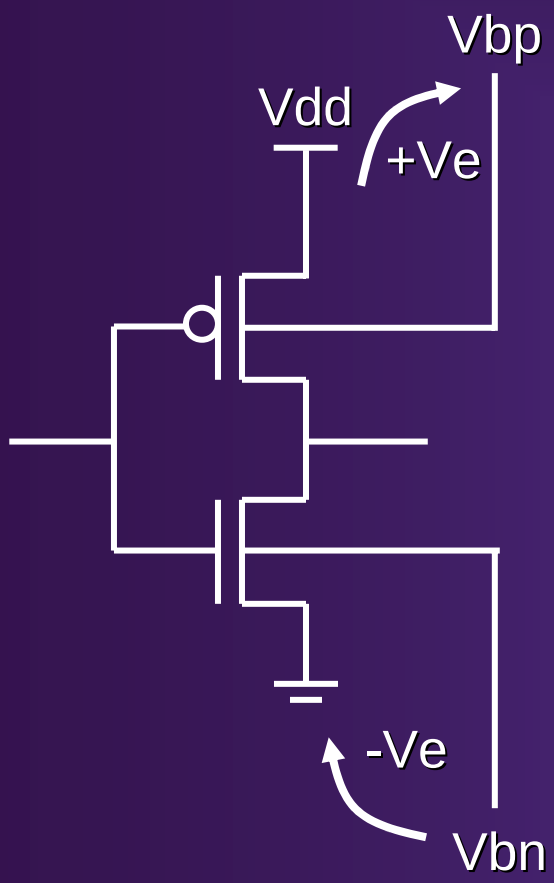
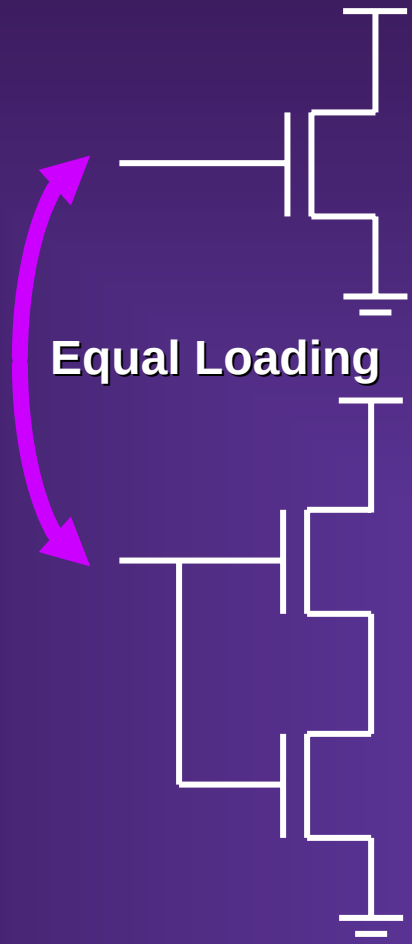
Leakage Power Circuit Techniques

Body Bias

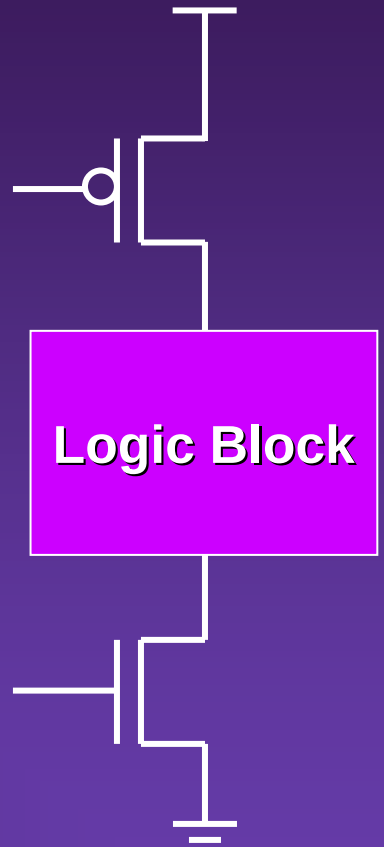


2-10X Reduction

Stacked Transistors



Sleep Transistor



2-1000X Reduction

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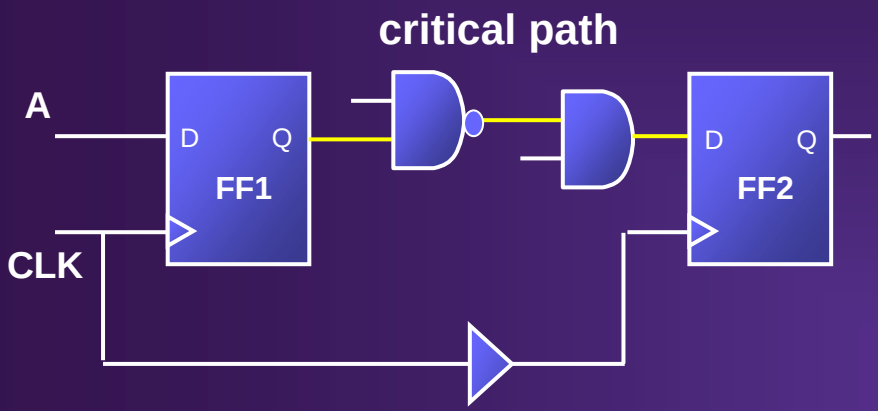
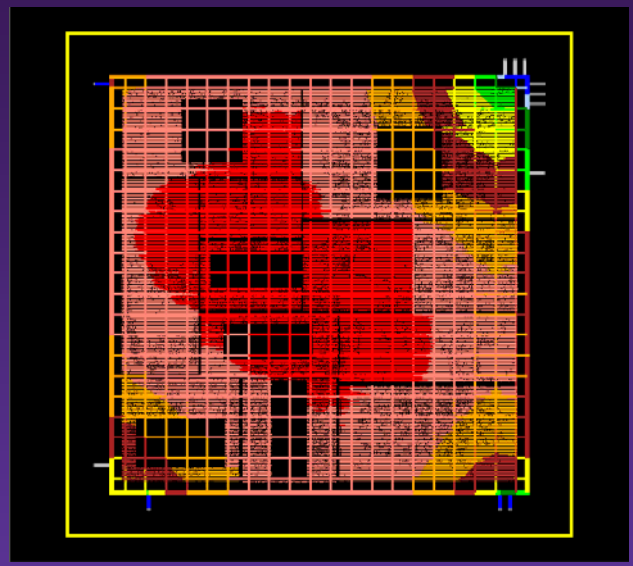
Source: Intel

Timing vs. Power





Trading

- **Old days: delay for area**
- **Now: power for delay**

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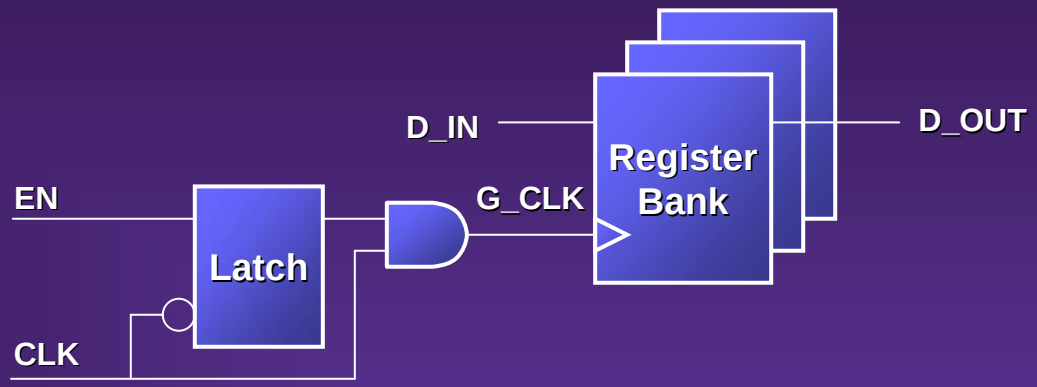
RTL Clock-gating

```
always @ (posedge CLK)
    if (EN)
        D_OUT = D_IN
```



Design	Size	Power Savings
RISC Core	220K	52%
LCD Display Block	400K	35%
Adaptive Computing	1200K	61%

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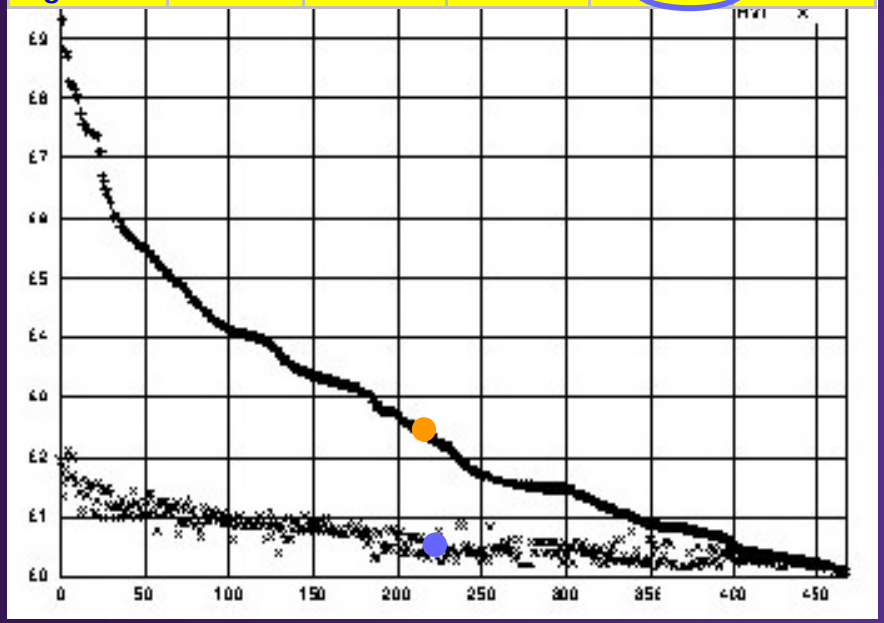
Dual-V_{th}

Decreasing Threshold Voltage Increases Leakage!

180nm Dual-V_{th}

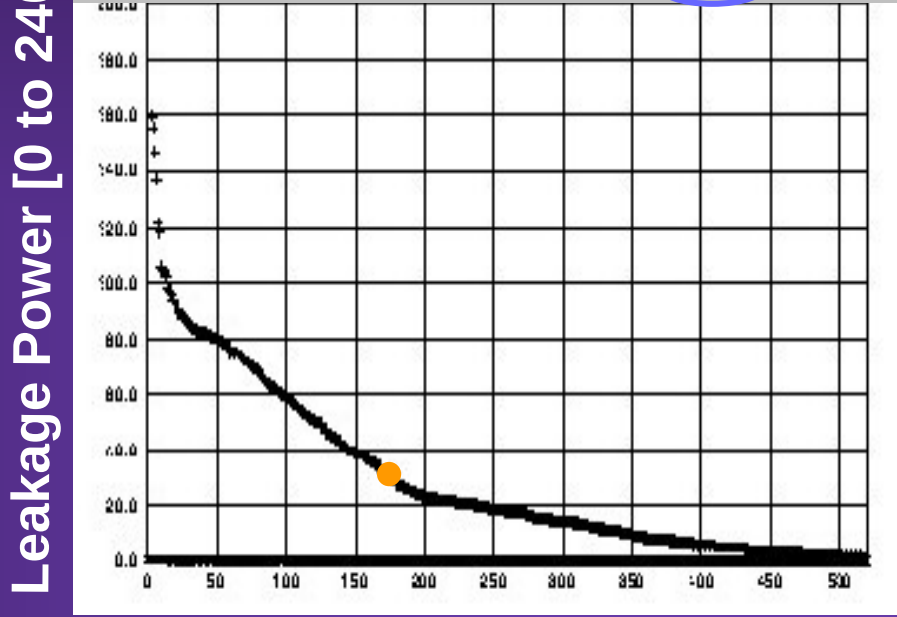
	Vdd (V)	Delay (ps)	Leakage Power Min (nW)	Leakage Power Aver (nW)	Leakage Power Max (nW)
Low Vth +	1.8	28	0.011	0.263	0.955
High Vth x	1.8	36	0.007	0.068	0.280



180nm Standard Cell Library

130nm Dual-V_{th}

	Vdd (V)	Delay (ps)	Leakage Power Min (nW)	Leakage Power Aver (nW)	Leakage Power Max (nW)
Low Vth +	1.2	10	1.135	30.779	233.395
High Vth x	1.2	16	0.002	0.043	0.580



130nm Standard Cell Library

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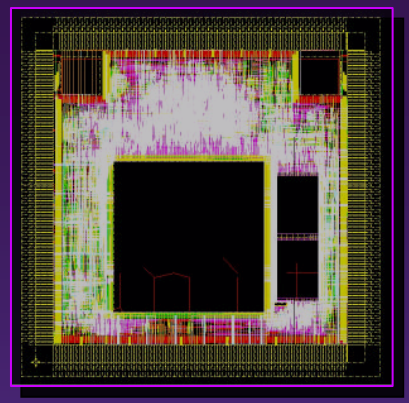
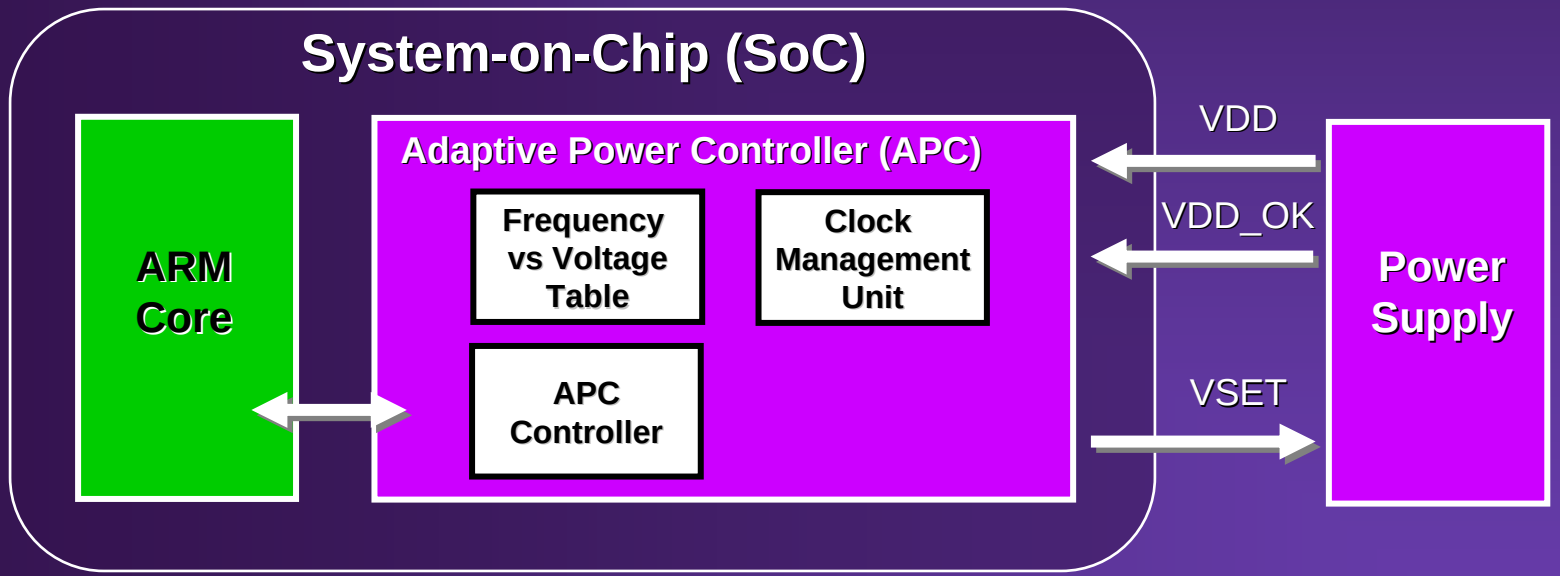
DVS Implementation



ARM926-DVS

Taped-out April '03



VDD_OK indicates when it is safe to update the clock

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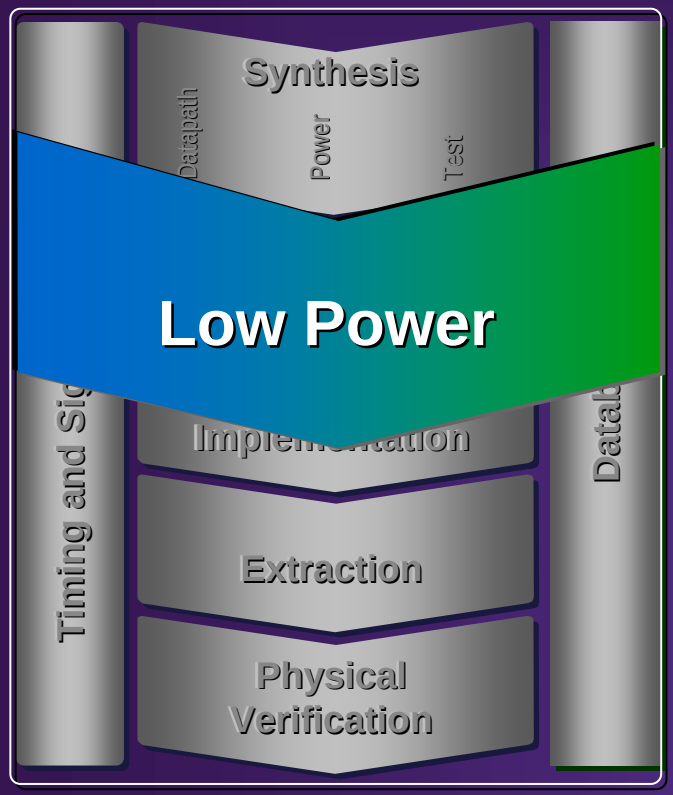
Future Trends



- Power density is doubling at every technology node
- Leakage power contribution increasing
- Power is tackled by technology, standards (GSM, OS), software, digital and analog hardware and tools
- Emerging trends include multi-V_{th}, multi-$V_{dd,}$ dynamic and adaptive voltage scaling
- Power sign-off a must

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Summary

Smaller, Cheaper

- DFM, Mixed Signal, Test, etc

Increasing Design Cost

- IP, SLD, structured ASIC, etc.

Faster

- Timing closure, SI, Statistical Timing, etc.

Less Power

- Process, circuits, architecture, SW, Energy efficient design

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