PHILIPS

Is there a Future for Differentiating ICs for High-End Televisions ?

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Outline

- High-end televisions
- Picture Quality Roadmap
- Current approach
- Technology Roadmap
- Solution?
- Conclusions

Television Market

Three market segments:

- High 1M Philips sets 1500-10000 $
- Mid 3M Philips sets 500-1500 $
- Low 9M Philips sets < 500 $

Philips Consumer Electronics

- #2 worldwide
- #1 Europe

Market players:

- Leaders; present in high-end
- Followers

High-End Television

High-End Television

High-end market segment:

- Entry point innovation
- Large margins
- Branding
- Differentiation is key

Current differentiation on picture quality

SD / HD source => HD display (Europe / USA)

- Spatial up-conversion
- Temporal up-conversion
- Image enhancements

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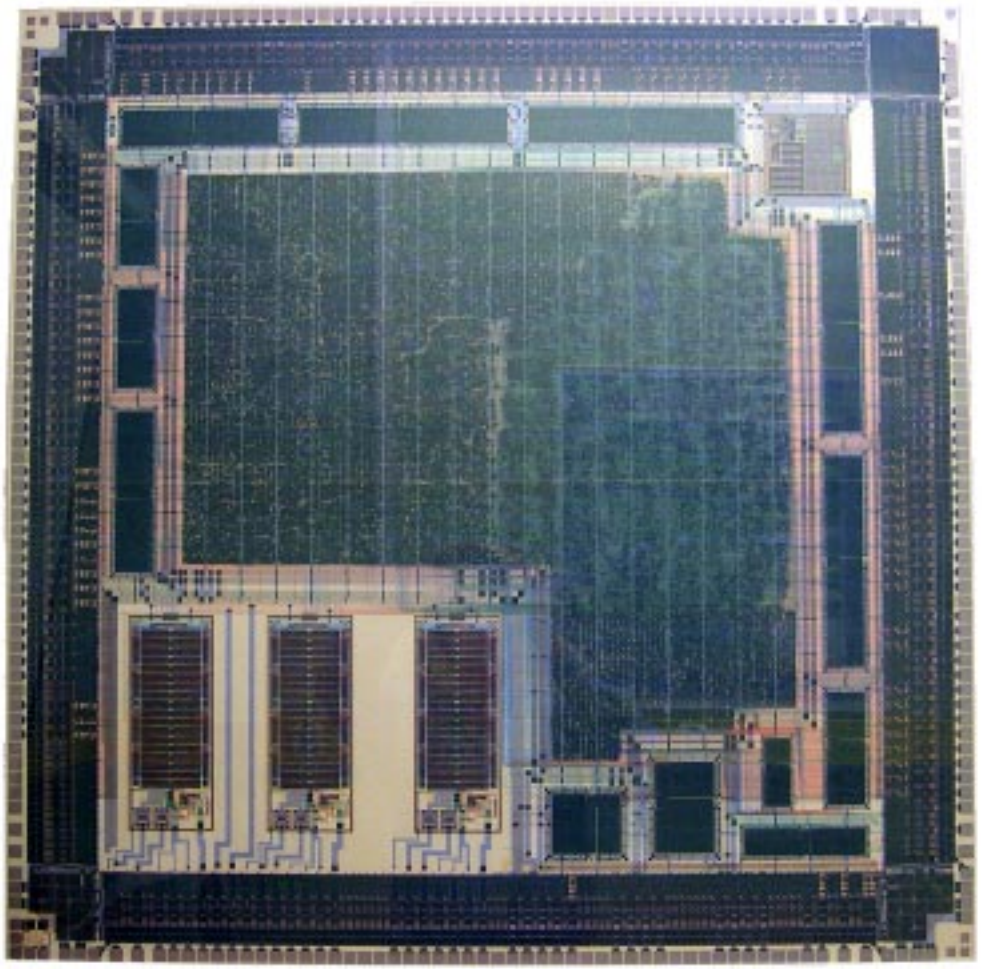
Picture Quality Roadmap

Digital image processing improvements like:

- Sub pixel based luminance transient improvement
- Dynamic contrast
- Digital natural motion
- Color dependent sharpness
- Green enhancement
- Blue stretch
- Skin tone correction
- 3-dimensional digital noise reduction
- scaling

Three EISA awards!!

Picture Quality Roadmap



Statistics:

401135 gates

32 mm2

278.4 kbit RAM

64 MHz

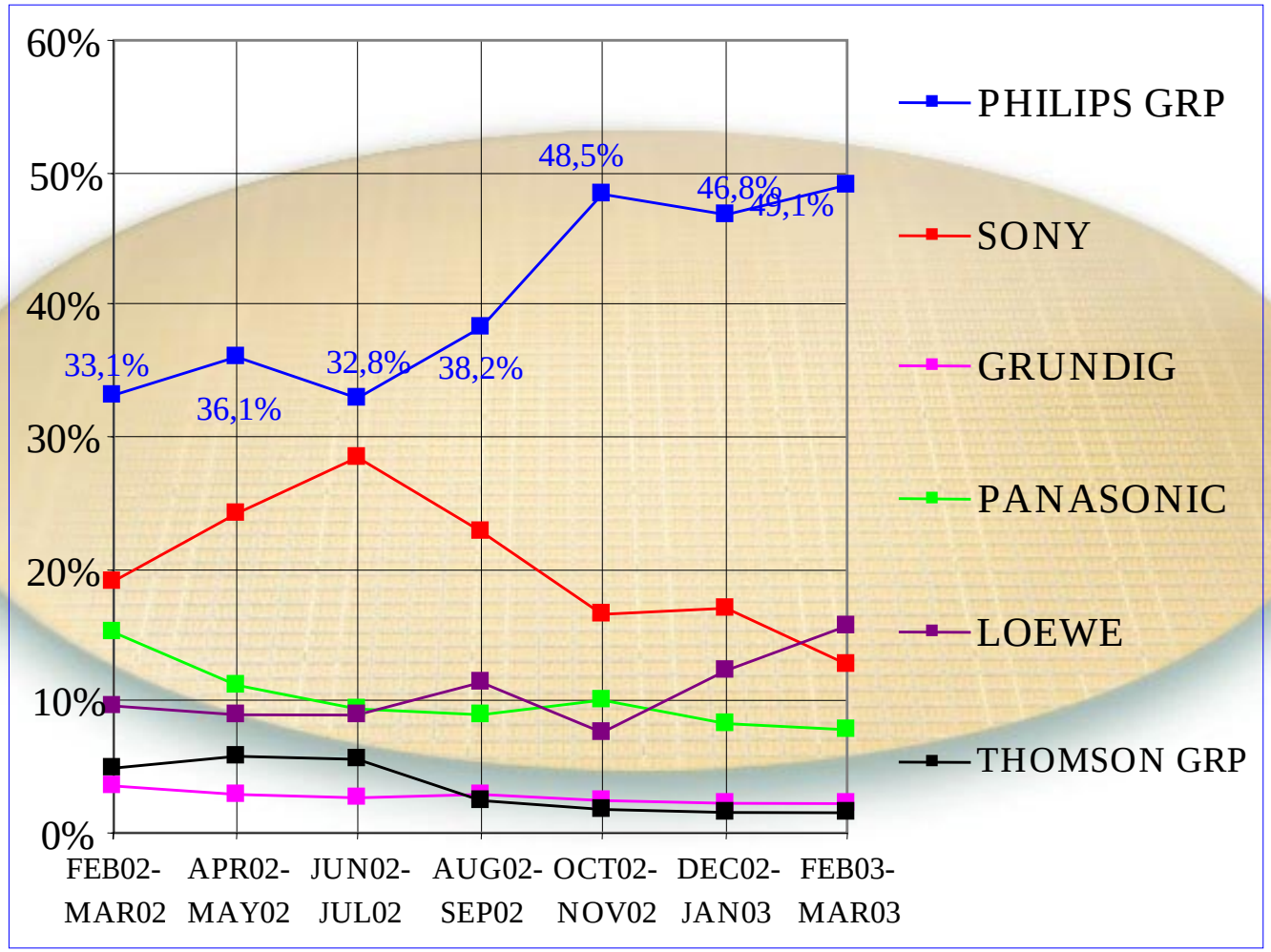
3 DAC's

PLL

0.18u; 4 metal layers

590 mW

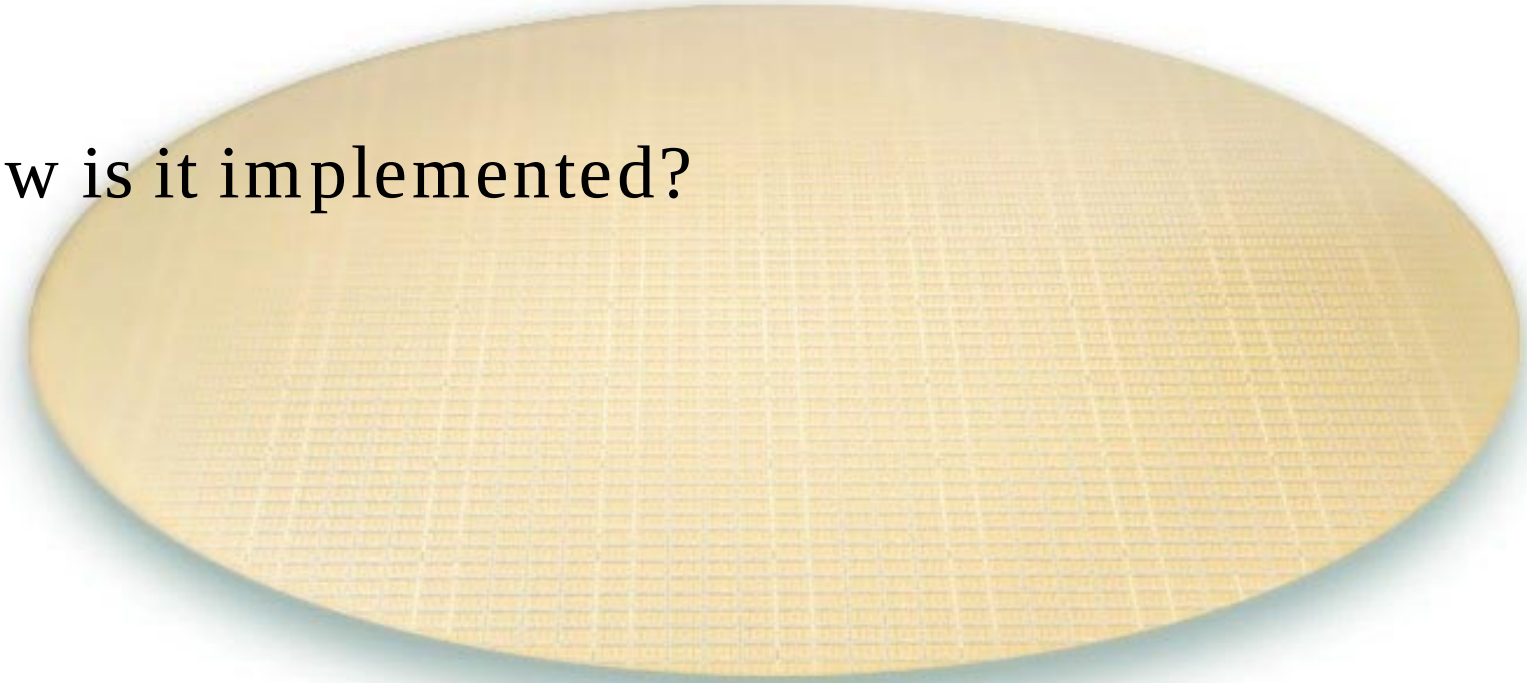
Picture Quality Roadmap



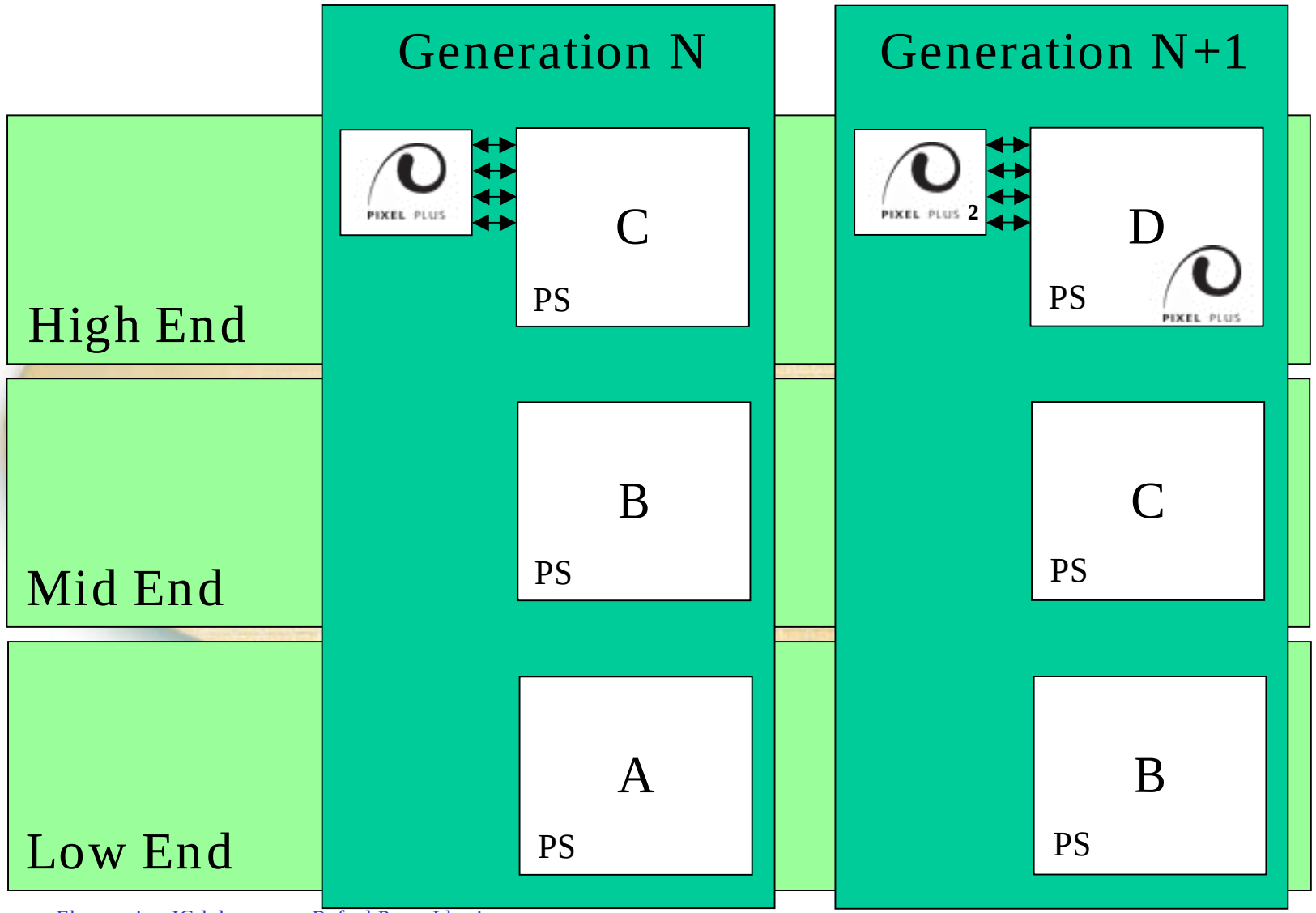
Picture Quality Roadmap

So far so good…

How is it implemented?



Picture Quality Roadmap



Picture Quality Roadmap

So far so good…

How is it implemented?

- Common TV platform provided by Philips Semiconductors
- Differentiation with additional key ICs
- Migration to future common TV platform

Lead time of differentiating functionality in market!

Picture Quality Roadmap

	G1	G2	G3	G4	G5
year	2001	2003	2005	2007	2010
resources (manyears)	100%	140%	320%	600%	1200%
technology (nm)	180	180	120	90	65
frequency (MHz)	64	64	133	250	350+
#Mgates incl. mem	100%	170%	500%	1000%	2000%
#Mgates excl. mem	100%	150%	500%	1250%	2500%

Picture Quality Roadmap

So there is the pain!!

- Exploding engineering costs
- Exploding complexity
- Exploding mask costs (~1M $ for 0.065u)!!

Current design approach is unsustainable

- Innovation will stop

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Requirements

Huge computational requirements

- HD @ 100fps = 200M pixels / s
- 1 pixel per clock
- 100-400 GOPS
- Regular & control dominated pixel processing

Communication requirements:

- Streaming data
- Latency tolerant (beware audio / video & football)

Power dissipation bounded (no fans)

Many different use cases (diversity)

Stability (no Ctrl + Alt + Del)

Current Approach

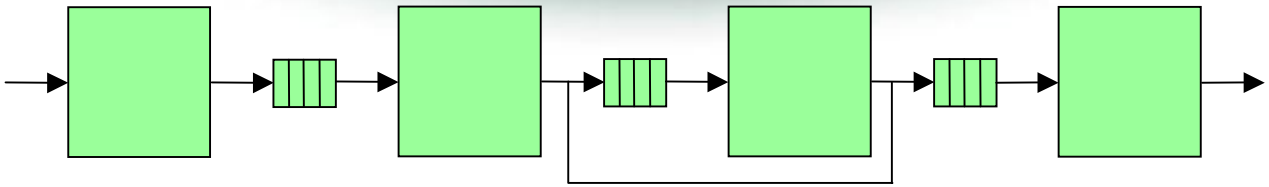
Computation:

- RTL VHDL blocks
- Heavy pipelining

Communication:

- FIFO buffers
- Handshaking
- Bypasses
- Centralized memory

Chain of video processing functions:



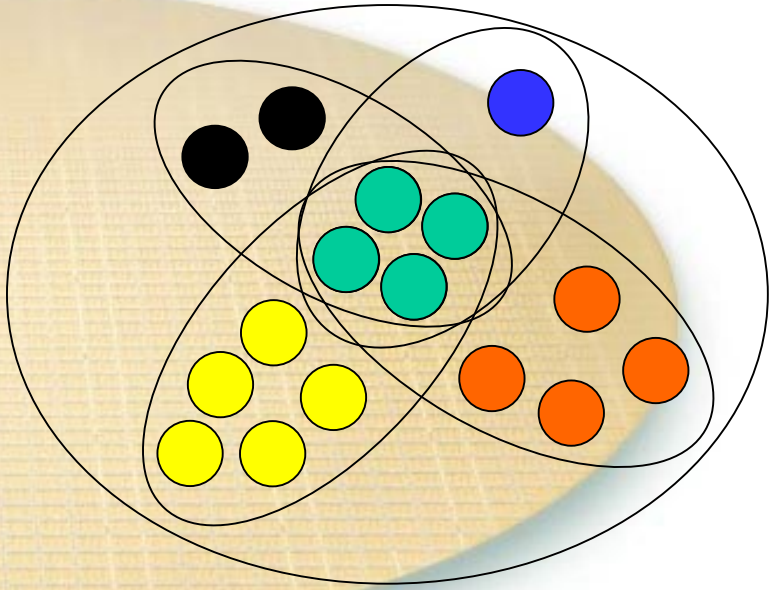
Current Approach

Many different use cases:

- Source (size, frame rate, TV, movie)
- Display (size, type)

Superset approach:

- Large volume
- High complexity
- Verification issue !!!!



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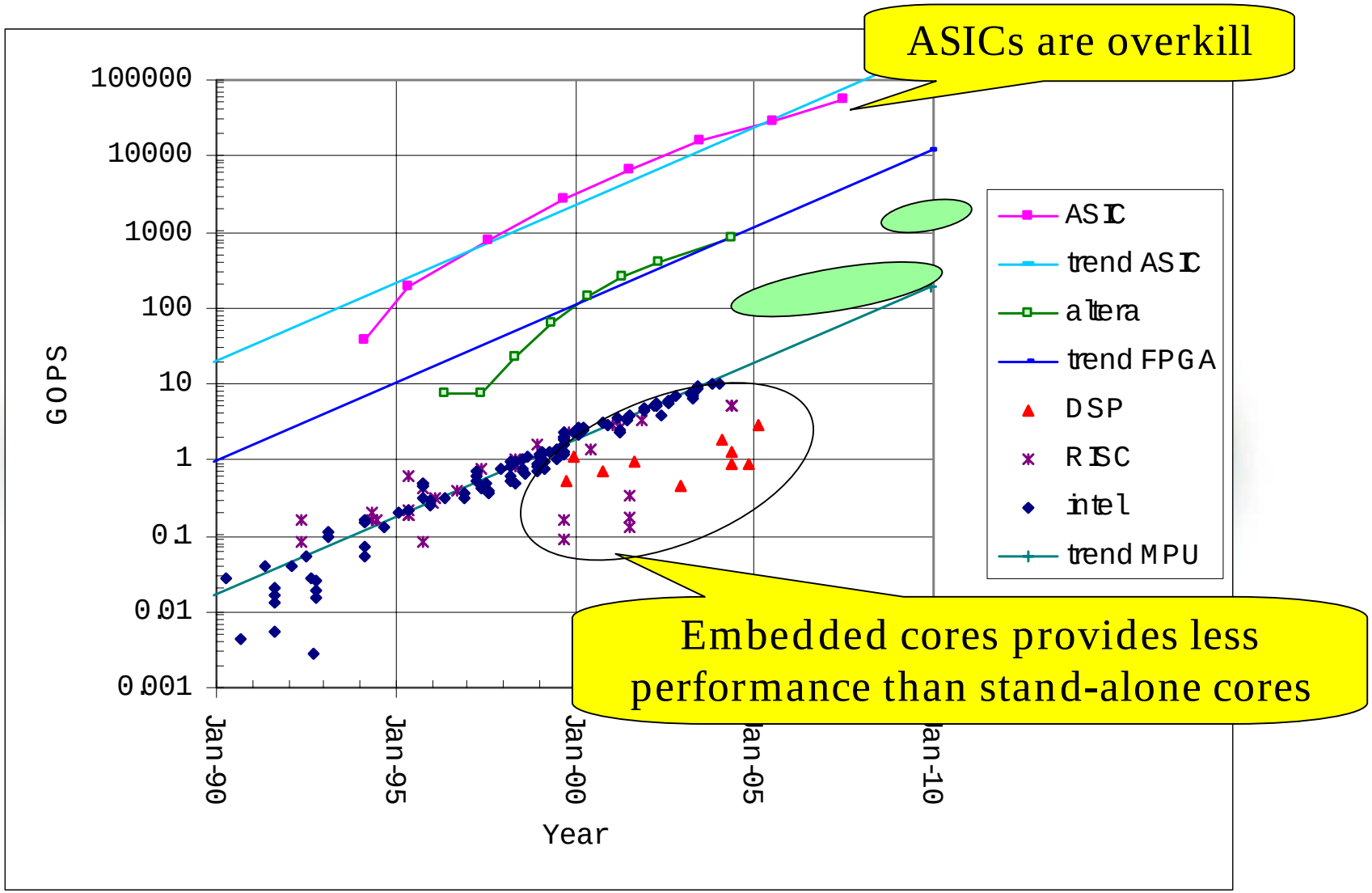
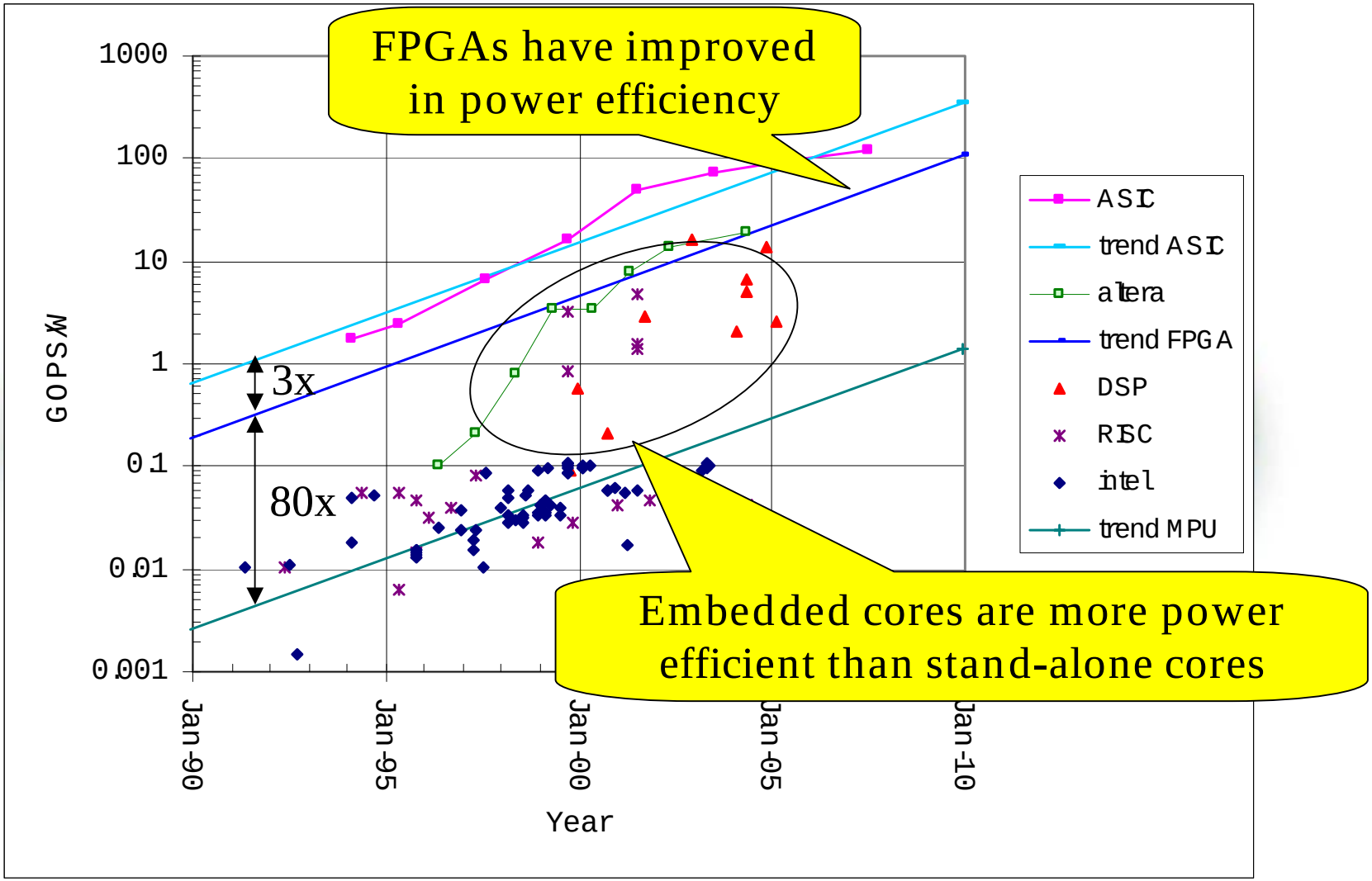
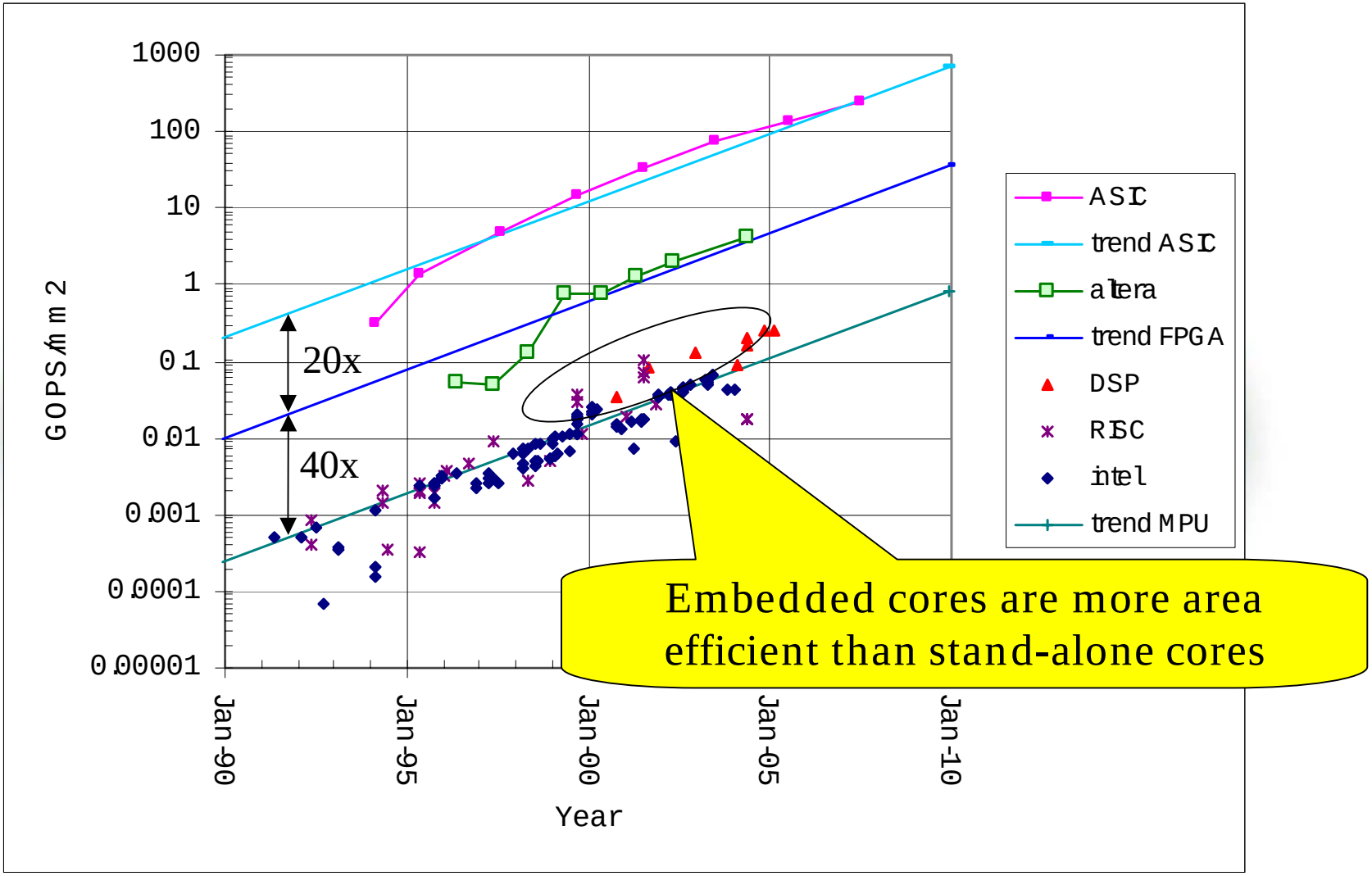
Technology Evolution



Technology Evolution



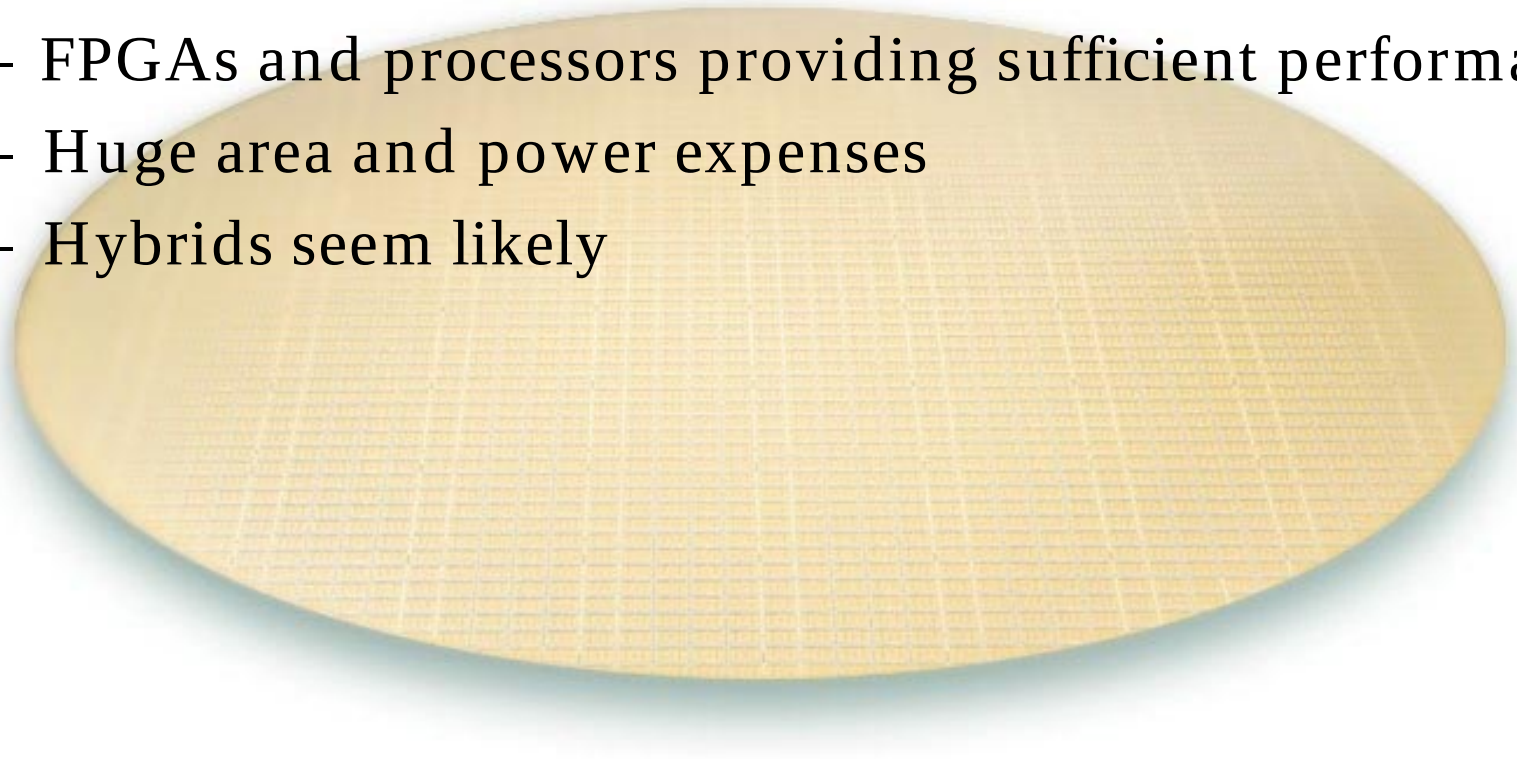
Technology Evolution



Technology Evolution

Observations:

- FPGAs and processors providing sufficient performance
- Huge area and power expenses
- Hybrids seem likely



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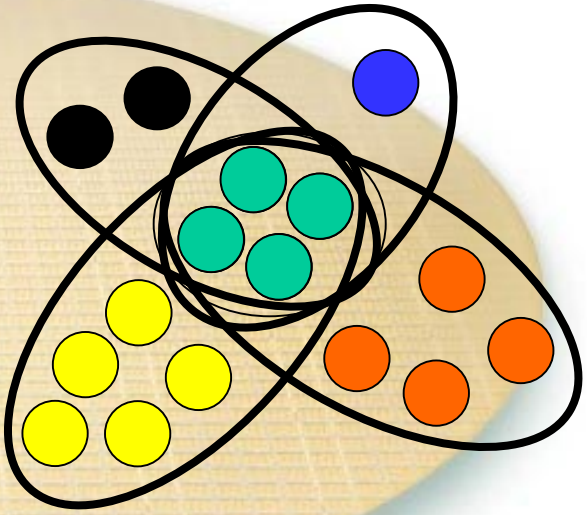
Solution?

Subset with flexibility approach:

Key:

- Composability
- Flexibility
- Scalability



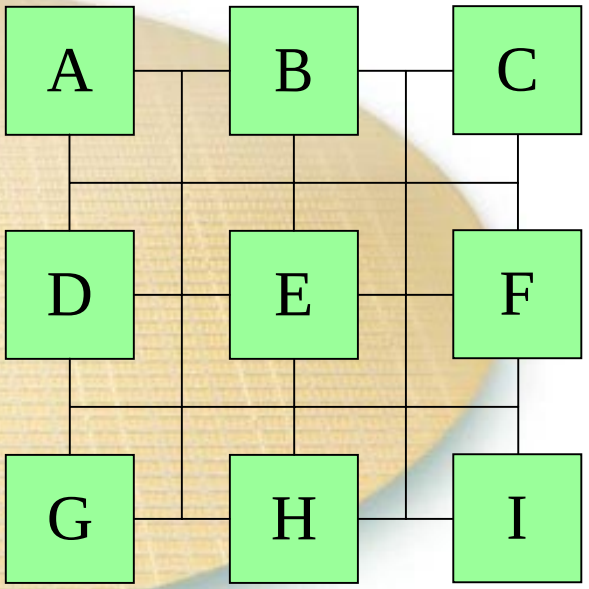
Solution?

- Exploding complexity and engineering costs:
  - Next step in design paradigm
    - Transistors => standard cells => synthesis => ?
  - Subset with flexibility approach
  - IP reuse
  - Composability
- Exploding mask costs:
  - Even larger volumes
  - Share silicon over more products
  - Flexibility / scalability

Solution?

Computation:

- Embedded processors?
- Dedicated HW blocks?
- Flexible (eFPGA) HW blocks?



Communication:

- Point to point?
- Busses?
- Network on Chip?

Computation

Embedded Processors:

- (Tunable) RISC / CISC
- VLIW / ULIW
- SIMD / vector
- Is SW cheaper than HW?

1 pel/clk

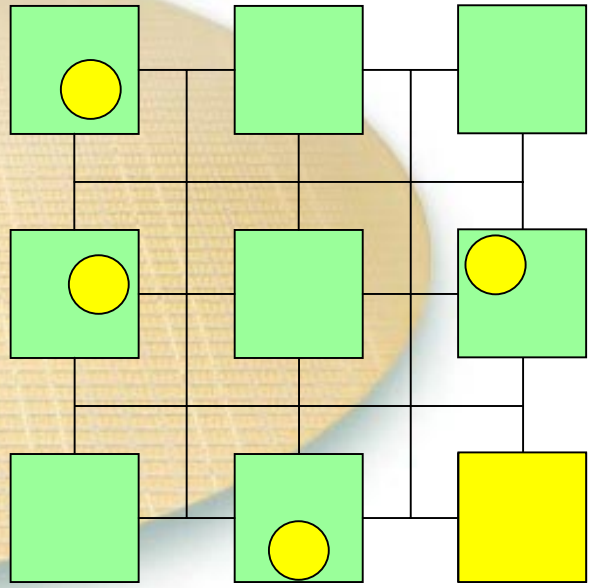
Dedicated HW blocks:

- Behavioral synthesis

Flexible HW blocks:

- Behavioral Synthesis
- Several e-FPGA blocks
- Fixed blocks with e-FPGA parts

20x area



Communication

Point to point:

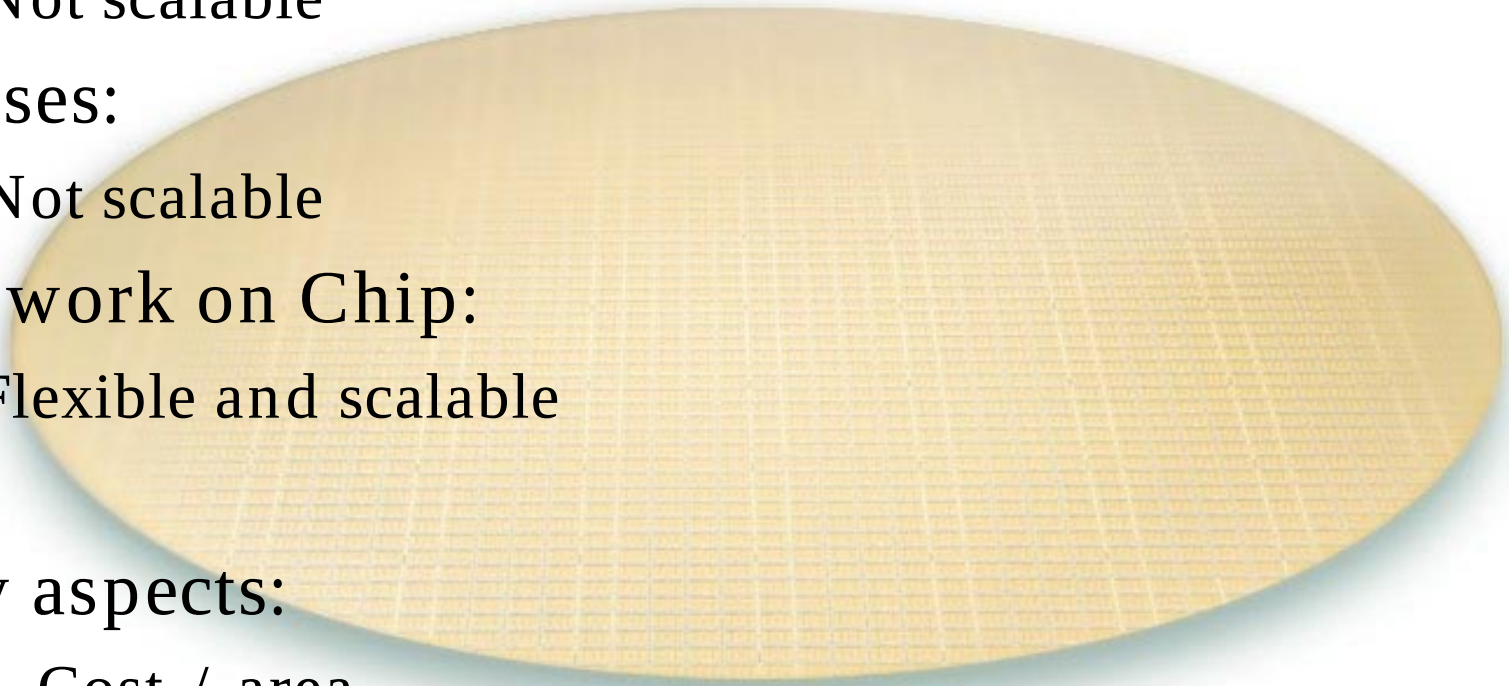
- Inflexible
- Not scalable

Busses:

- Not scalable

Network on Chip:

- Flexible and scalable



Key aspects:

- Cost / area
- Required degree of flexibility (diversity)
- Composability

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Questions / Challenges

Computation:

- Optimal mix ASIC / e-FPGA / programmable cores
- What should be flexible, what not
- Programming model

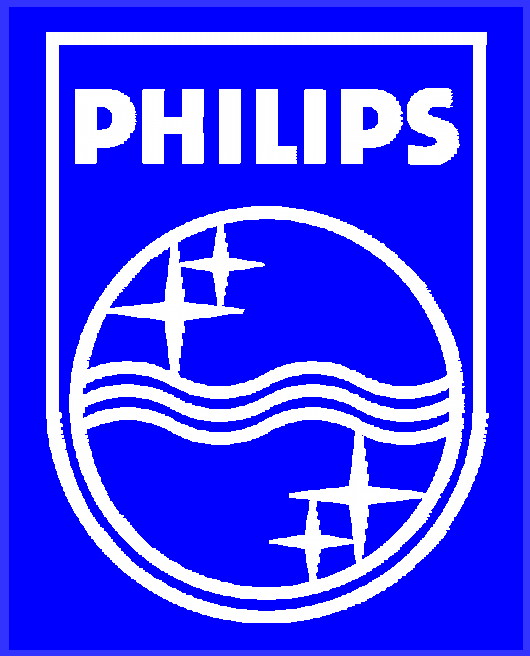
Communication:

- Composability
- Flexibility / scalability

Both:

- Power / area efficiency
- Engineering efficiency

Total cost (engineering hours + masks + silicon area)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