Power Management in Wireless SOCs

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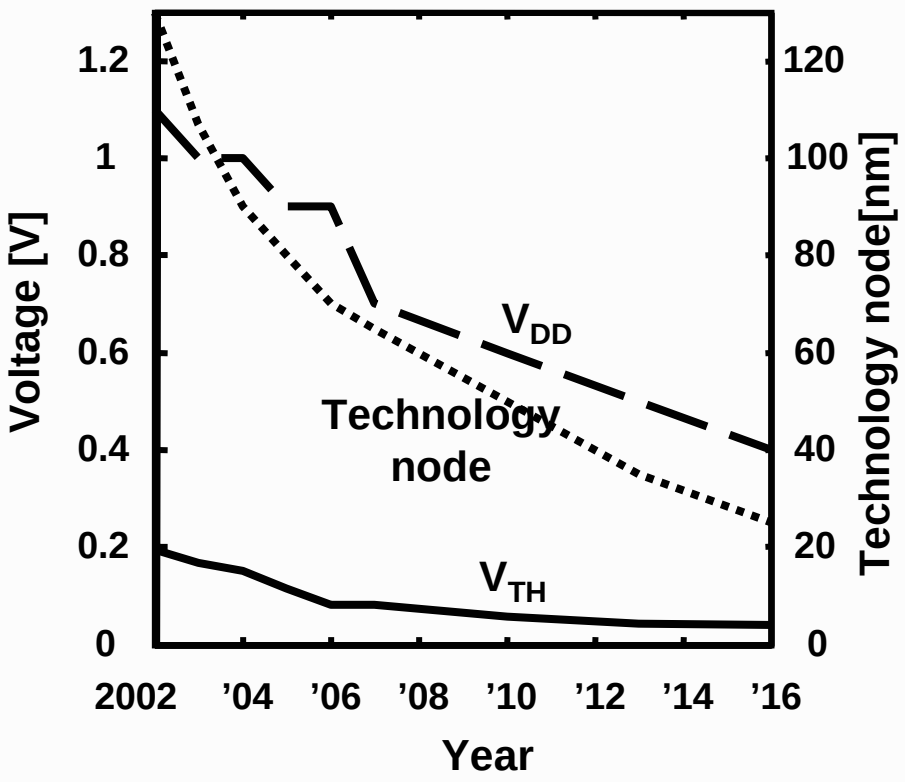
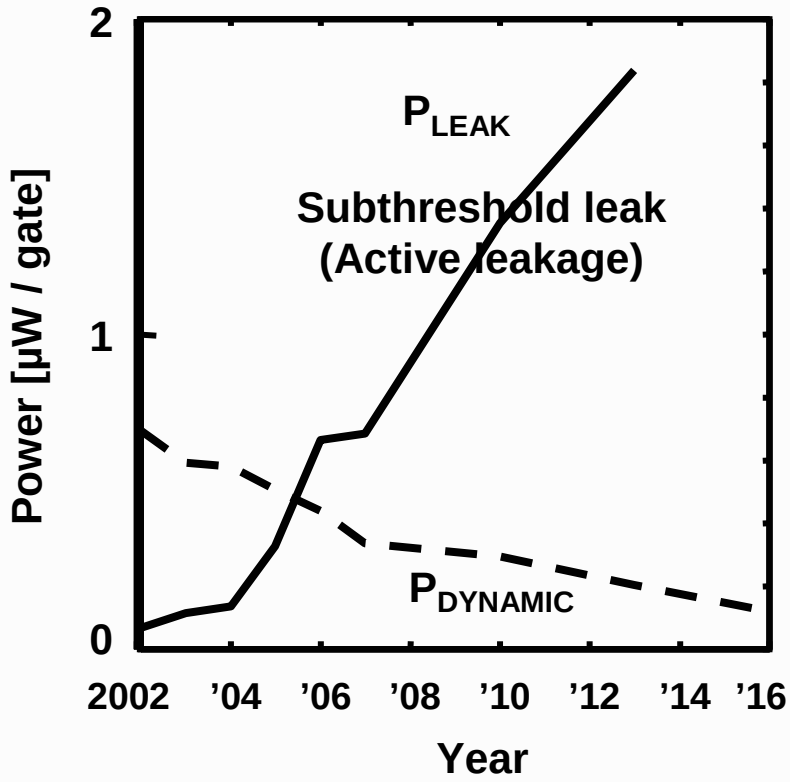
The Leakage Challenge (1)





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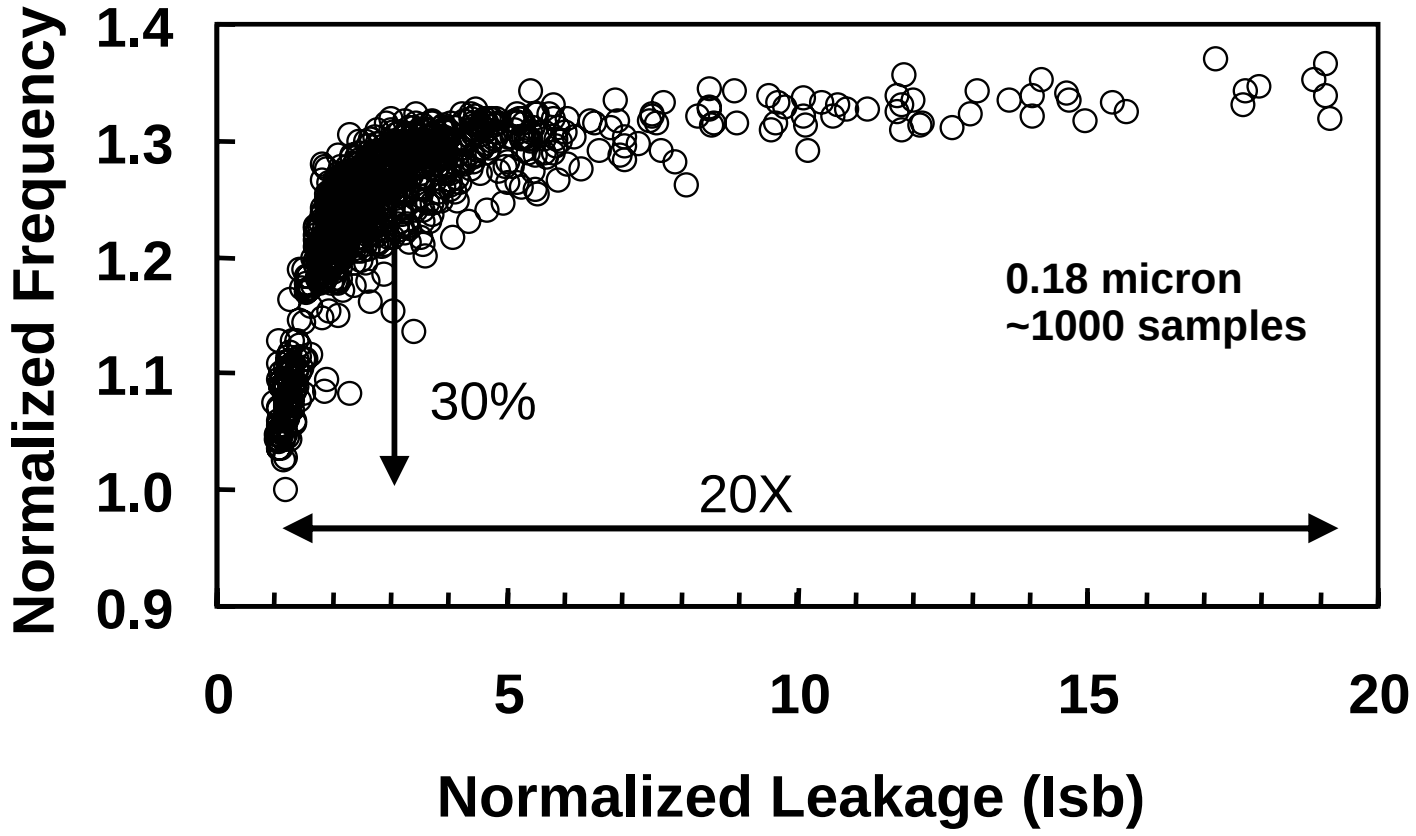
The Leakage Challenge (2)



Source: S. Borkar, Intel

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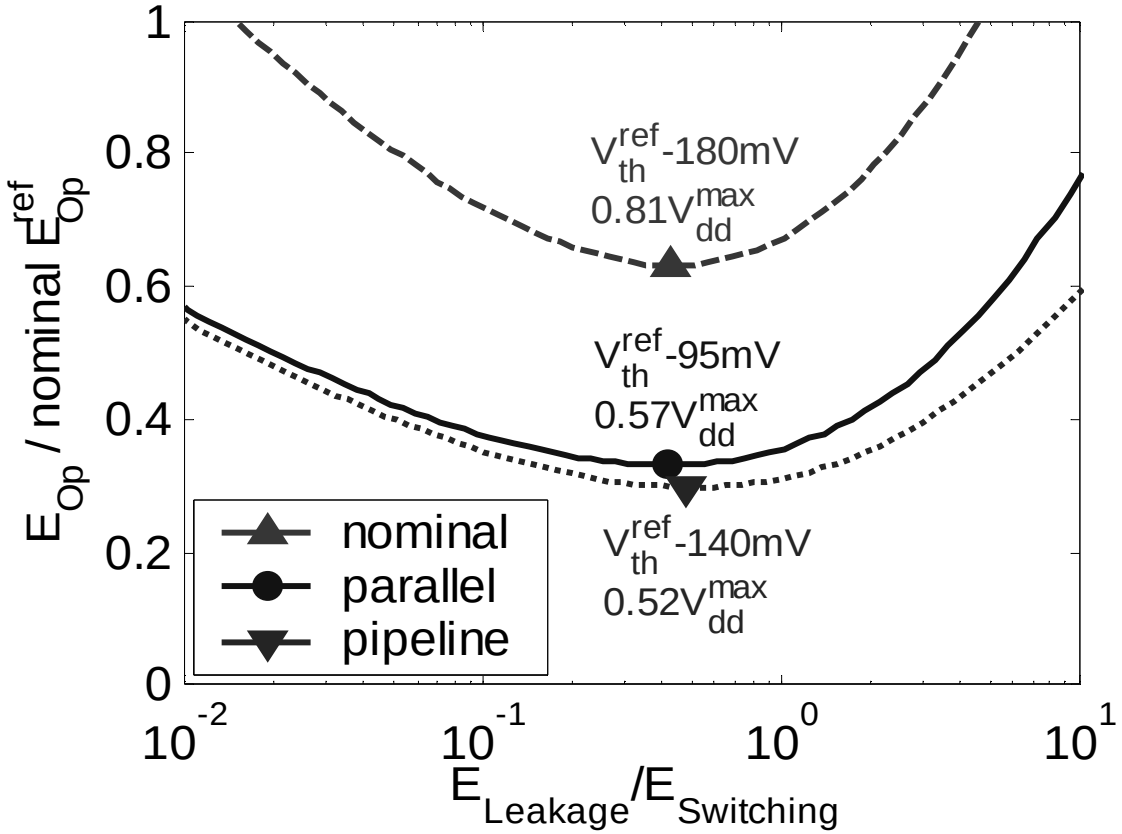
The Other Side of the Story: Leakage is good for you!



Optimal designs have high leakage ($E_{Lk}/E_{Sw} \approx 0.5$)

Must adapt to process variations and activity

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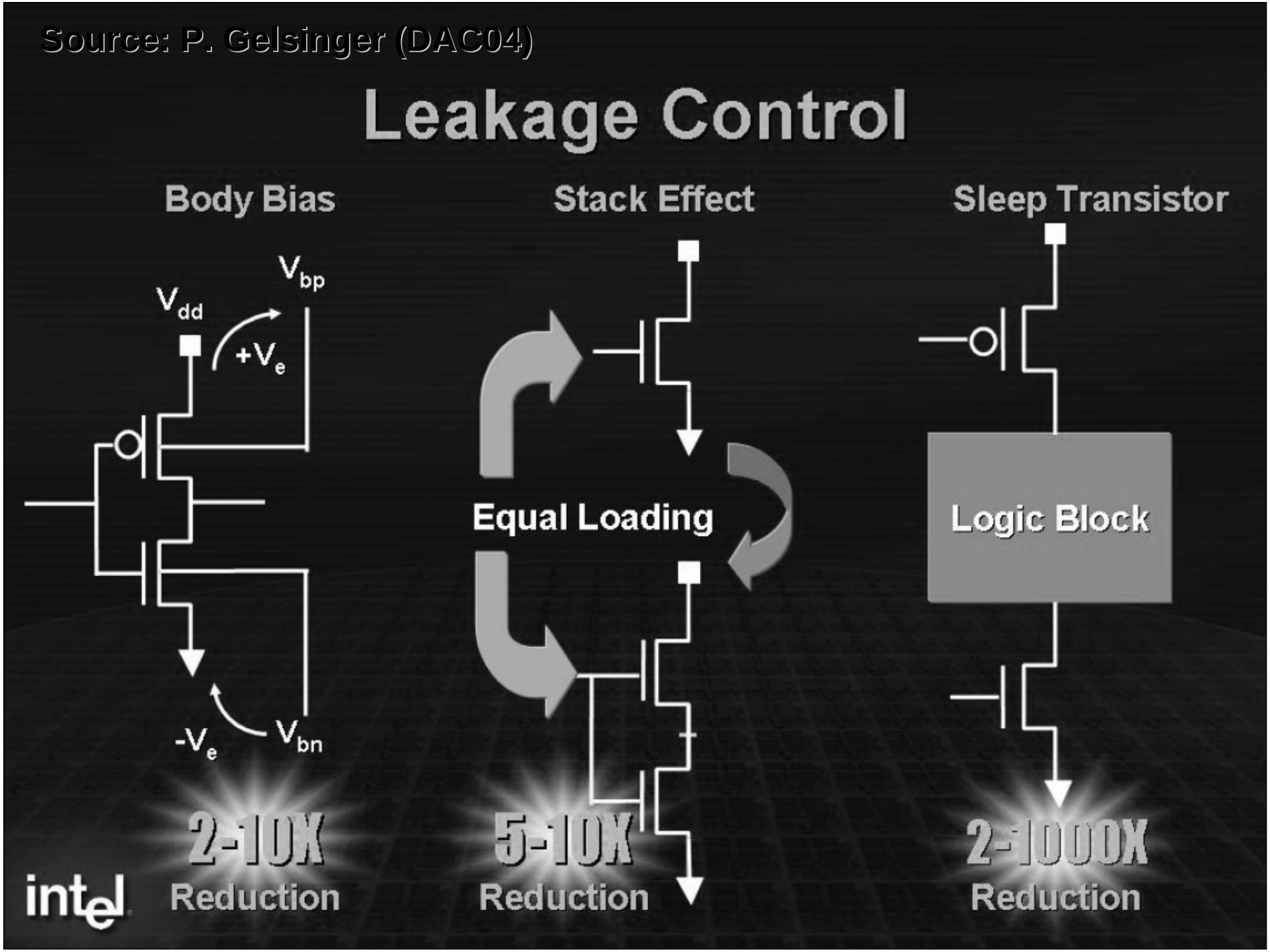
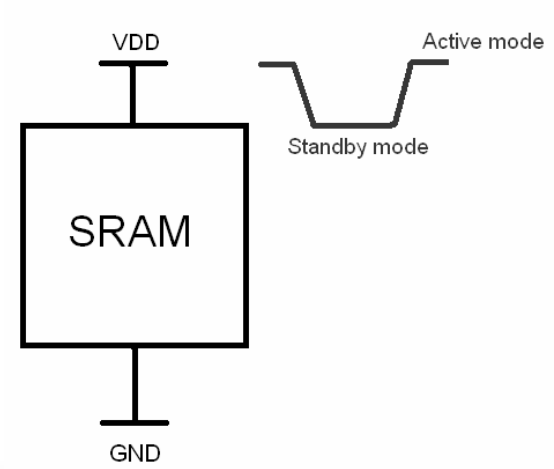
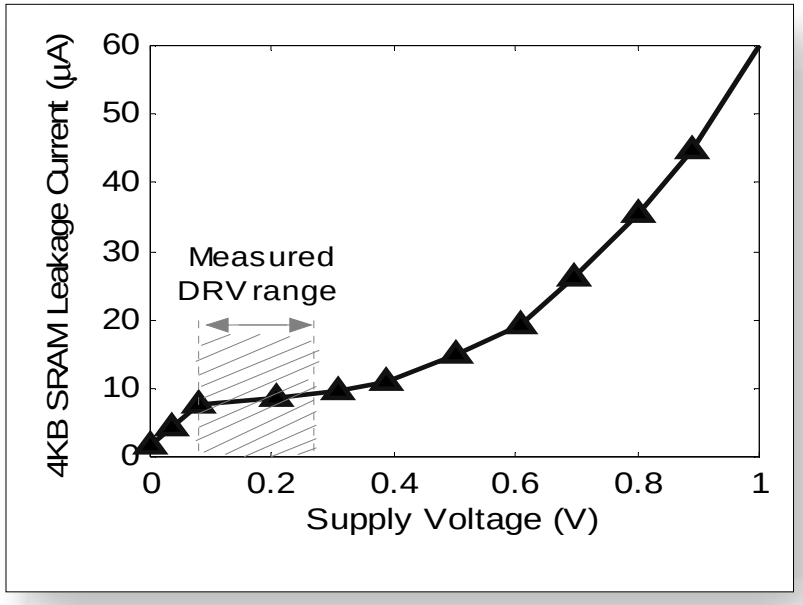
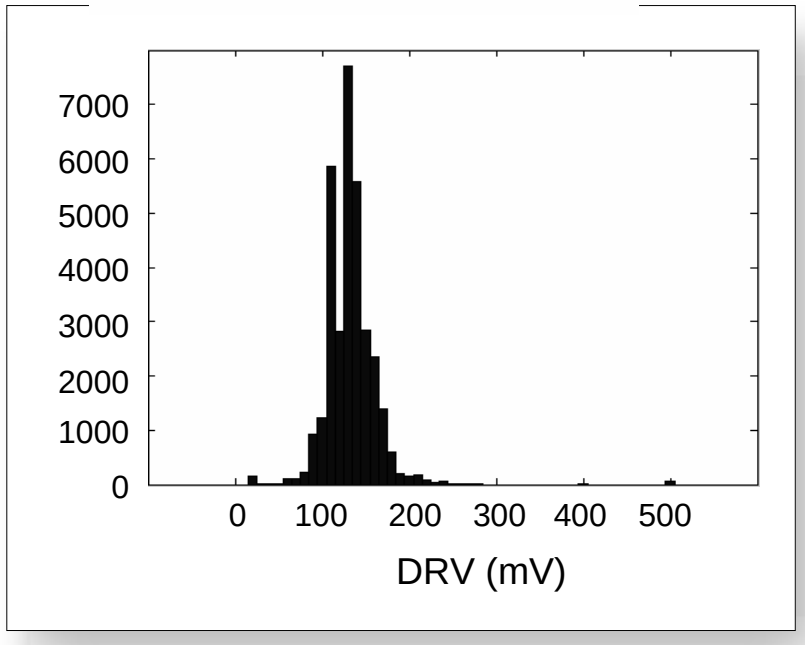
Source: P. Gelsinger (DAC04)



What to do about memory?
"The data retention voltage (DRV)







Data obtained from 4K bytes SRAM test-chip, implemented in 130 nm CMOS

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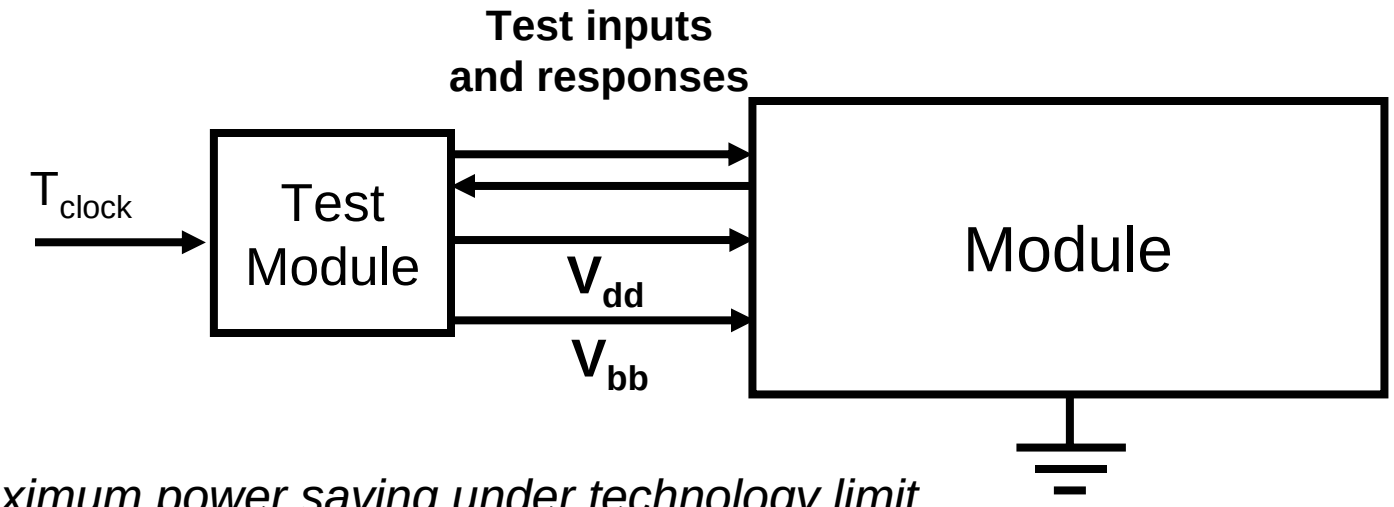
Calibrating for Process Variations

Most variations are systematic, and can be adjusted for at start-up time using one-time calibration!

- Relevant parameters: T_{clock}, V_{dd}, V_{th}
- Can be easily extended to include leakage-reduction and power-down in standby



- *Achieves the maximum power saving under technology limit*
- *Inherently improves the robustness of design timing*
- *Minimum design overhead required over traditional design methodology*

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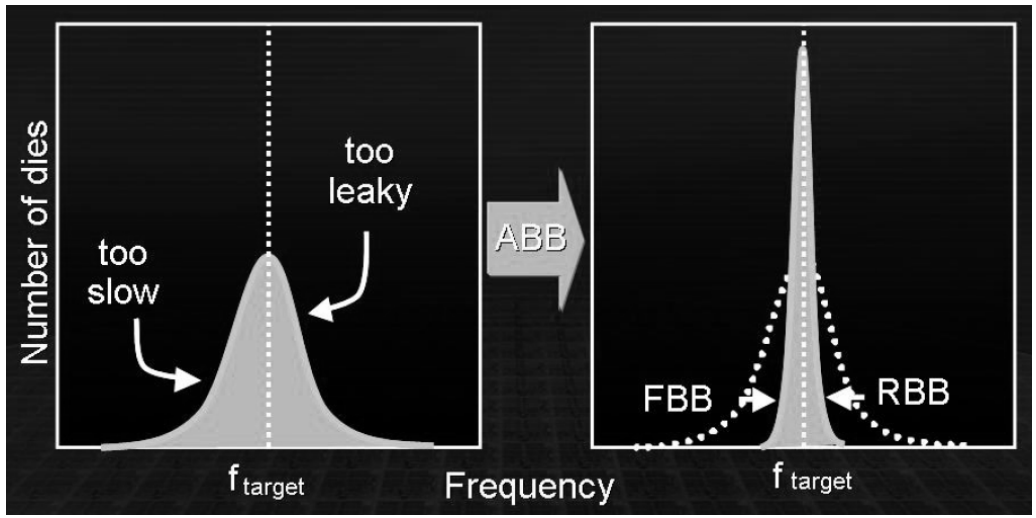
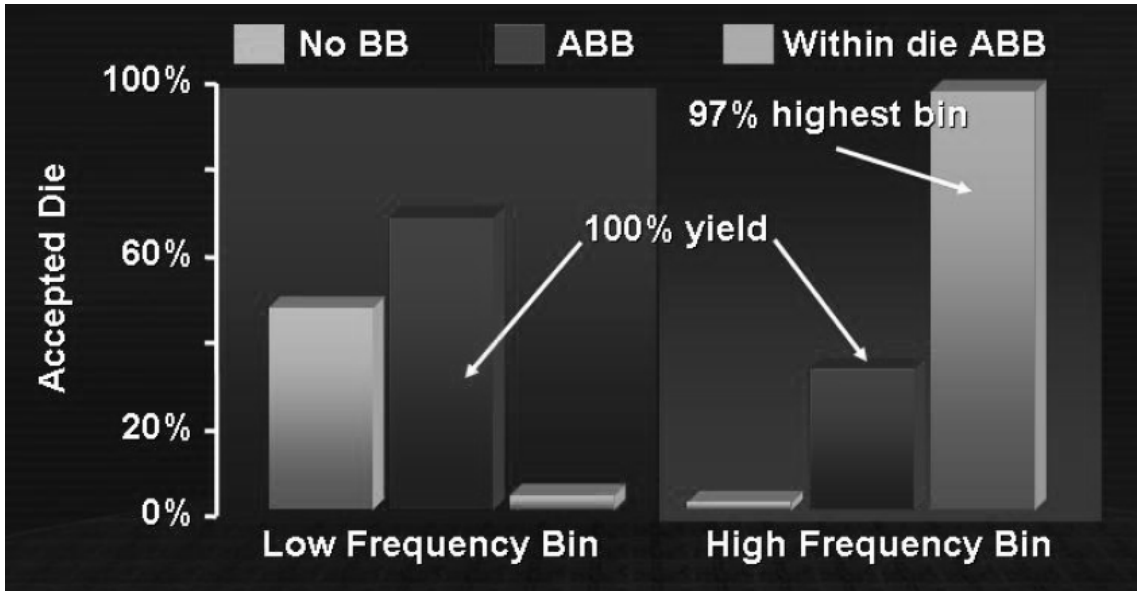
Adaptive Body Biasing



Source: P. Gelsinger (DAC04)



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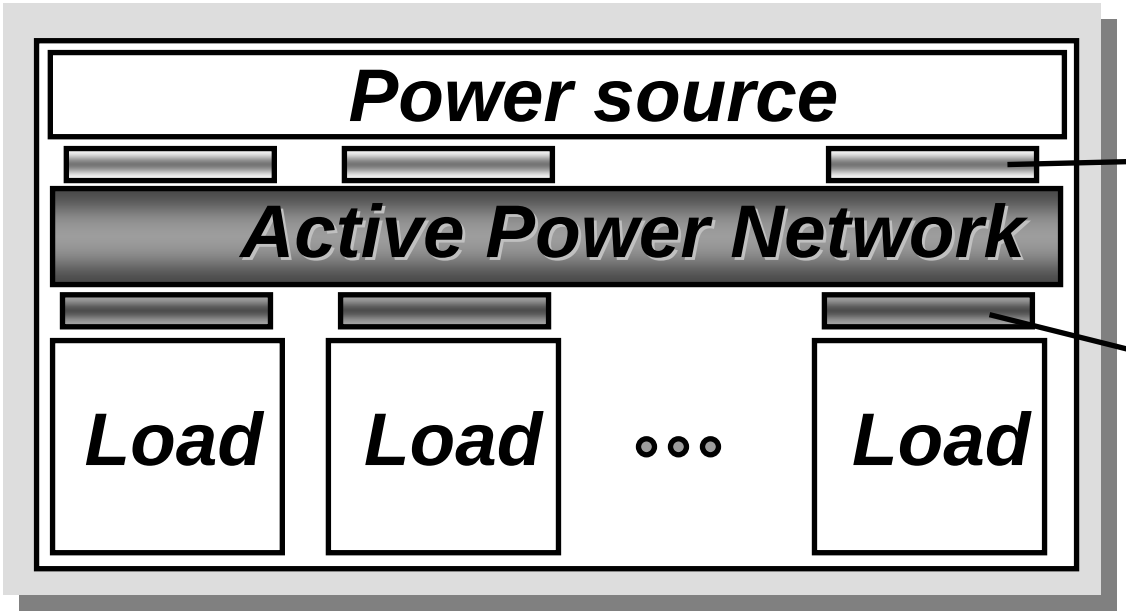
Introducing "Power Domains (PDs)"

Similar in Concept to "Clock Domains", but extended to include power-down (really!) and local supply and threshold voltage management.



- Dynamic voltages for variable workload
- Power gating or shut-off for leakage control
- Lifetime extension exploiting battery attributes
- Noise management

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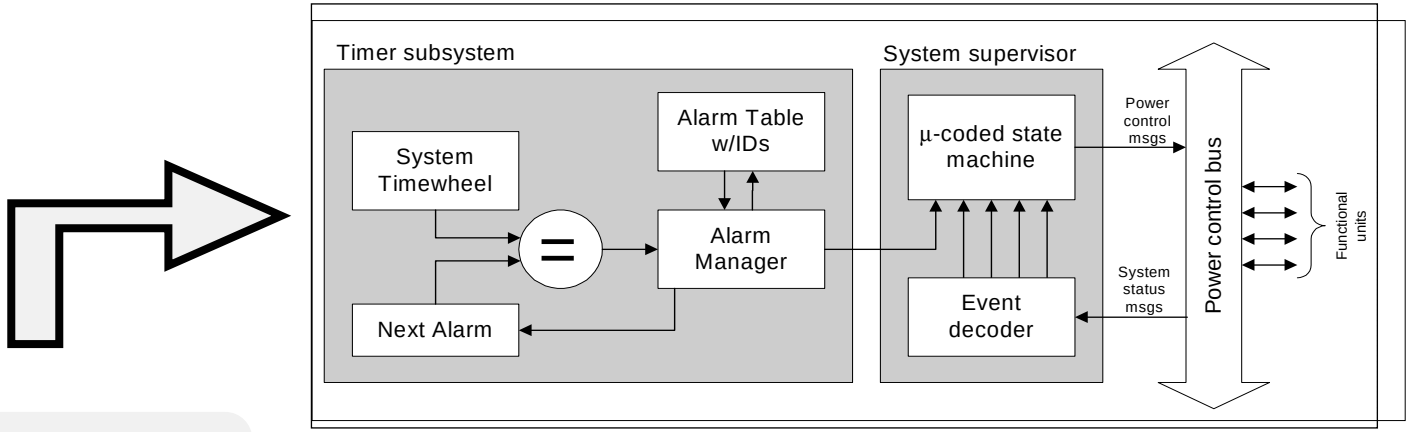
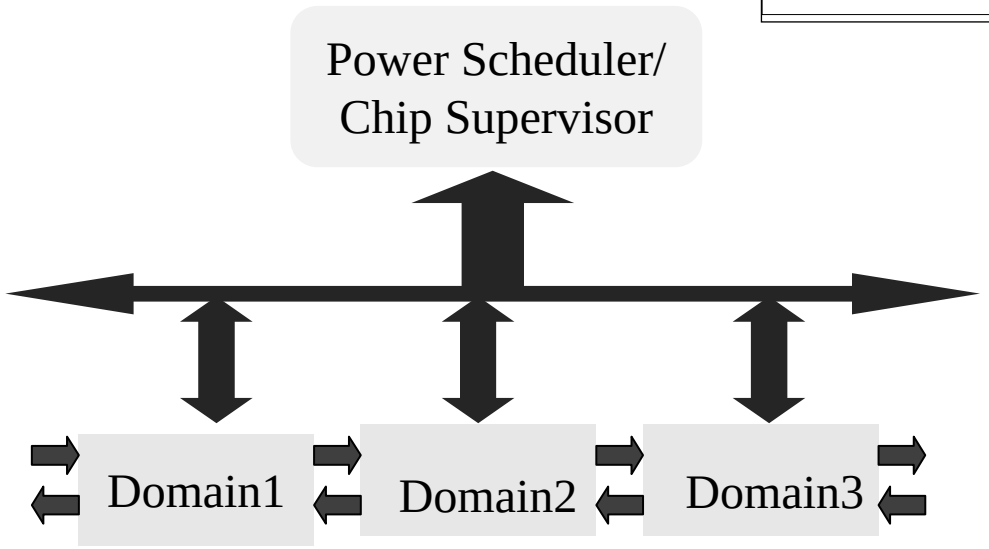
Introducing "Power Domains (PDs)"

Who is in charge?





Chip Supervisor (or Chip O/S)

- **Maintains global state and perspective**
- **Maintains system timers**
- **Alerts blocks of important events**

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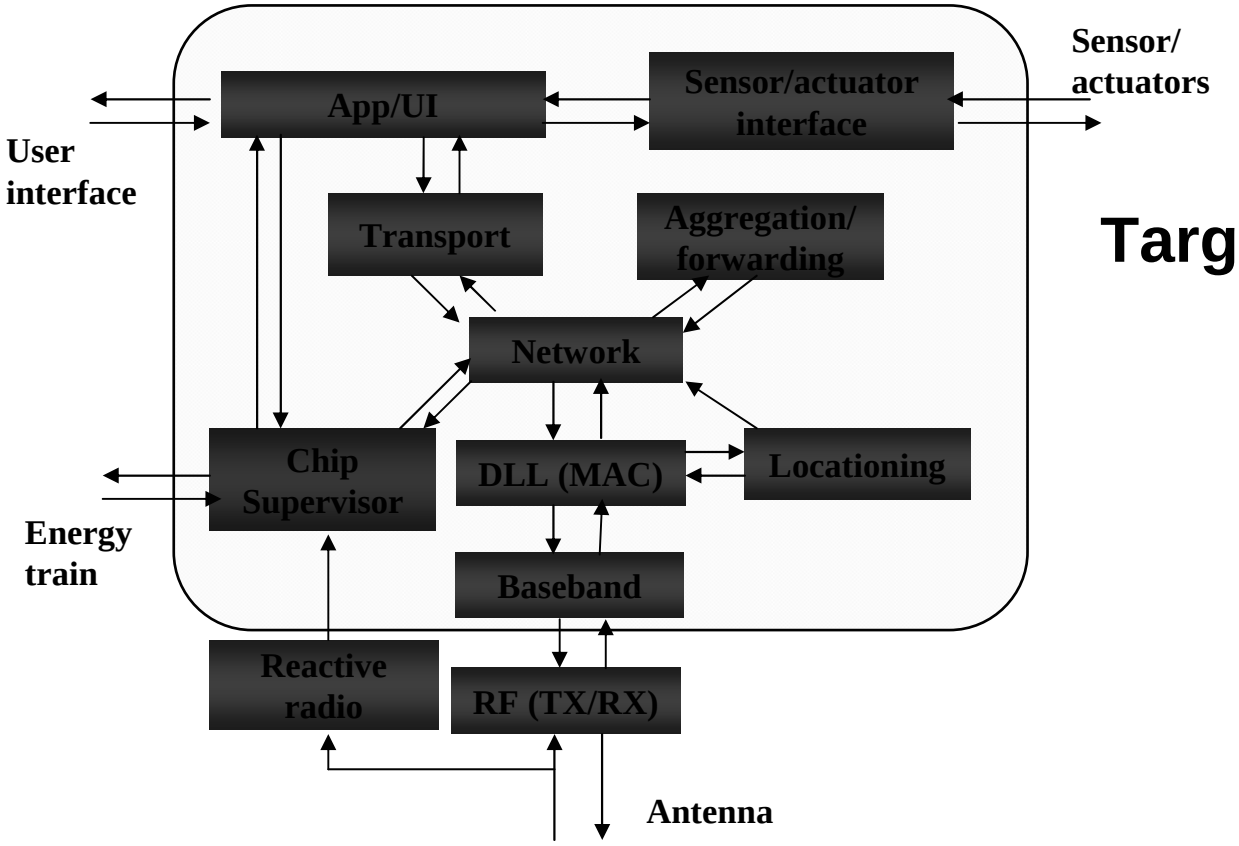
A Case Study —
Protocol Processor for Wireless Sensor Networks



Target: < 50 μW average

"Charm" Processor

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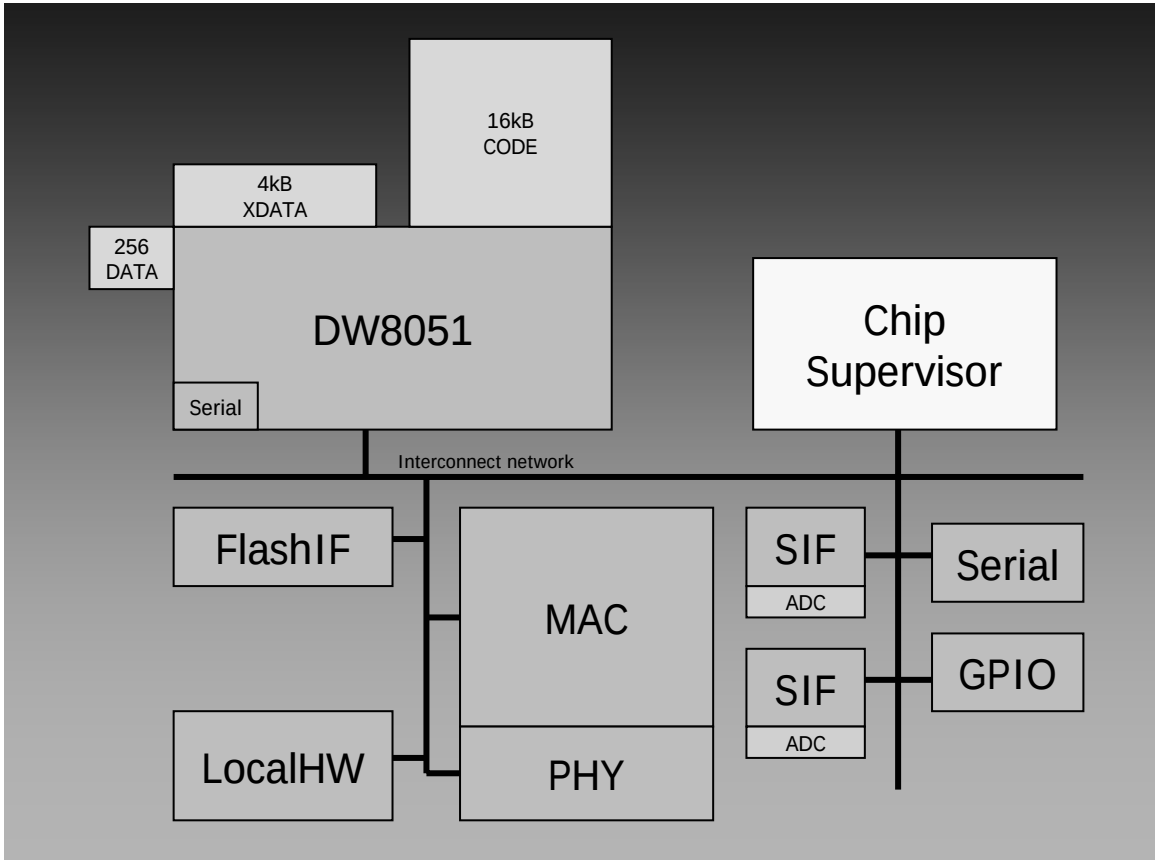
Charm Architecture



- **1 V operational supply voltage**
- **16 MHz Clock Frequency**
- **Simple processor aided with dedicated accelerators**

- **Reactive inter- and intra-chip signaling**
- **Aggressive Use of Power-Domains**
- **Chip Supervisor Manages Activity**

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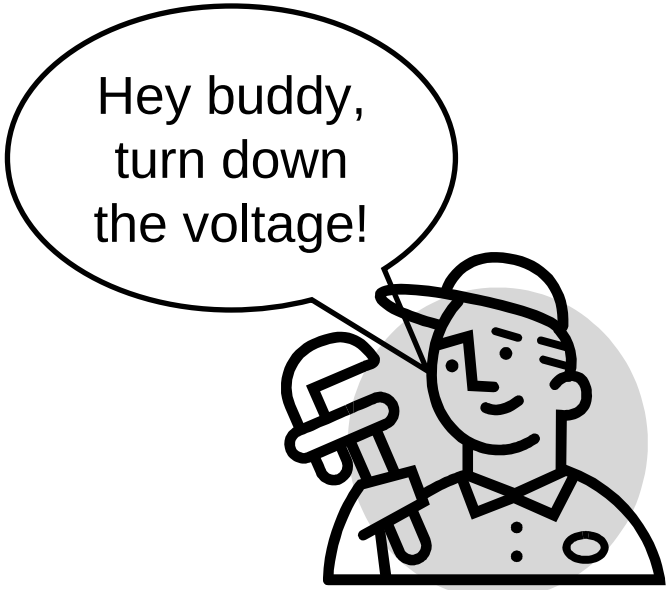
Call a Plumber…This Thing Leaks!

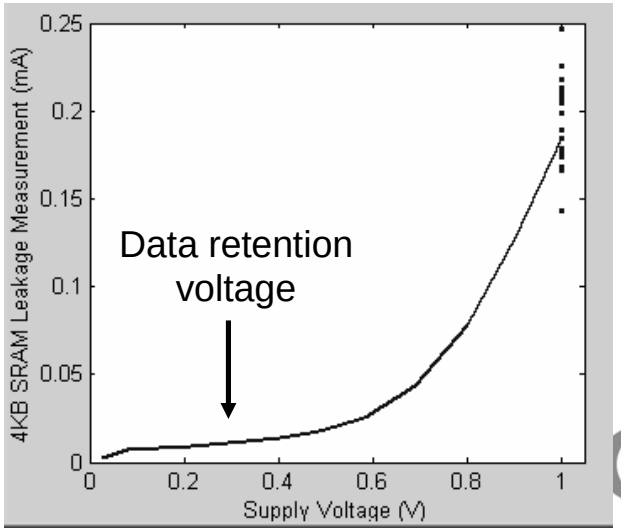
		Est. leakage @1V (uW)	
Block	**Area (um^2)**	**Logic**	**Memory**
Locationing	337990	39.9	
DW8051	63235	8.2	2880.0
Interface	6098	0.8	
Neighborlist	21282	2.5	13.5
Serial	2554	0.4	
NetQ	6296	0.7	108.0
DLL	126846	17.4	13.5
Supervisor	51094	6.4	
Total		**76.3**	**3015.0**

← 64KB SRAM for SW code and data

← 30X the target power…just in leakage!!



Leakage vs. Supply Voltage



~15X reduction

1/15 A * 0.3 V = 98% less leakage power

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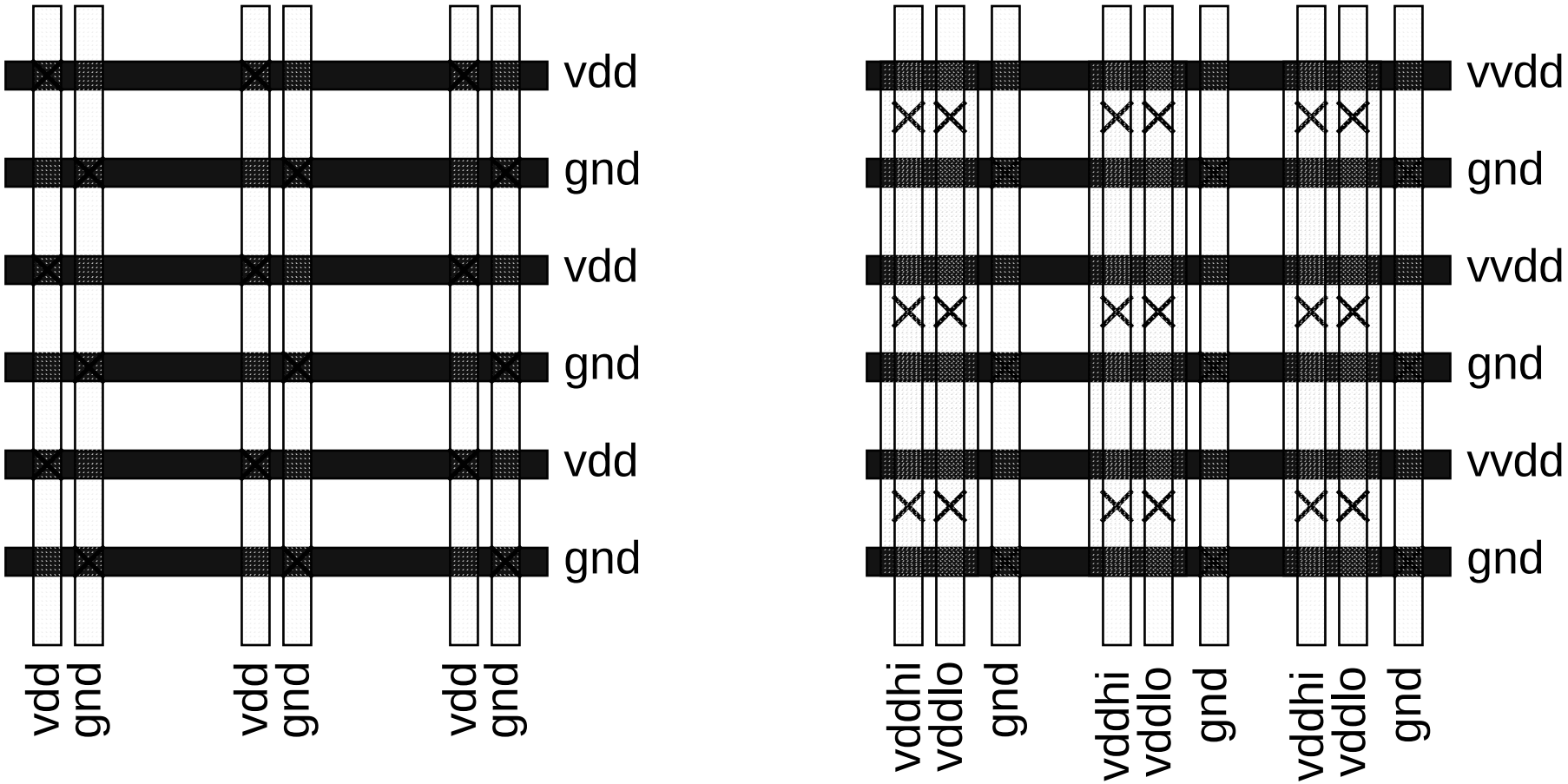
Gated Power Architecture



- **Vddhi – active mode voltage (nominal)**
- **Vddlo – standby mode voltage allows retention of state**

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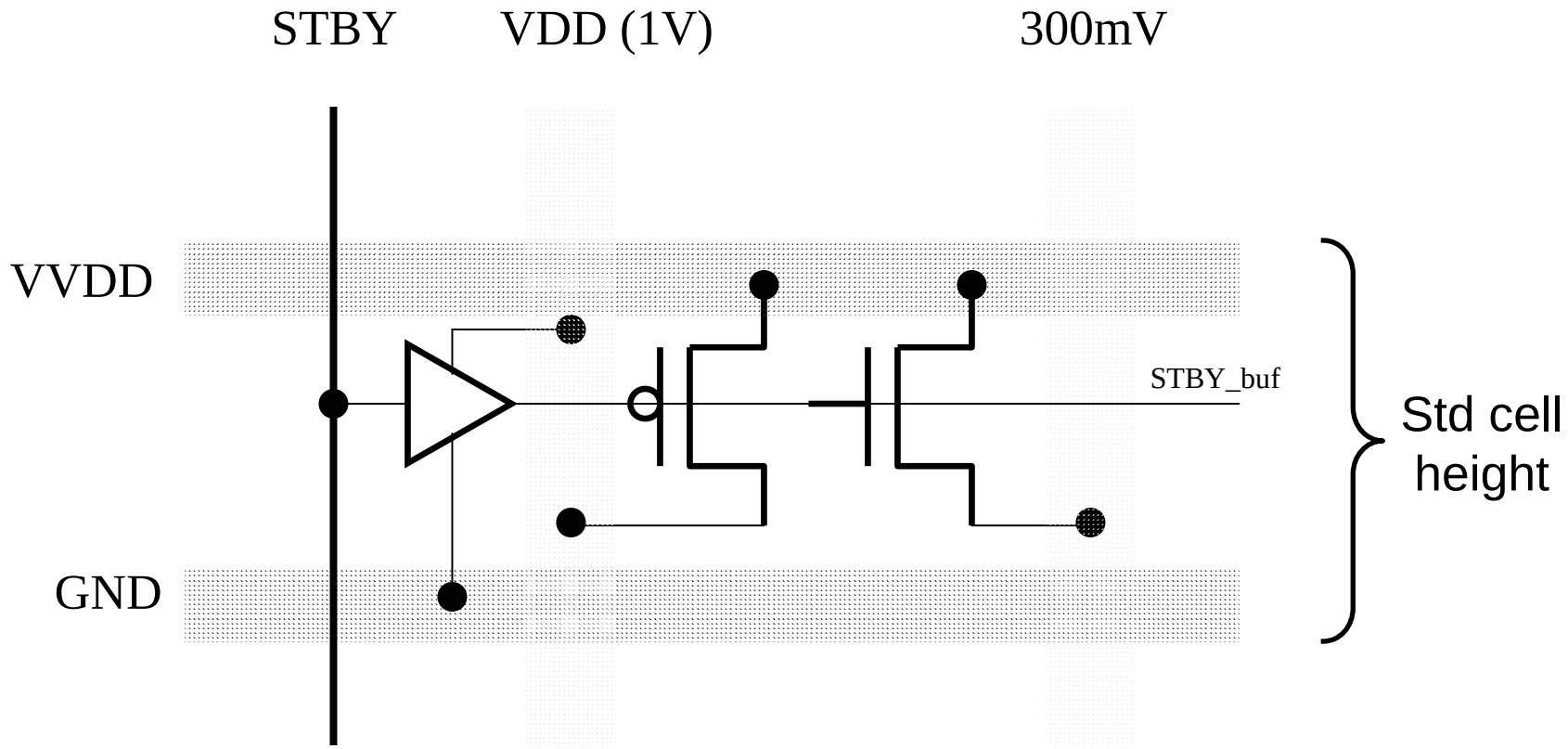
Power Switch Tile



- **Tile is easily incorporated into standard design flow**
  - Cell has same pitch as std. cell library components
  - Switch tiles placed prior to other standard cells
  - One additional power strap added to power routing step
- **Switch design can be independent of block size**
  - Built in buffer distributes driver circuitry
  - Enables creation of a buffer tree during STBY signal routing

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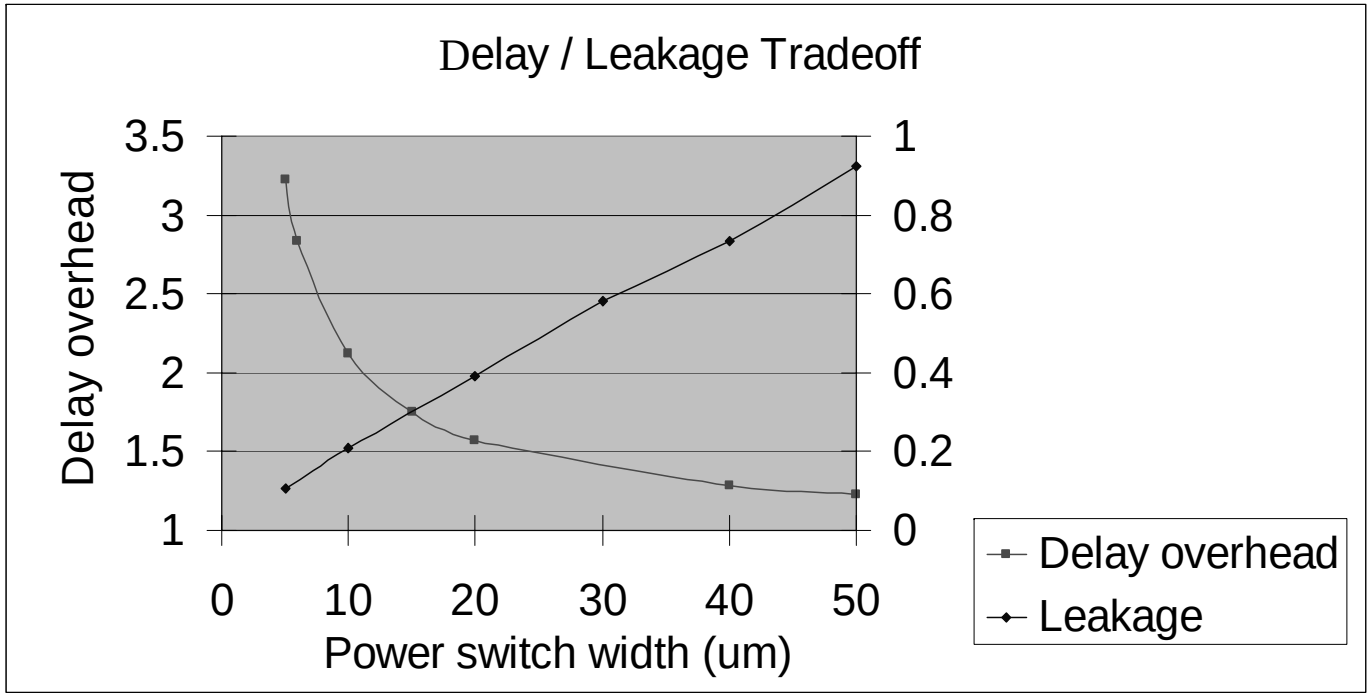
Power Switch Sizing



- **Switch sizing enables trade-off between delay overhead and leakage**
  - Delay scale normalized to un-gated design
  - Leakage scale normalized to case when switch size is 50 μm
- **Timing slack determines delay requirement**
  - Control domains (DLL, processor) – tolerant of delay overhead
  - Datapath domains (locationing) – longer critical paths, less tolerant of delay overhead

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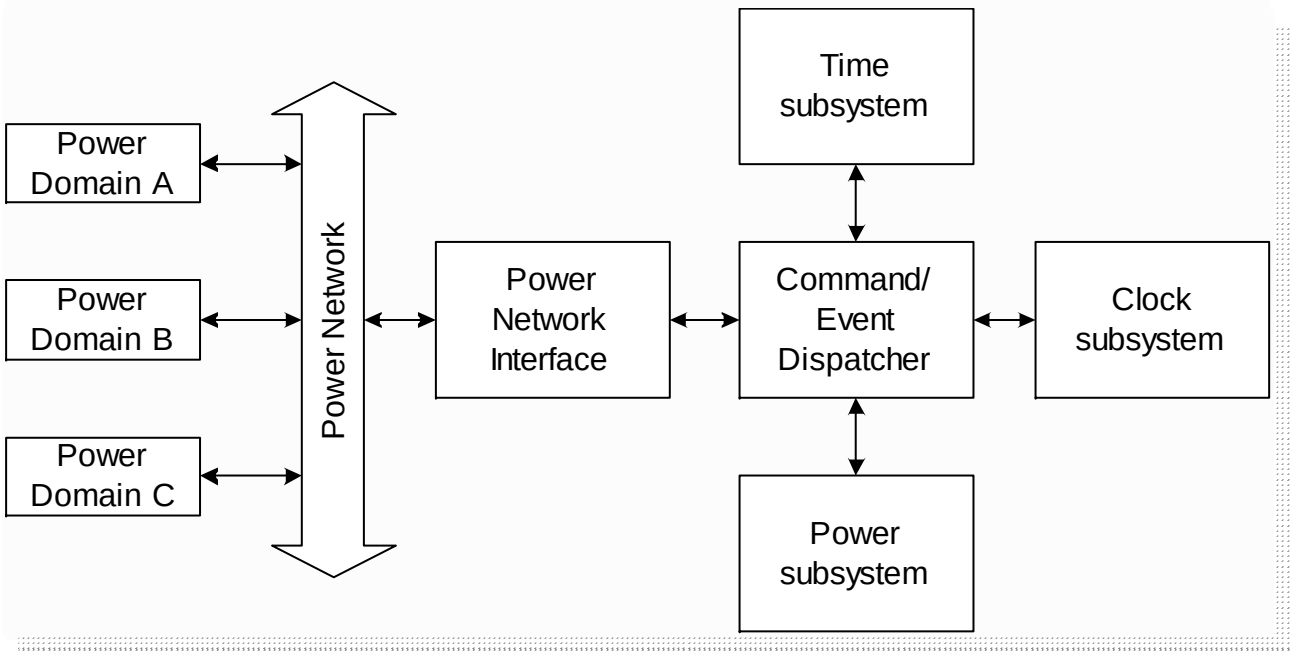
System Supervisor



- **How to control block activation/deactivation?**
- **System supervisor centralizes power control**
  - Power subsystem – gates block power rails
  - Clock subsystem – gates block clocks
  - Timer subsystem – system time-wheel and wake-up timers

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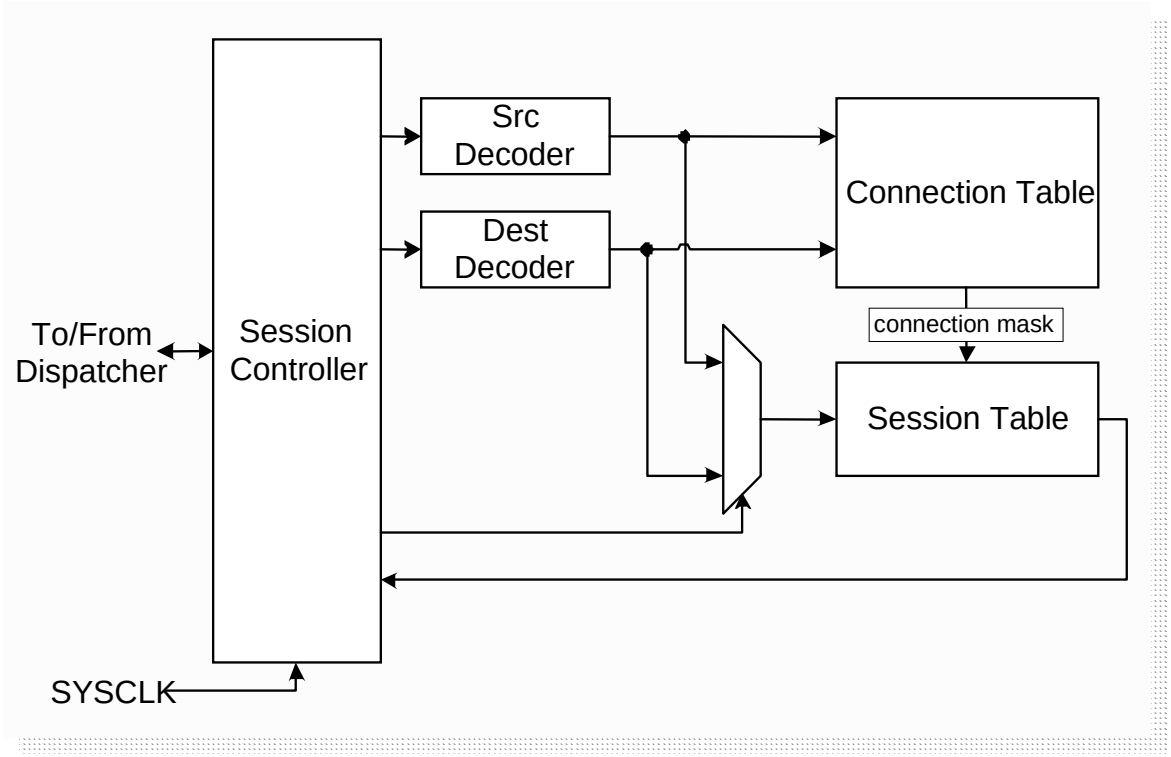
Power Subsystem



- **Session controller – opens/closes sessions**
- **Connection table – holds connectivity masks and performs port address translation**
- **Session table – keeps track of open sessions**

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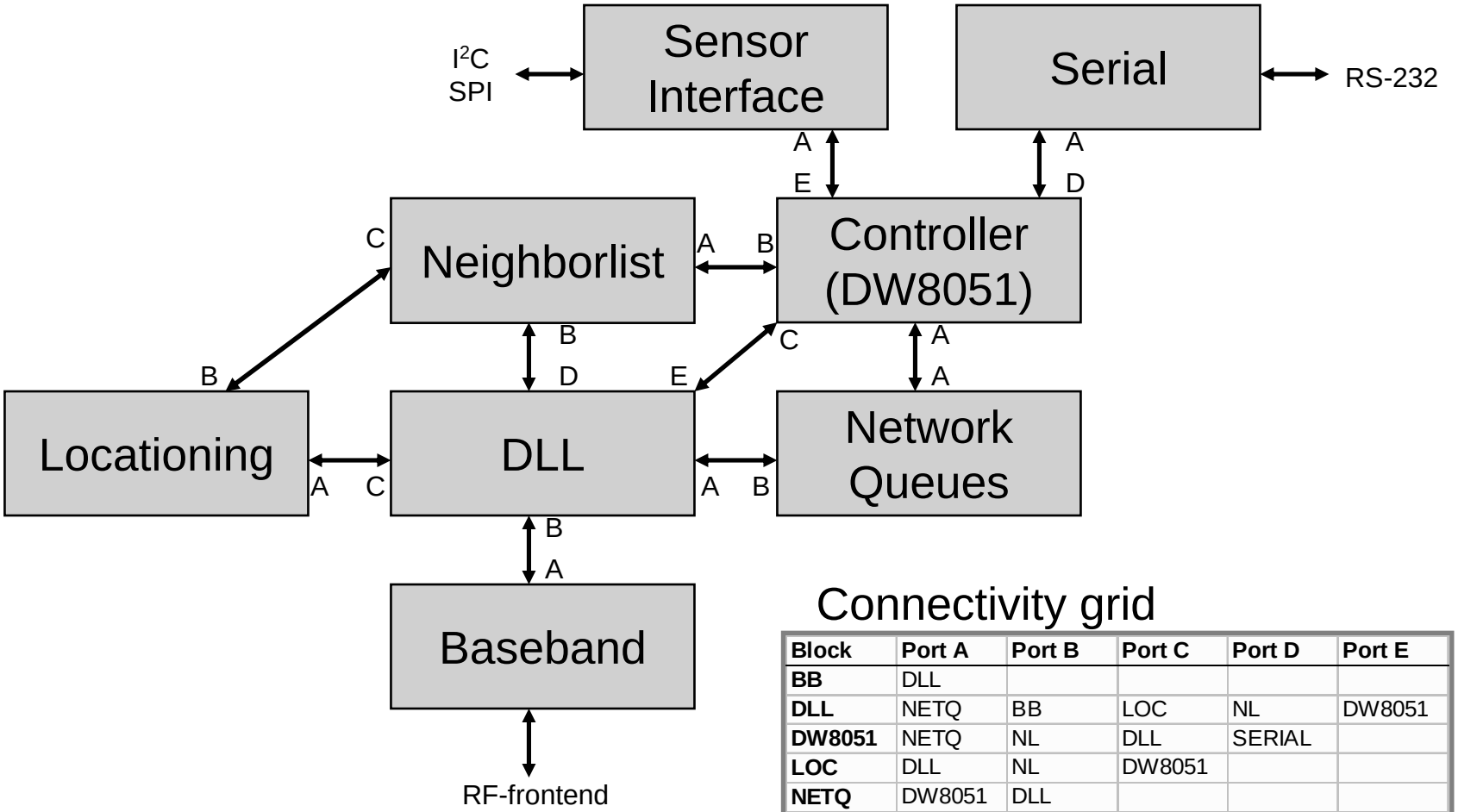
Charms Sub-blocks and Connectivity



Connectivity grid

Block	Port A	Port B	Port C	Port D	Port E
BB	DLL				
DLL	NETQ	BB	LOC	NL	DW8051
DW8051	NETQ	NL	DLL	SERIAL	
LOC	DLL	NL	DW8051		
NETQ	DW8051	DLL			
NL	DW8051	DLL	LOC		
SERIAL	DW8051				

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Power Session Table

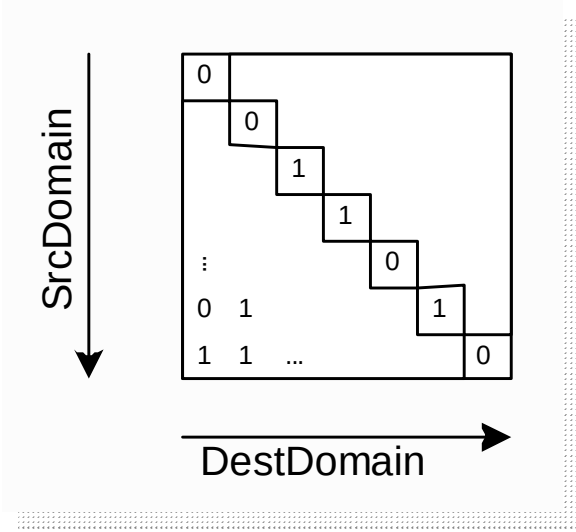
Before a power domain can communication with a neighbor, it must first open a session

Power policy:

A power domain can sleep if…

1) It has closed all its sessions
2) No other domain has a session open with it
3) It wants to go to sleep

Session Table



A ‘1’ in row i means that power domain i has an open a session with another domain

A ‘1’ in column k means that another domain opened a session with domain k

A ‘1’ in entry (i, i) is domain i's self-sleep bit

can_sleep(i) = reduction_nor(row i) and reduction_nor(col i)

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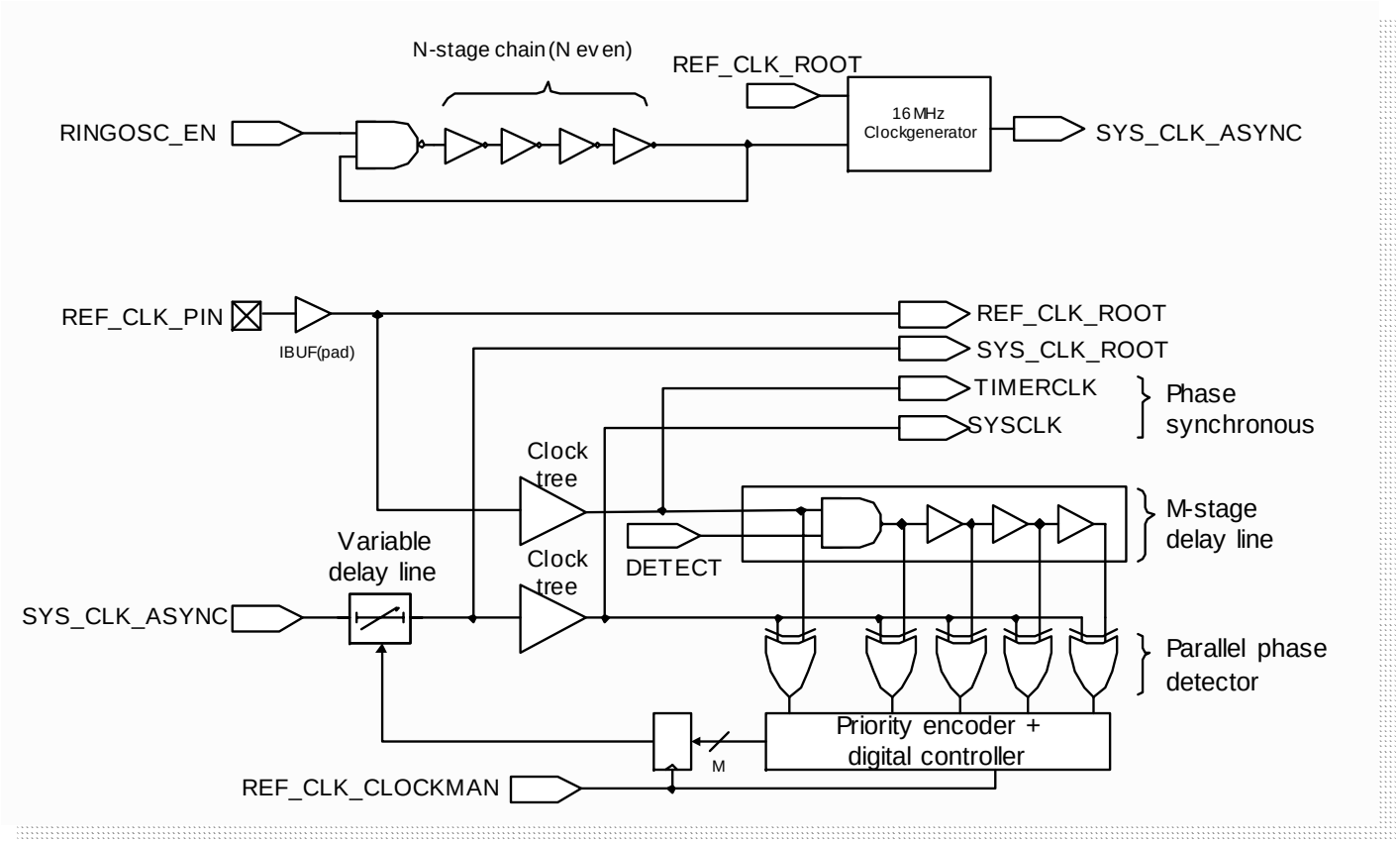
Clocking Subsystem



- **Low frequency external clock (32 KHz)**
- **Generated, switchable, higher frequency clock (16 MHz)**
- **Two clocks are made phase-synchronous using DLL**
- **Control signals are generated by system supervisor**

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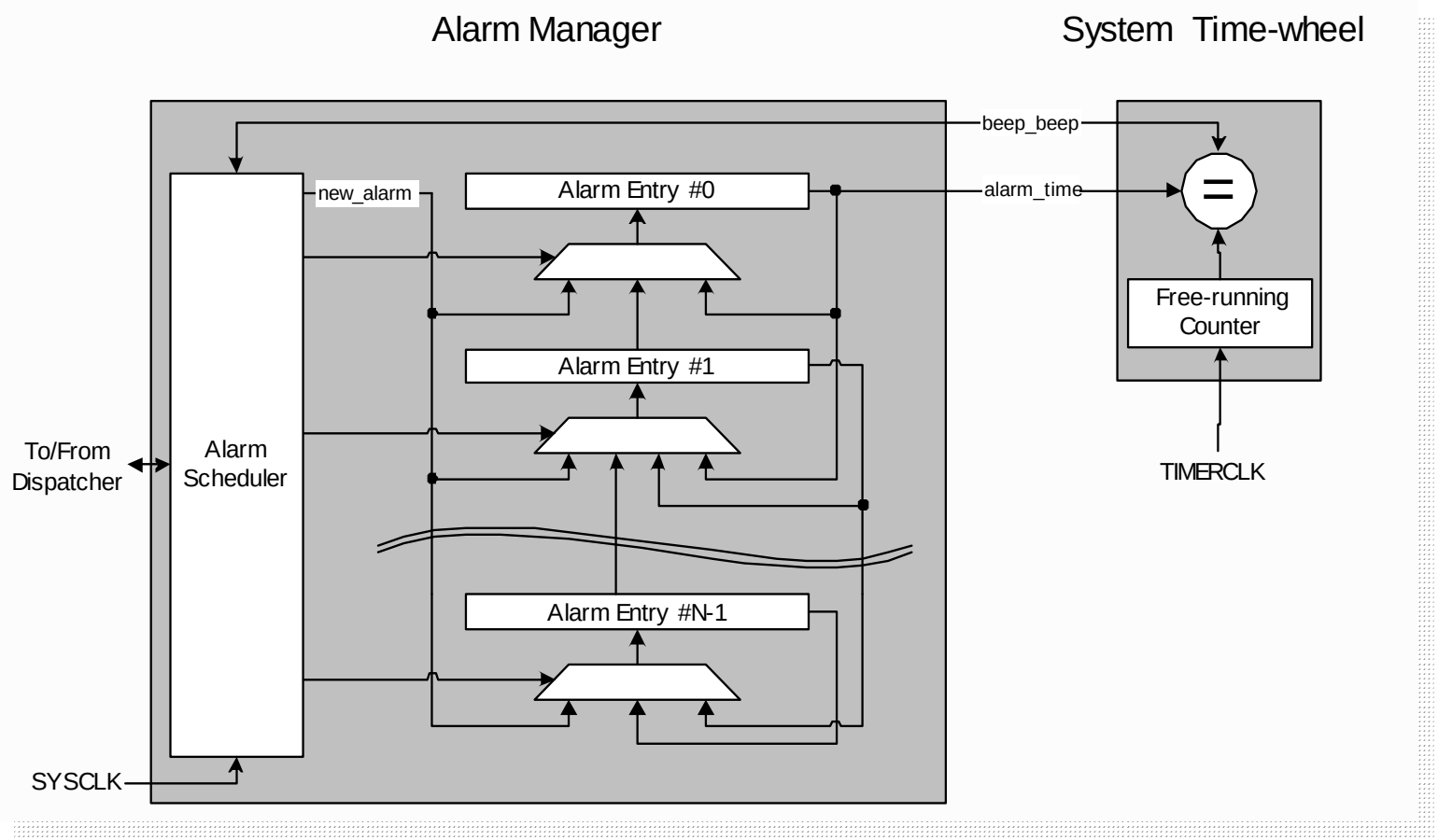
Timer Subsystem



- **Centralized system time-wheel**
  - Blocks schedule wake-up alarms
  - Eliminates other large counters so blocks can sleep
  - Allows power domains to sleep
- **Very low switching activity factor**
  - SYSCLK is disabled during deep sleep
  - Serial (ripple) comparison starting with MSB

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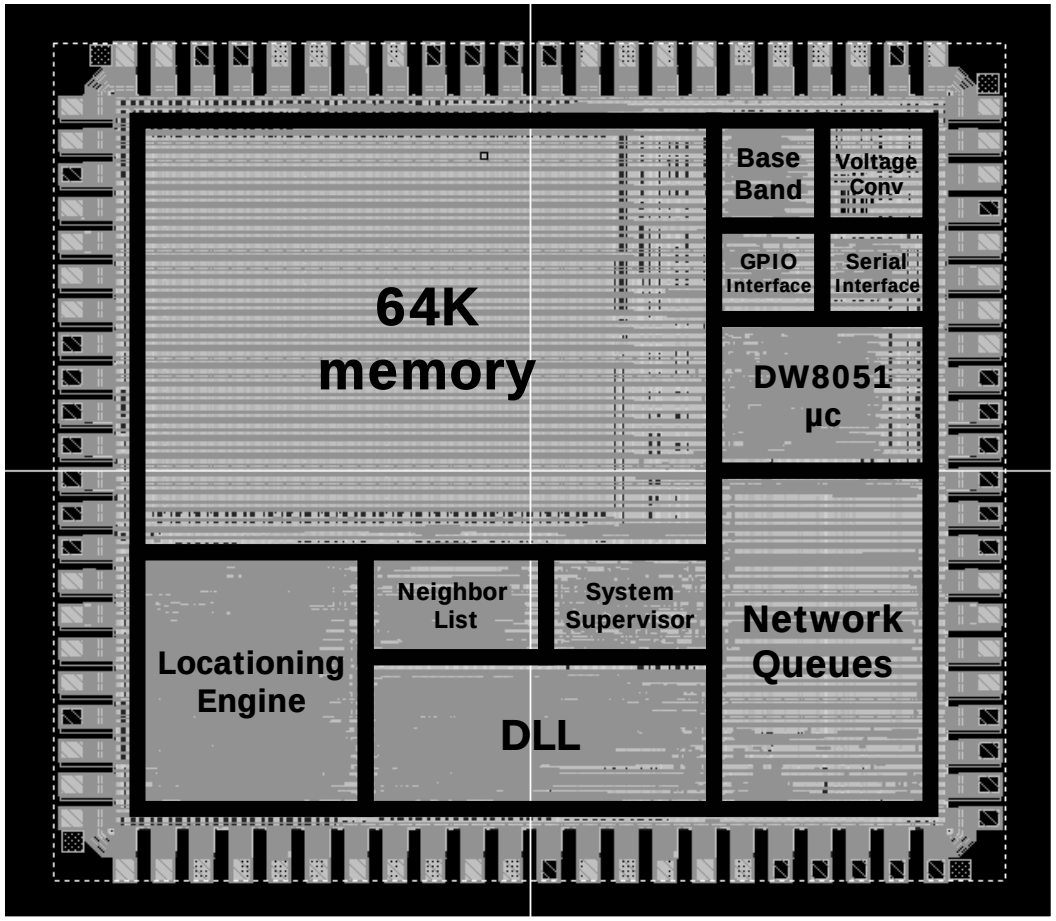
Wireless Sensor Network Protocol Processor



In fab

Technology	0.13µ CMOS
Chip Size	3mm x 2.75mm = 8.2 mm^2
Transistor Count	3.2M
Gate Count	62.5K gates
Clocks Freqs	16MHz(Main), 1MHz(BB)
On Chip memory	68Kbytes
Core Supply Voltages	1V(High) –0.3V(Low)
On_Power	< 1 mW
Standby Power	µWs

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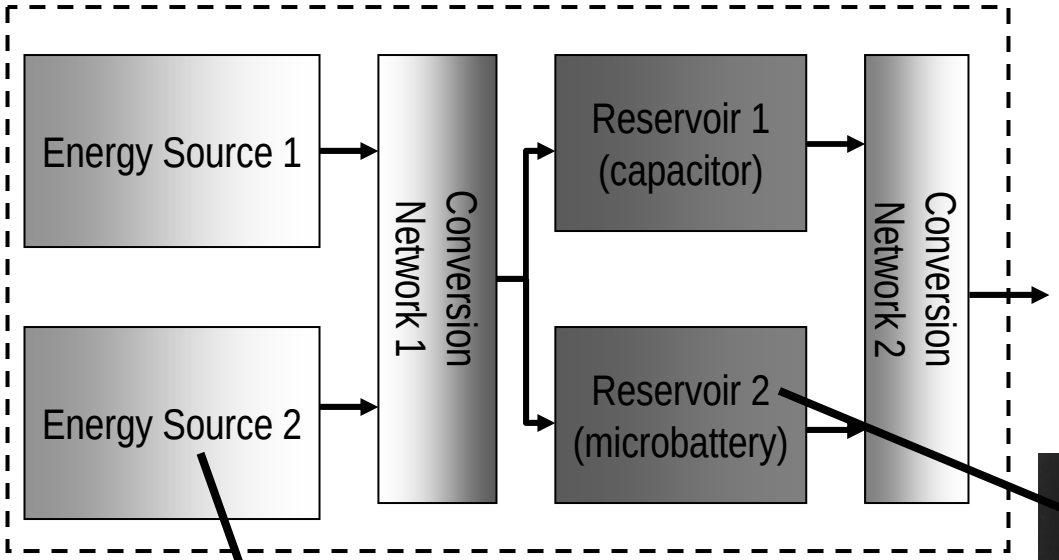
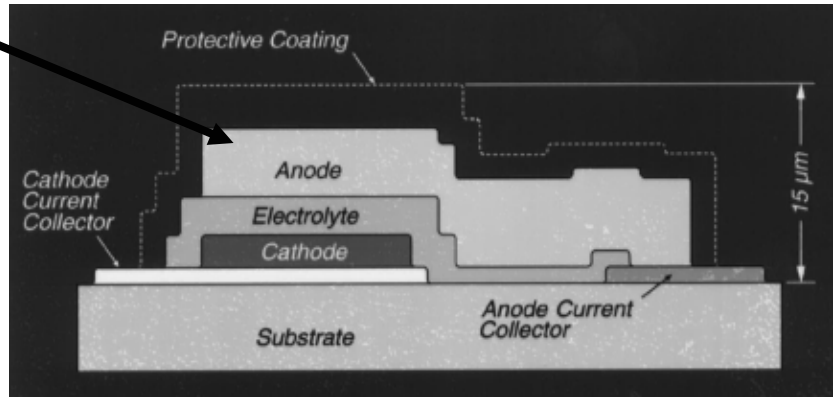
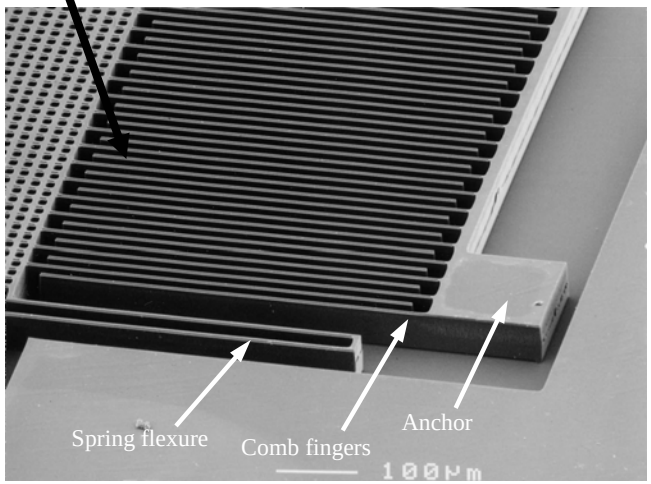
A Longer Term Perspective: On chip power generation and conversion networks



Energy generation and conversion network

Micro-battery





Electrostatic MEMS vibration converters

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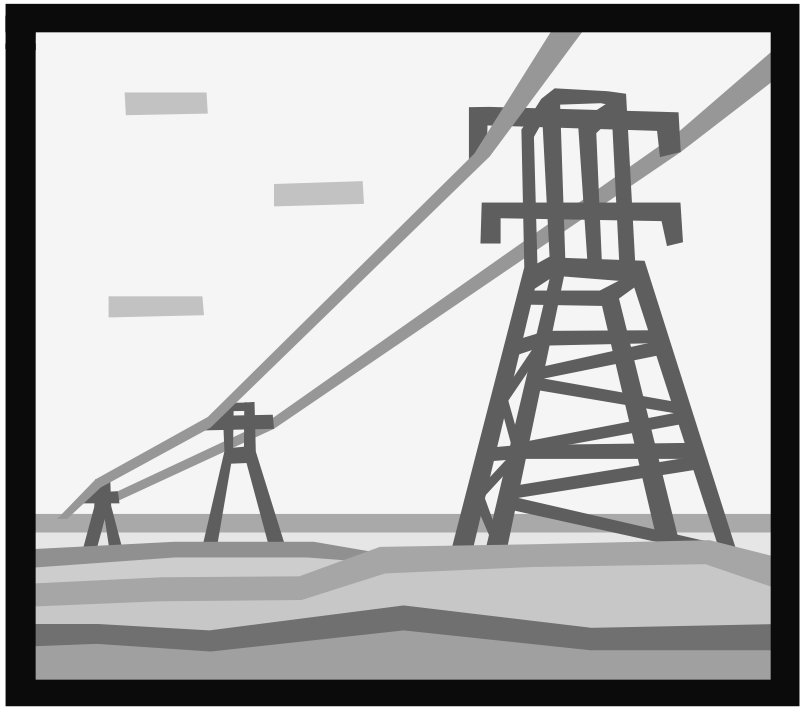
Summary and Perspectives

- **Active and static power management is leading to a fundamental change in the concept of power distribution on a chip**
- **Power domains locally manage and trade-off performance, leakage and process variance**
- **System supervisors giving new meaning to the term OS**
- **Towards “PGE on a chip”**



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