Embedded processors in FPGA's

Dr.-Ing. Yankin Tanurhan

Sr. Director Applications & IP Solutions

Actel Company Overview

- Established FPGA Supplier
  - First product shipped - 1988
  - $150 M in sales in 2003
  - 53 consecutive quarters of Pro Forma profitability
  - Strong balance sheet - $149M cash, no debt
  - 26% R&D spending
  - More than 500 employees
  - Fabless company
  - #1 Flash FPGA supplier
  - #1 Antifuse FPGA supplier

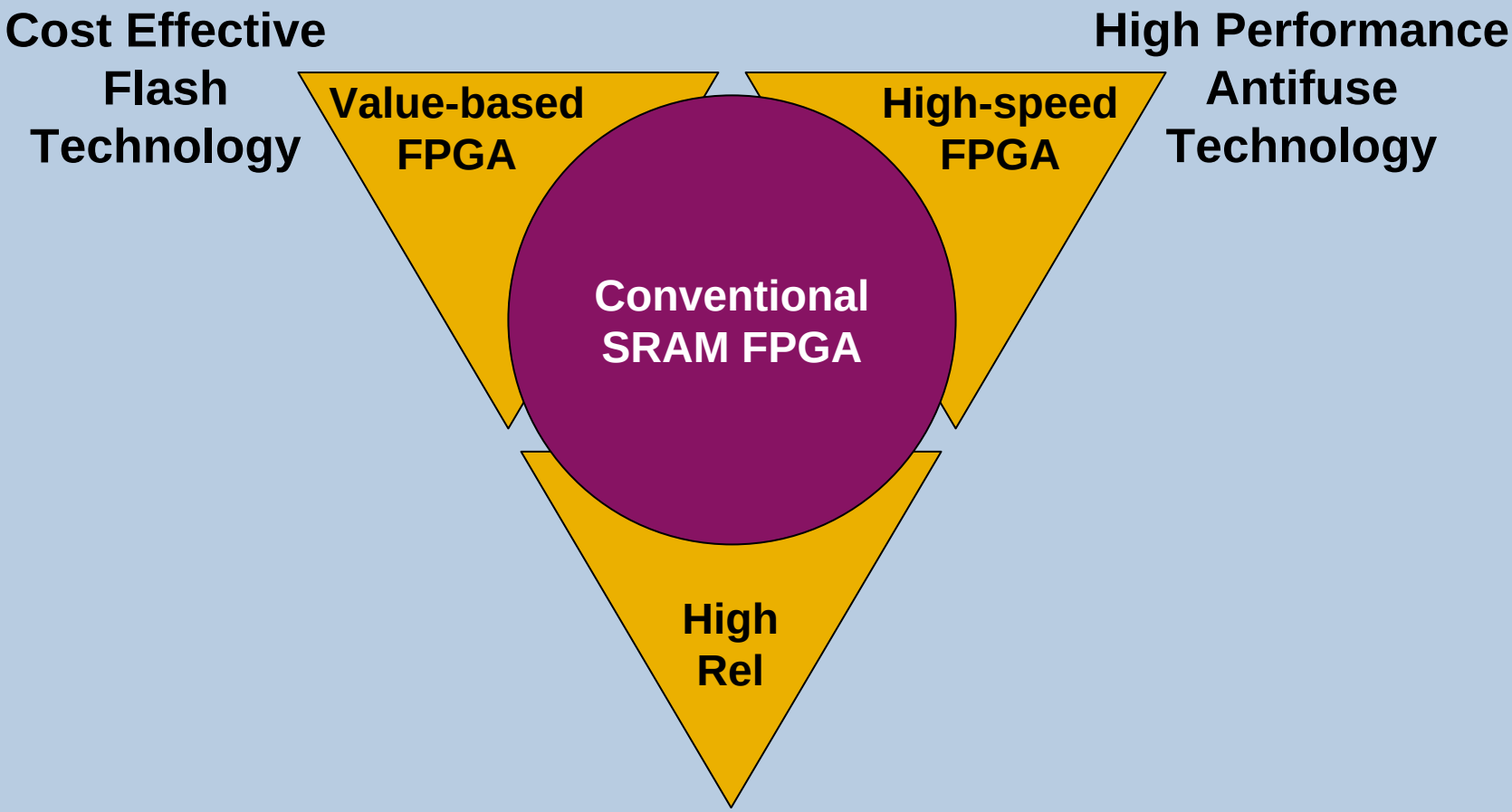
Actel's new 157,000 ft^2 WorldWide Headquarters in Mountain View, Calif.

The Nonvolatile FPGA Company

Agenda

- Who are we ?
- Industry Trends
- Reconfigurable Computing and Target Applications
- Platform
- Design and Development Methodology
- Summary

Actel Strategy & Target Markets



Actel's Key Advantages

Security

- **Tamper-proof, high security, FPGAs prevents reverse engineering, cloning, and over-building**

Power

- **No power-up spike or configuration power, Lowest total system power**

Immune to Firm Errors - High Reliability

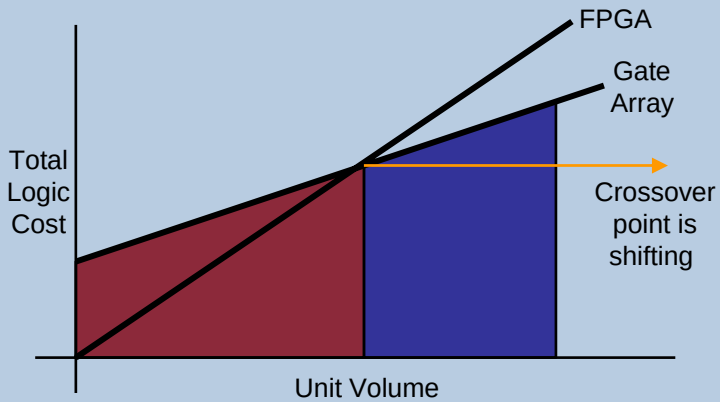
- **All products immune to neutron induced configuration errors**

Total System Cost

- **Single chip solution, live at power-up, lowest total system cost**

Why is FPGA Winning?

- Product life cycles shortening
  - **FPGA reduces development cycle**
  - **FPGA reduces development cost**
- Popularity of reconfigurable systems
  - **FPGA allows field upgrade**
- Increasing FPGA densities
- Lessening process disadvantage
  - **FPGA is a technology driver for independent foundries**



Reconfigurable Computing

- Compute by building an application specific computation circuit rather than executing instructions on a general purpose processor
- Efficient approach for long running or streaming computations
  - **Signal and image processing**
  - **Cellular telecommunication and network processing**
  - **Cryptography**
  - **Pattern matching/recognition**
  - **Neural and automata networks**

RC Fabric options

- Coarse-Grained RC fabric
  - **Array of processors, local storage and fast communication**
  - **Most of the players terminated**
    - **MorphICs, Chameleon etc.**
- FPGA based RC
  - **Programmable fabric that can be dynamically or partially reconfigured**
  - **Past 10 years growth of FPGA speed and density exceeds that of CPU**
- FPGA + CPU based RC
  - **CPU as HardIP**
    - **Physically embedded predefined CPU, not configurable on-chip bus, potential problems with cache and memory management**
  - **CPU as SoftIP**
    - **Choice of the right architecture or architecture combination as needed**

Some Performance Results

FUNCTION	Fastest DSP Processor Available	Just FPGA State of the art
FIR Filter – 256 Taps, Linear phase 16-bit data/coefficients	9.3 MSPS fclk=600MHz	300 MSPS fclk=300MHz
Complex FFT – 1024 point, 16-bit	10µs fclk=600 MHz	1µs fclk=150 MHz
Viterbi Decoding Throughput	500 channels at 7.95 kbps for a total of 3.9 Mbps	~ 155 Mbps
Reed-Solomon Decoding Throughput	4.1 Mbps fclk=600 MHz	10 Gbps fclk=85 MHz

What's Happening in SOC ?

- All logic suppliers (ASIC/ASSP/PLD) are tending toward SOC devices that are specialized for a few applications and targeted toward a small group of customers
- Market share is being concentrated
  - **Leverage customer relationships to gain system expertise**
  - **Large investment needed in IP in order to meet SOC specifications**
  - **Market share brings economy of scale in unit price**
- Time to market is shrinking
  - **Revenue and profit impact from delayed entry is immense**
- Development costs are exploding
  - **Mask sets cost**
  - **Complexity of design**

Design with the Traditional MCU

- Traditional MCUs limited to “standard” designs
  - **Fixed core and peripherals are cost effective and programmable**
  - **But, they are often missing peripherals that add board cost**
- ASICs are expensive and take a long time
  - **Mask and probe NRE cost often over $1M (more for design NRE)**
  - **Even with “design reuse”, seems like re-inventing the wheel**
  - **After an 18- month development cycle, market opportunity gone and company is left with specific inventory**
- Designers need custom parts on demand

Why Soft IP ?

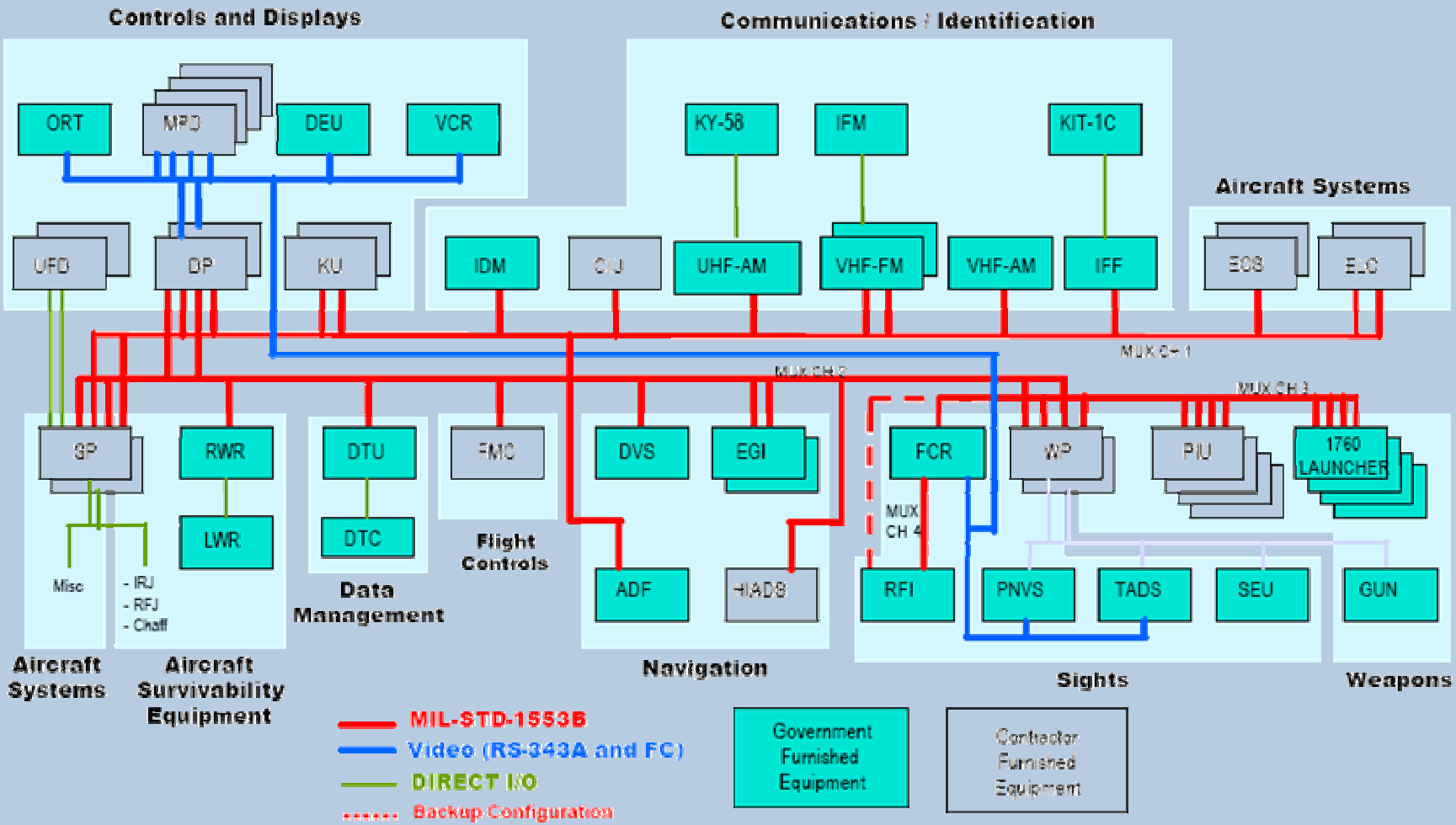
- Opportunity to optimize the array according to applications requirements and domain of computation
  - **Whatever choice you make it will be wrong for some situation !**
- Reduction in power, area and cost
  - **Adaptability brings efficiency**
- Flexible adjustment of the interconnects in size and performance
  - **Bottleneck is in the interfaces and connectibility and whatever choice you make …**
- Multiple task specific processors can be integrated
  - **Instruction set can be extended as needed**
  - **Still choices for a set have to be made to have a standardized design flow**

Platform-Based Design

- An FPGA platform saves time
  - **Integrated and pre-verified**
  - **Configurable with pre-built IP blocks**
  - **Simple to add logic blocks**
  - **Readily available with low-cost development tools**
  - **Immediate and customer-specific**
  - **Includes rapid, inexpensive prototyping**
- But,
  which MPU architecture is the “right” one?

Typical Application

Apache Longbow Architecture



We started with the 8051

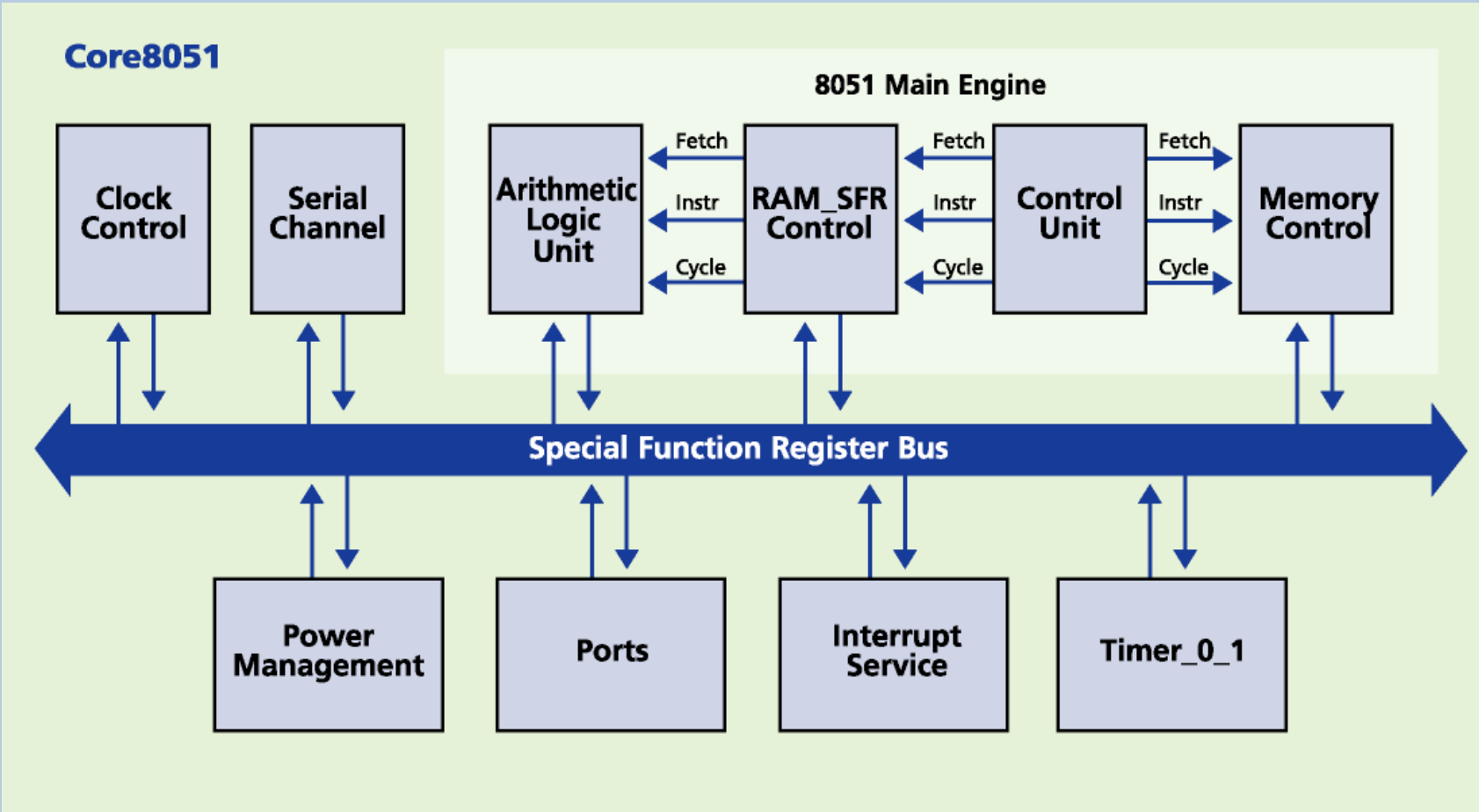
- The 8-bit market is huge and continues to grow
  - **Over 3 billion units per year and growing**
- New applications still use 8-bit
  - **Industrial, military, aerospace, automotive, consumer and communications applications often utilize efficient 8-bit processing**
- 8051 still owns 23% of the 8-bit market
  - **Over $900 million and 650 million units per year**
  - **Installed base in the billions**
  - **There are over 30 thousand 8051 code developers**

Core8051 Infomercial

Core8051 + Actel FPGA

- **100% ASM51 Code Compatible**
- **CPU with Boolean processor**
- **13 interrupts with 4 priority levels**
- **2 timers**
- **Programmable Serial Channel**
- **Four 8-bit I/O ports**
- **1 clock cycle per instruction**
- **Embedded memory available**
- **Removable OCI block**
- **Creates a full-featured low-cost 8051**
- **As low as 35¢/MIPS**

Core8051 Block Diagram



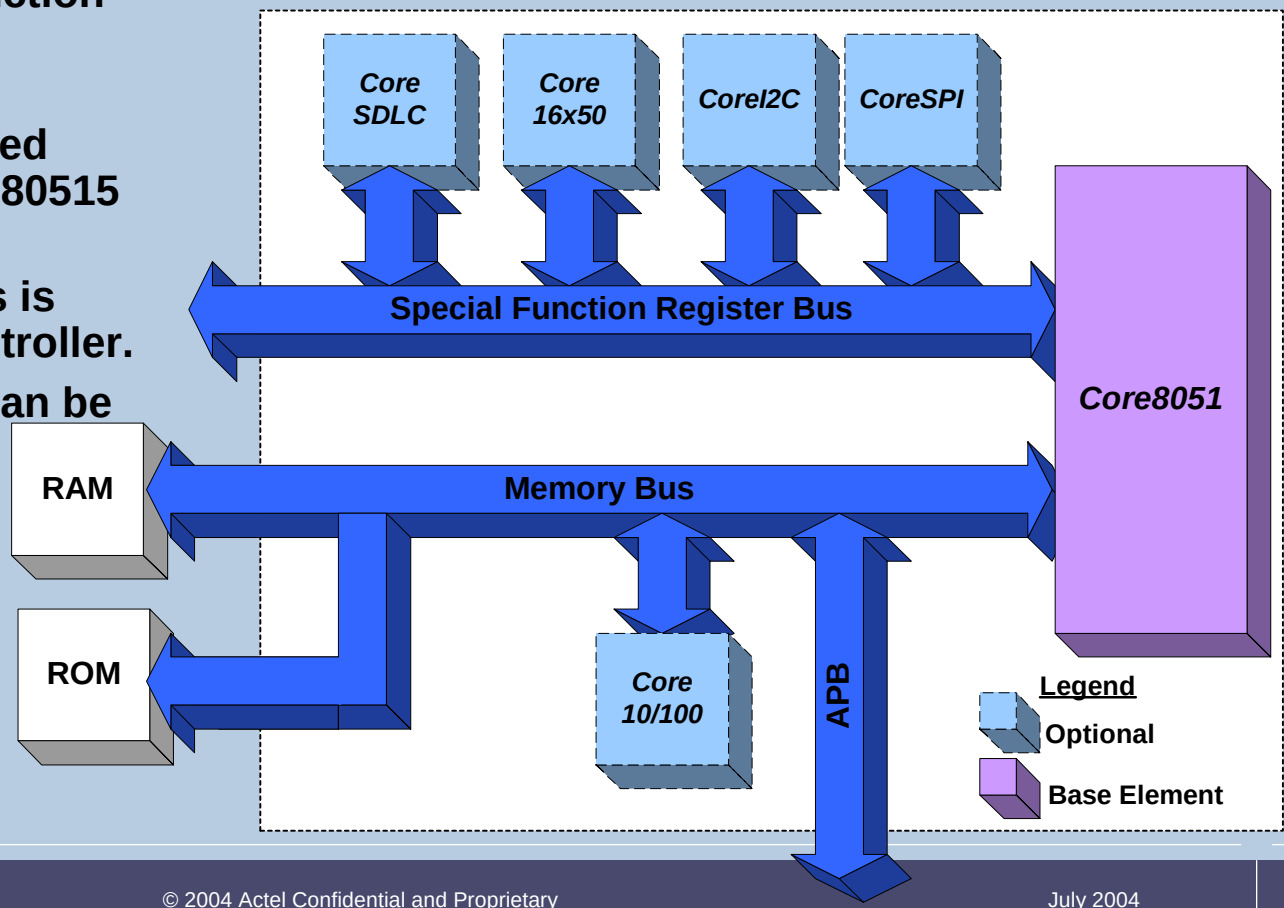
Platform8051

The FPGA as an "Embedded System Platform"

- **Simplifies system design and reduces cost**
  - **Uses current Actel FPGAs, design tools and IP**
- **Pre-verified platform**
  - **Saves time and allows quick expansion**
  - **Peripherals verified individually and platform verified as a whole**
- **FPGAs allow customization without NRE and time delays**
  - **Customer focuses on adding unique IP**
  - **Eliminates development time of ASSPs and ASICs**
  - **Including custom radiation-tolerant and radiation-hardened designs**
- **Platform is configurable**
  - **Design with one core, a group of cores or entire platform**
  - **Delivered in one day over the Web**
- **Development board allows fast prototyping**

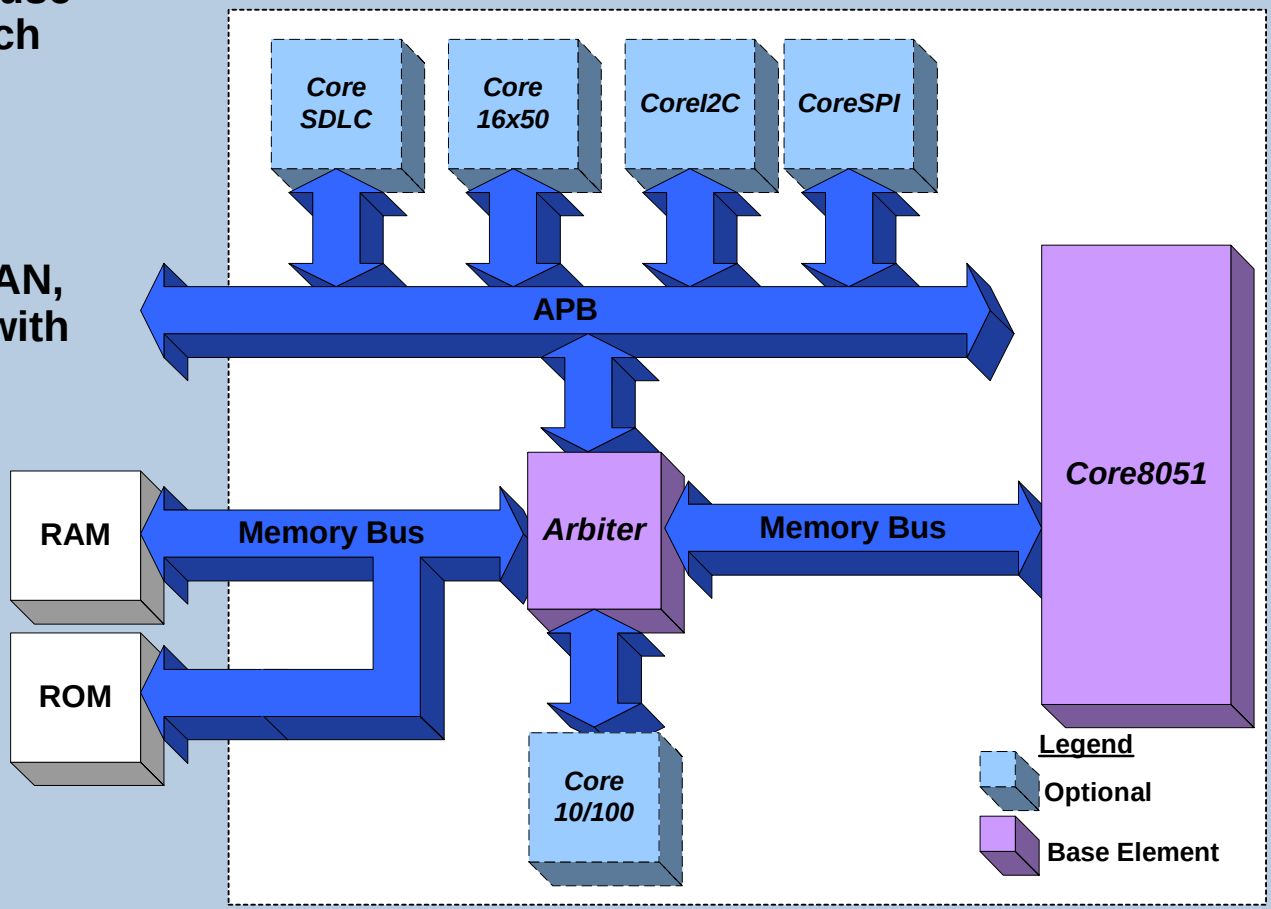
Platform8051 (Option1)

- Solution 1 represents the typical 8051 system.
- The SDLC, I2C, CAN, SPI peripherials are connected to the CPU using dedicated 8051 SFR (Special Function Register) bus.
- Both RAM and ROM memories are connected directly using native R80515 memory bus.
- The same memory bus is also used by MAC controller.
- The user peripherals can be connected to the APB interface.



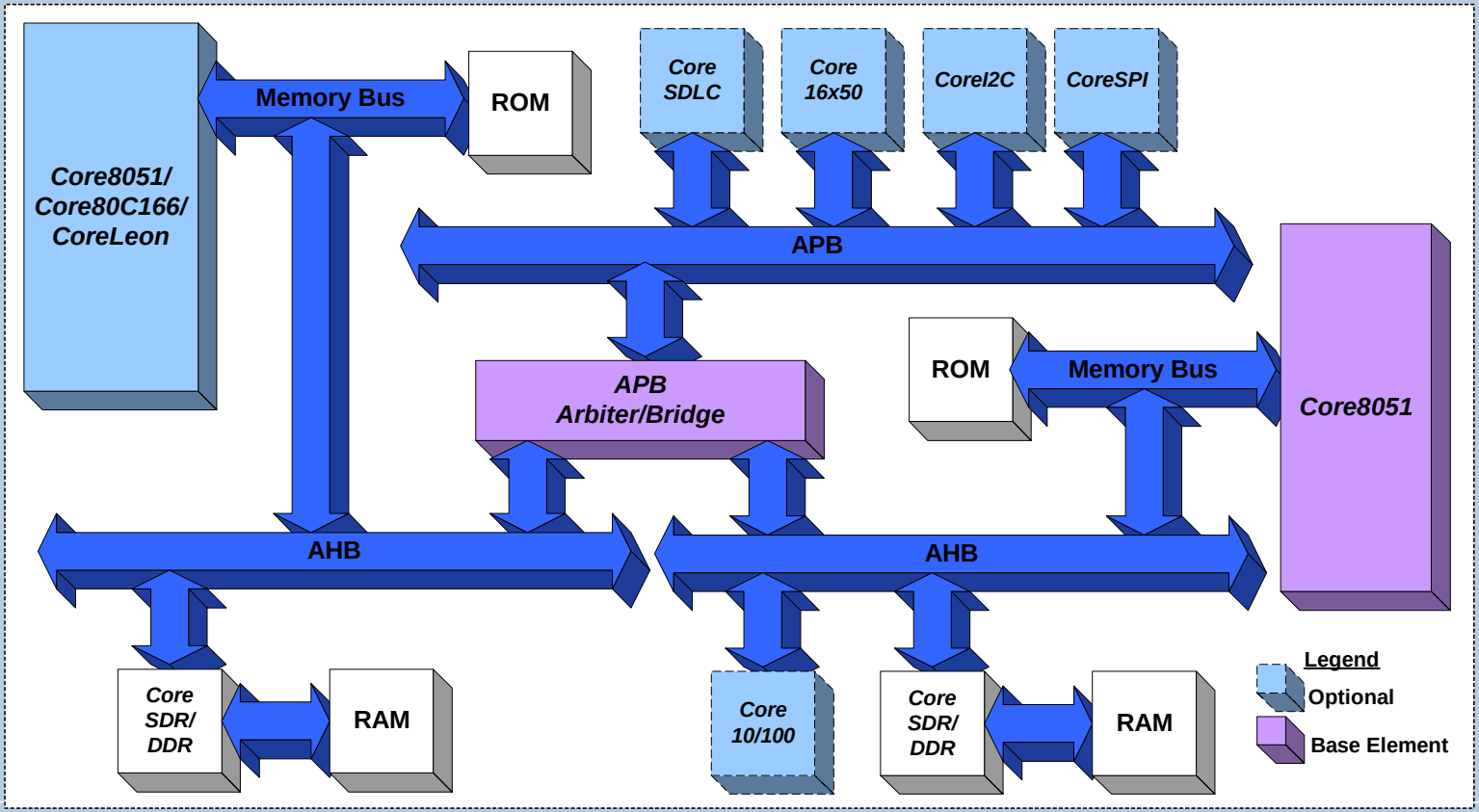
Platform8051 (Option2)

- Solution2 is the modified version of Solution1.
- The difference is that this system does not make use of native SFR bus. Which makes the architecture more flexible for CPU upgrades.
- All key peripherals, including SDLC, I2C, CAN, and SPI communicate with CPU only via APB bus wrappers.
- This solution makes configuration of the system easier, but also reduces performance.

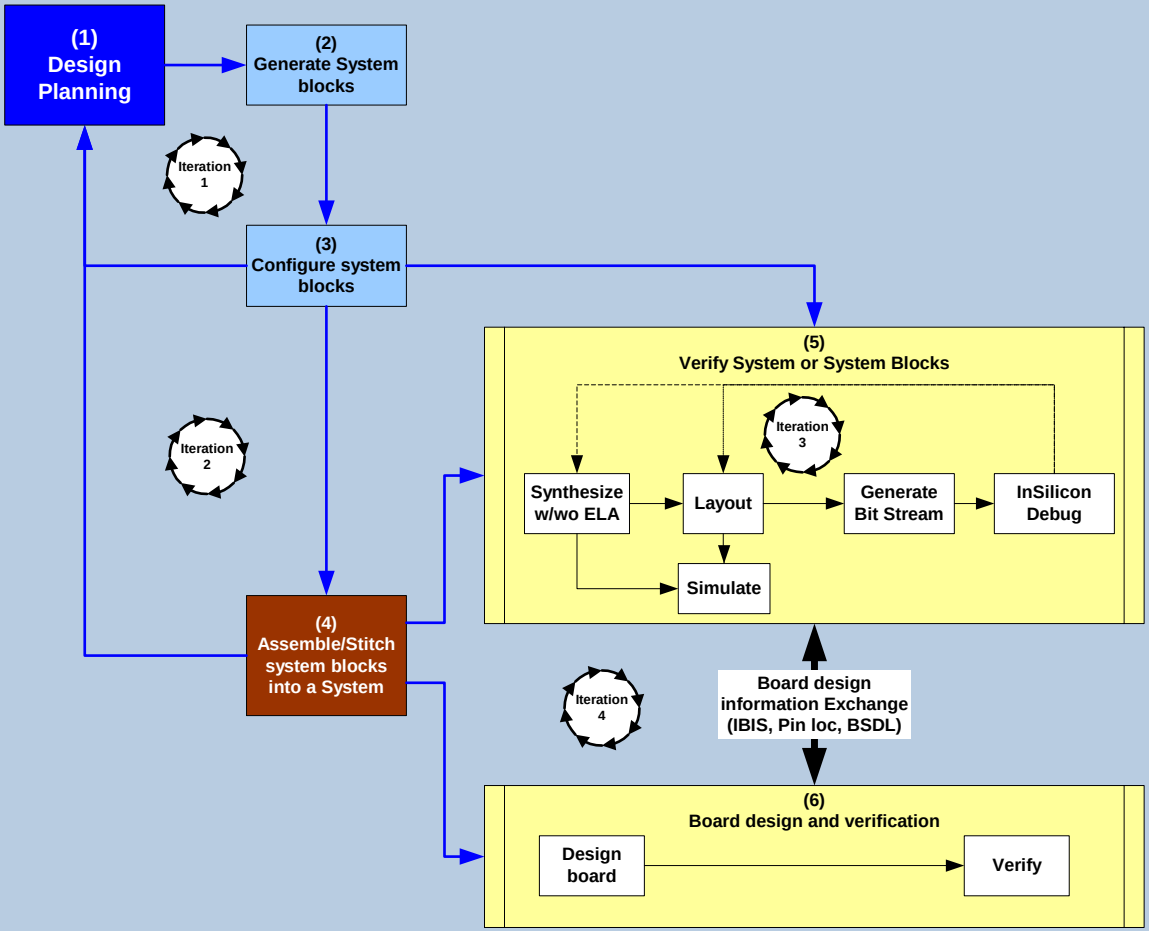


Platform8051 (Option3)

- **The Solution 3 is the MPSOC Platform which contains a family of AMBA-based reusable peripheral IP blocks required for advanced SOC (System-on-a-chip) designs with microprocessor core.**
- **It contains all the functionality for a typical SOC application including components such as bus bridges to AHB, APB, memory, serial units and ethernet controller.**



System level design flow



- Focus now on system
  - Build in pieces
  - Validate pieces
  - Integrate incrementally
  - Auto stitch
  - Validate incrementally
  - ** Start from a reference design, then iterate
- Key components
  - Generation of systems
  - Assembly of systems
  - Incremental changes
  - Debugging
  - Board level links

Platform8051 Development Kit

- Board
  - **APA-600 FG676**
  - **Modular with daughter card area**
- Demonstration Design
  - **Web server application**
  - **Core8051 and Core10/100**
- Software
  - **Libero v6.0 Platinum**
  - **Keil IDE**
  - **TCP/IP Stack**
- Optional FlashPro Lite JTAG connector and programmer

Debugging/Validation

- Hardware Software Co-Verification
  - **Software - OCI logic build into the 8051**
    - **External GUI can access via JTAG link and FlashPRO**
    - **Load & Execute Code, single step, read/write registers and memory**
  - **Hardware – CLAM, Logic Analyzer function within the FPGA**
    - **External GUI can trace internal activity via JTAG link**
    - **Logic Analyzer added inside the FPGA**
- Features
  - **Triggers**
    - **Up to 4 Hardware triggers supported**
    - **Trigger on Code read/write, Code Execution, External Data read/write, SFR read/write, Internal Data read/write**
  - **Trace**
    - **History of most recent branch points**
    - **Software execution flow can be reconstructed**
    - **Trigger(s) can start/stop Trace buffer writes**
  - **32 Channel 100MHz logic analyzer function**

Summary

- FPGA is the coming platform for heterogeneous system design
- We introduced an 8-Bit MPSoC platform which is cost efficient and fast
- Debugging is still an art
- 16 and 32 Bit solution to follow