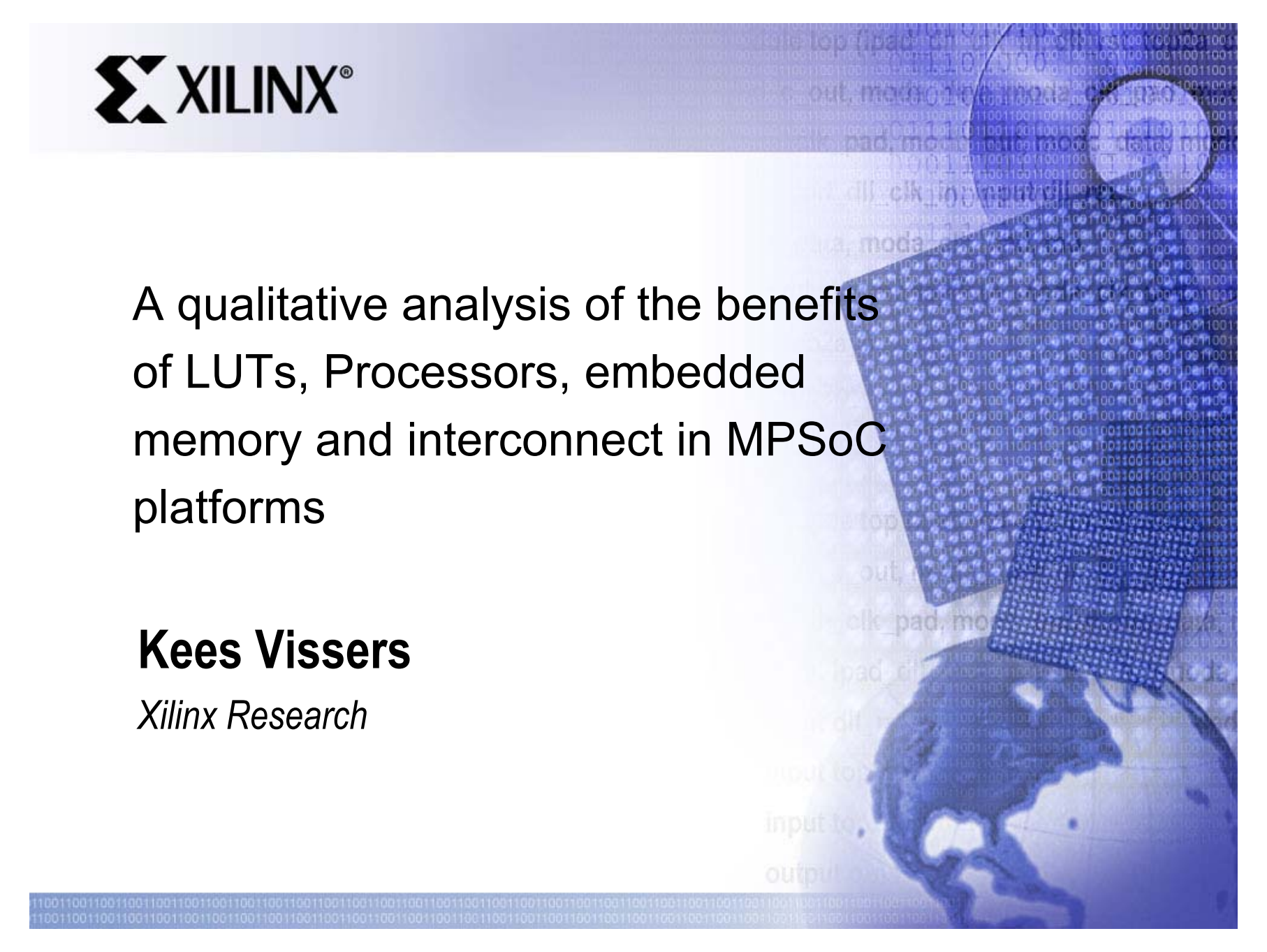


A qualitative analysis of the benefits of LUTs, Processors, embedded memory and interconnect in MPSoC platforms

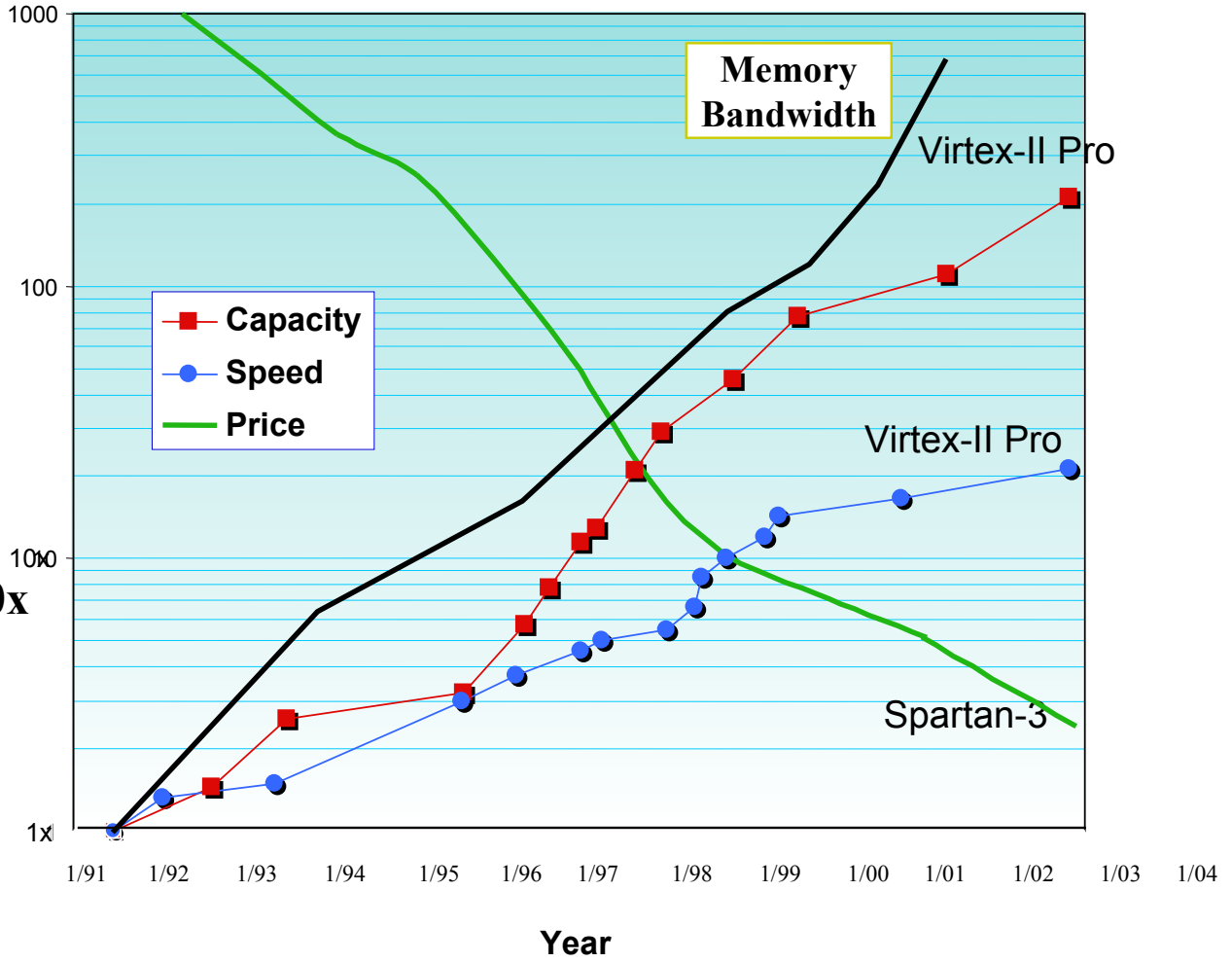
Kees Vissers

Xilinx Research

OUTLINE

- Historical Perspective
- Conventional FPGAs
- Applications and Programming
- Future Directions

FPGA, the last 10 years



Price: 300x

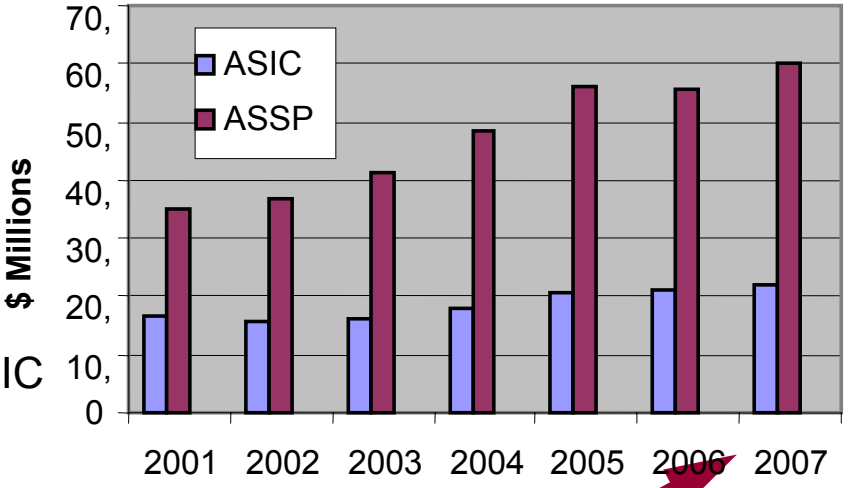
Speed: 20x

Capacity: 200x

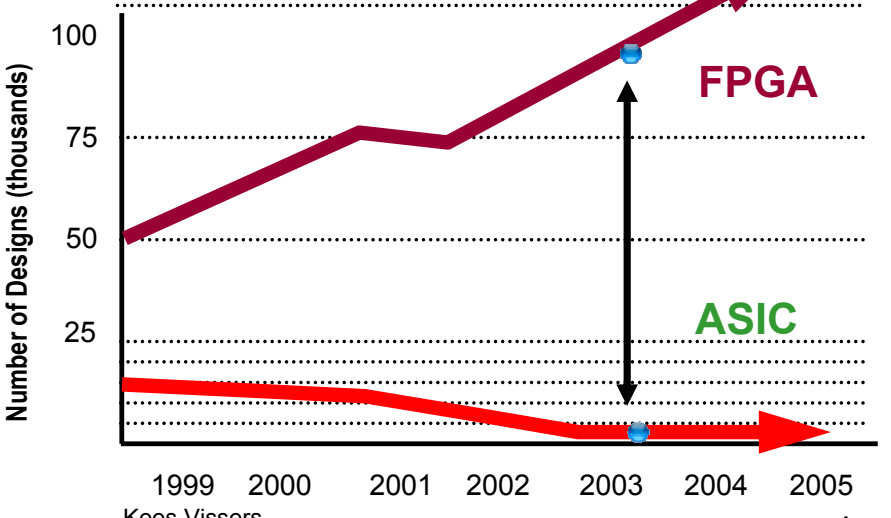
4000x- 6000x customer value!

The market

→ 2007 ASIC/ASSP = 80 B$
→ NRE = 30M$
→ R&D = 20% revenue
→ Revenue = 150M$
→ ~500 successful ASSP/ASIC



- Design Starts



The ultimate solution

- Glueless interfaces
- Can handle all external memory, e.g DDR RAM, QDR RAM, SRAM
- Can do all the processing
- Is fully programmable/reconfigurable in all aspects: I/O, function, memory architecture, signal level, etc

ONLY Platform FPGAs can do this.

Processors: Itanium 2 6M

- 130 W (107 W typical)
- 3 Levels of Cache: 16k + 16k, 256K, 6M
- 130nm
- 1.5 GHz
- 95 percent of the 7,877 pins are for power
- 1,322 Specint base2000 for a single processor!
- Next generation: 1.7GHz and 9MByte cache!

Ref: IEEE Micro April 2004, vol. 24, Issue 2, pp. 10-18: ITANIUM 2 PROCESSOR 6M: HIGHER FREQUENCY AND LARGER L3 CACHE, Rusu et. al, Intel.

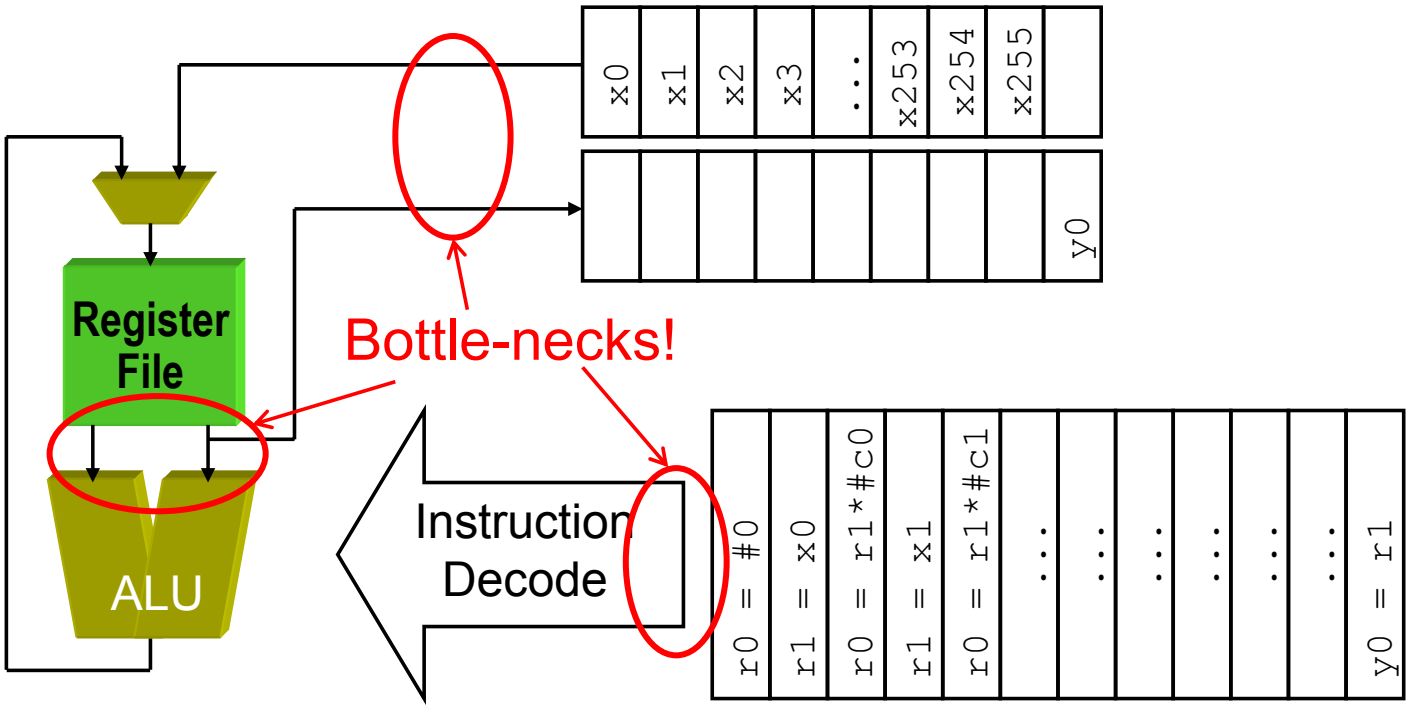
Processors: DSP

- TI C6414: 2 levels of cache
- Philips PNX1500 (Trimedia core): 2 levels of cache
- Often specific DMA, Bus architecture and optimized main memory architecture: does not easily fit the C programming paradigm.

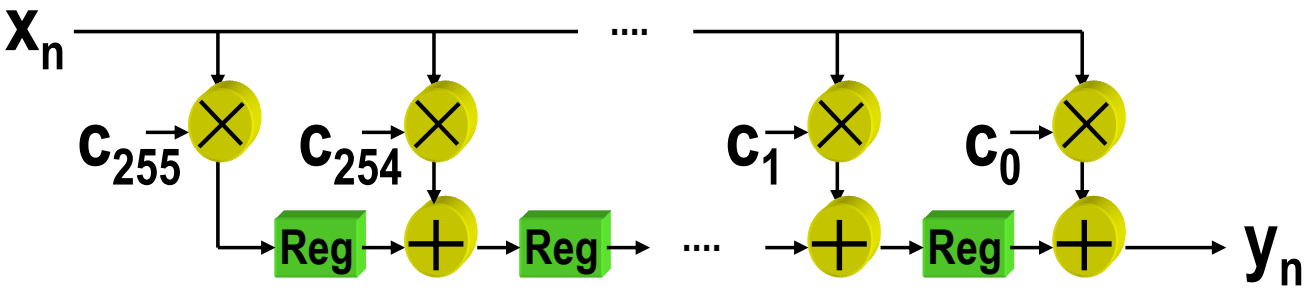
Conclusion: the memory model is a problem

A Von Neumann-style Computation Example

256 Tap FIR Filter $y_n = \sum_{K=0}^{255} c_k x_{n-k}$



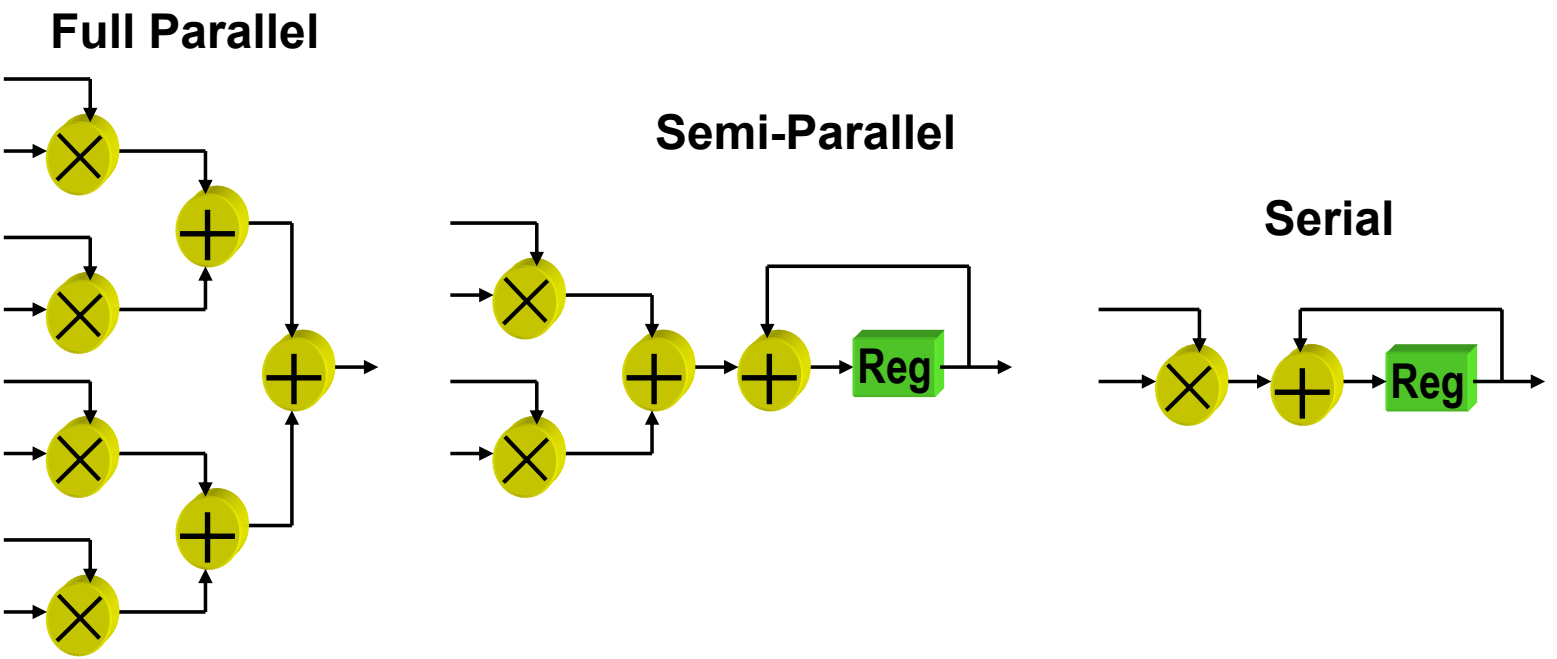
FIR Implementation in RC



- For highest speed, use as many compute elements as problem allows.
- Capable of producing an output sample in one "instruction cycle".
- Call this "Spatial computing". (see DeHon)

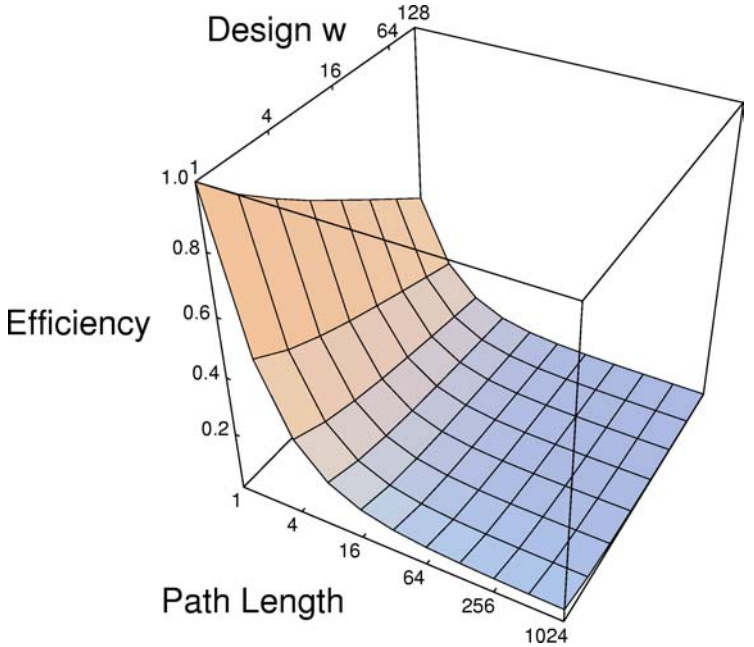
Customizing Architecture in RC

- Tailor a solution to optimize throughput, precision and cost

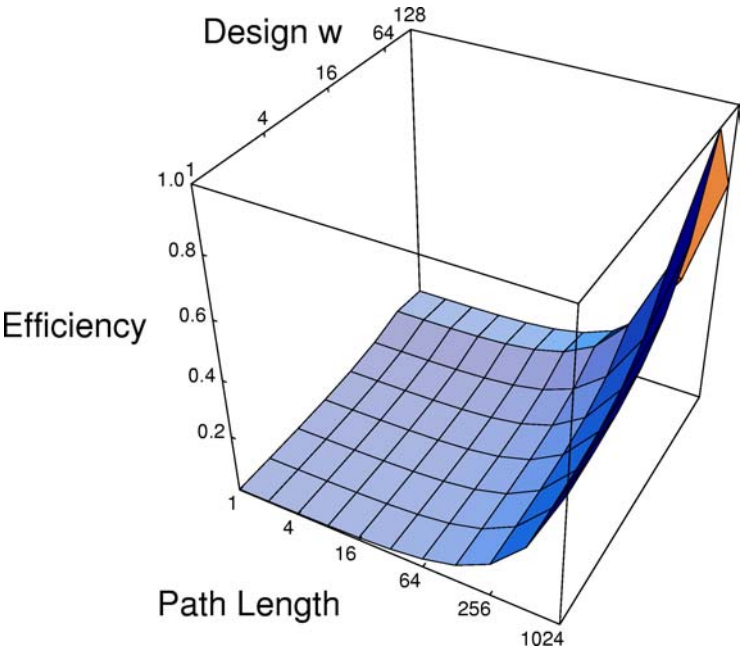


Architectural Efficiency
Spatial vs. Temporal Computing

FPGA (c=w=1)



"Processor" (c=1024, w=64)

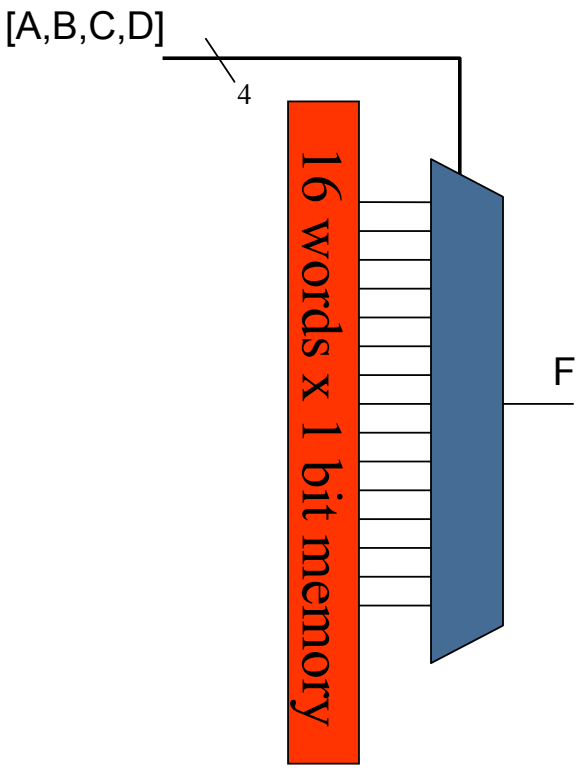


Figures courtesy of André DeHon, California Institute of Technology

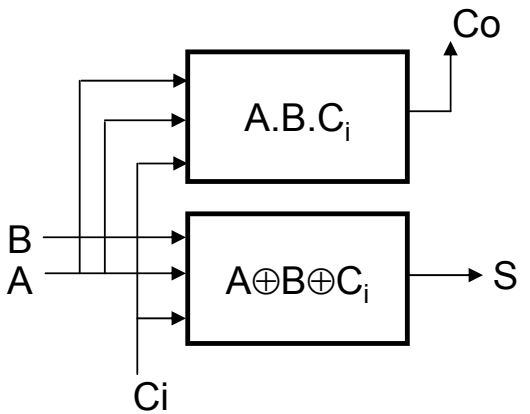
OUTLINE

- Historical Perspective
- Conventional FPGAs
- Applications and Programming
- Technology Impact
- Financial Impact
- Future Directions

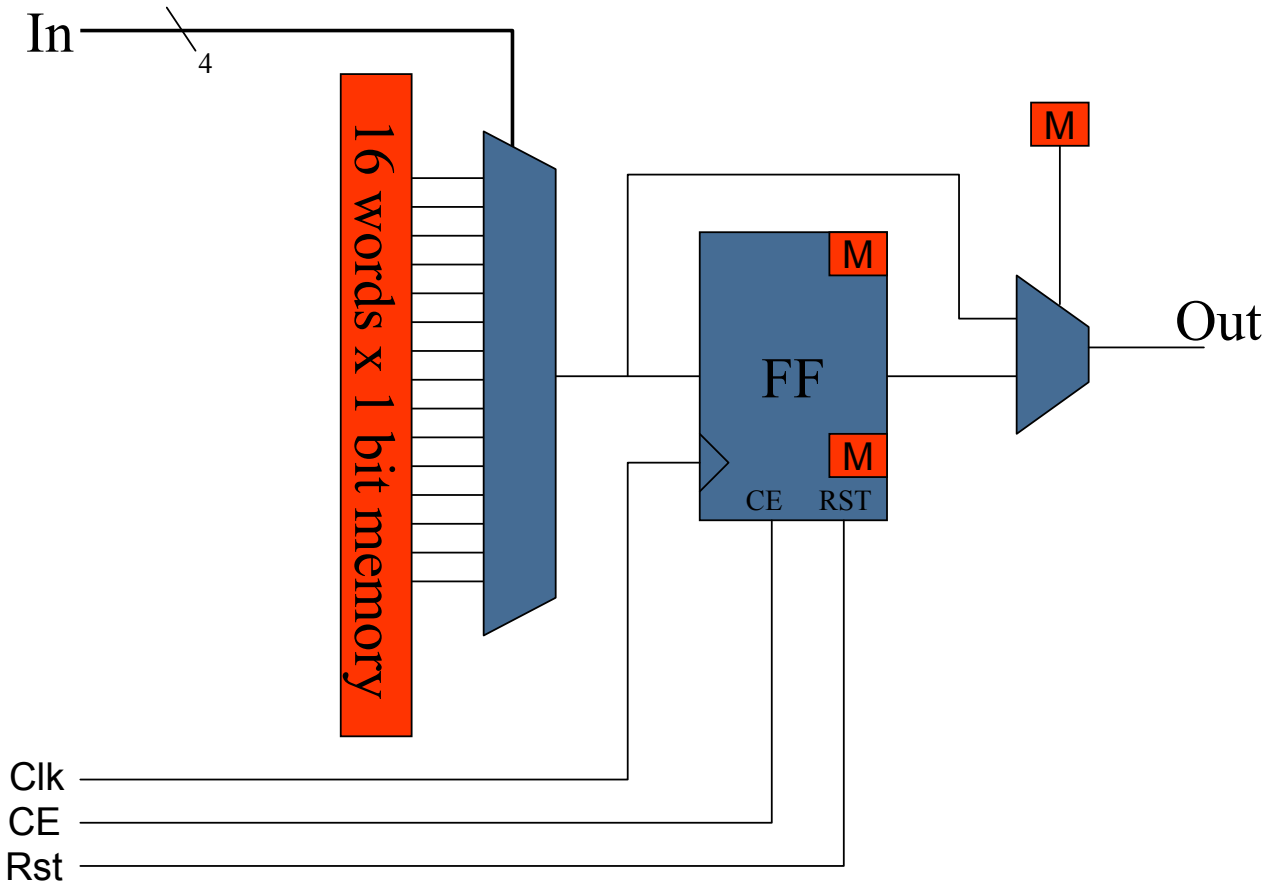
Building an FPGA: Logic First



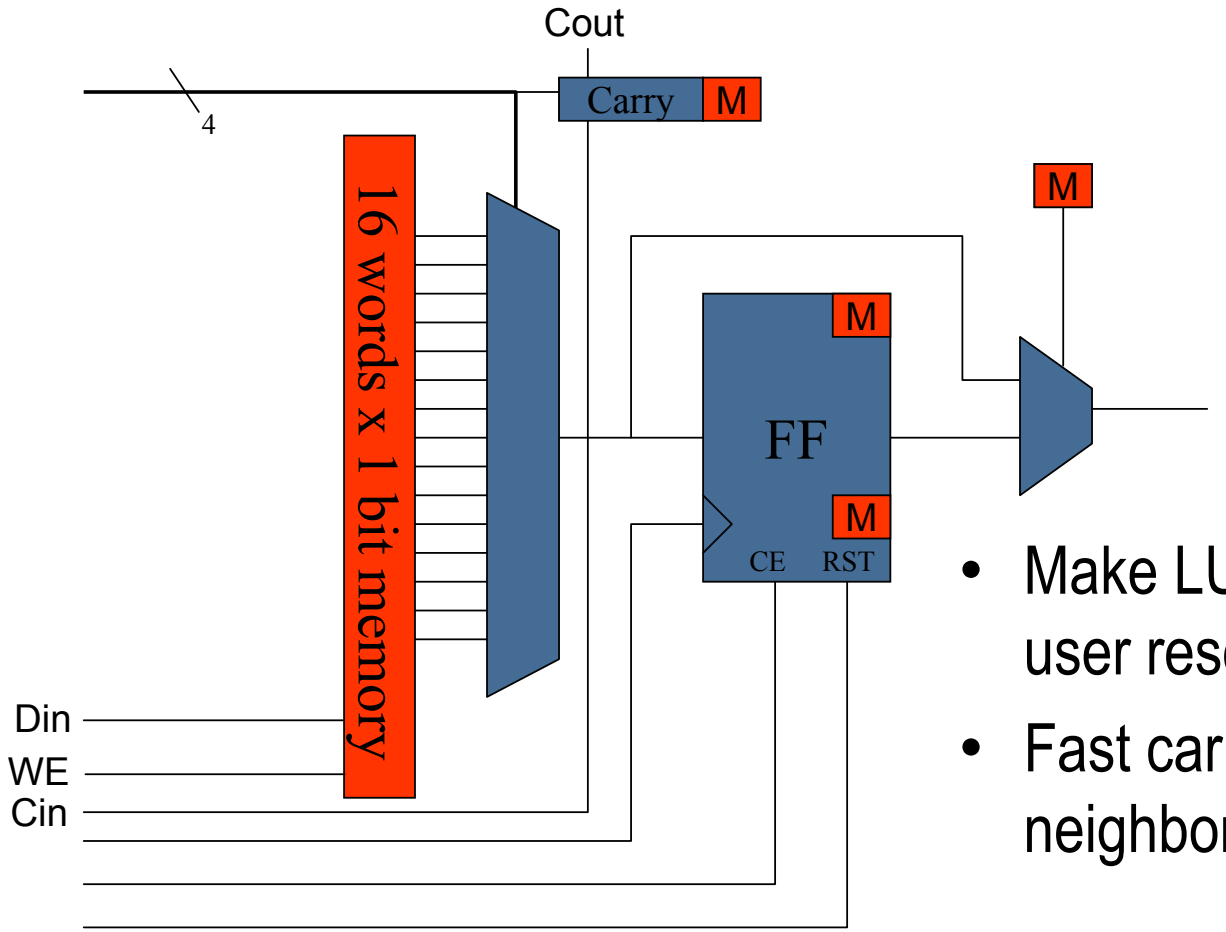
- A 4-input lookup table (LUT) can implement any function of 4 inputs.
- For example, a 1-bit adder needs 2 LUTs:



Add FF to make a Logic Cell

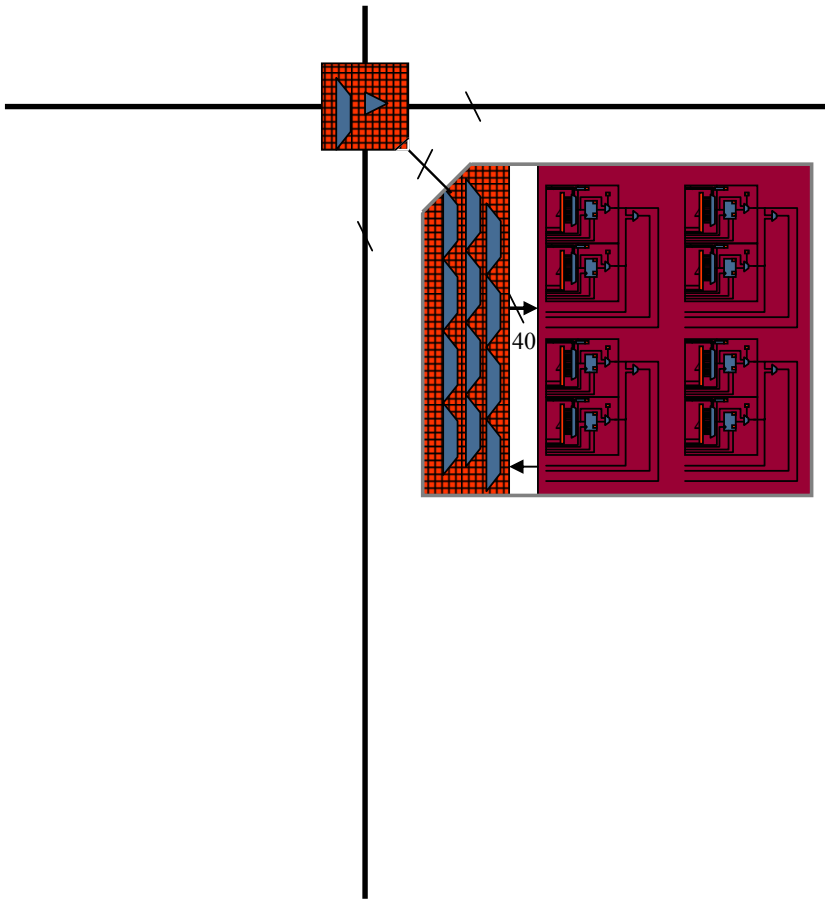


Arithmetic, Distributed RAM



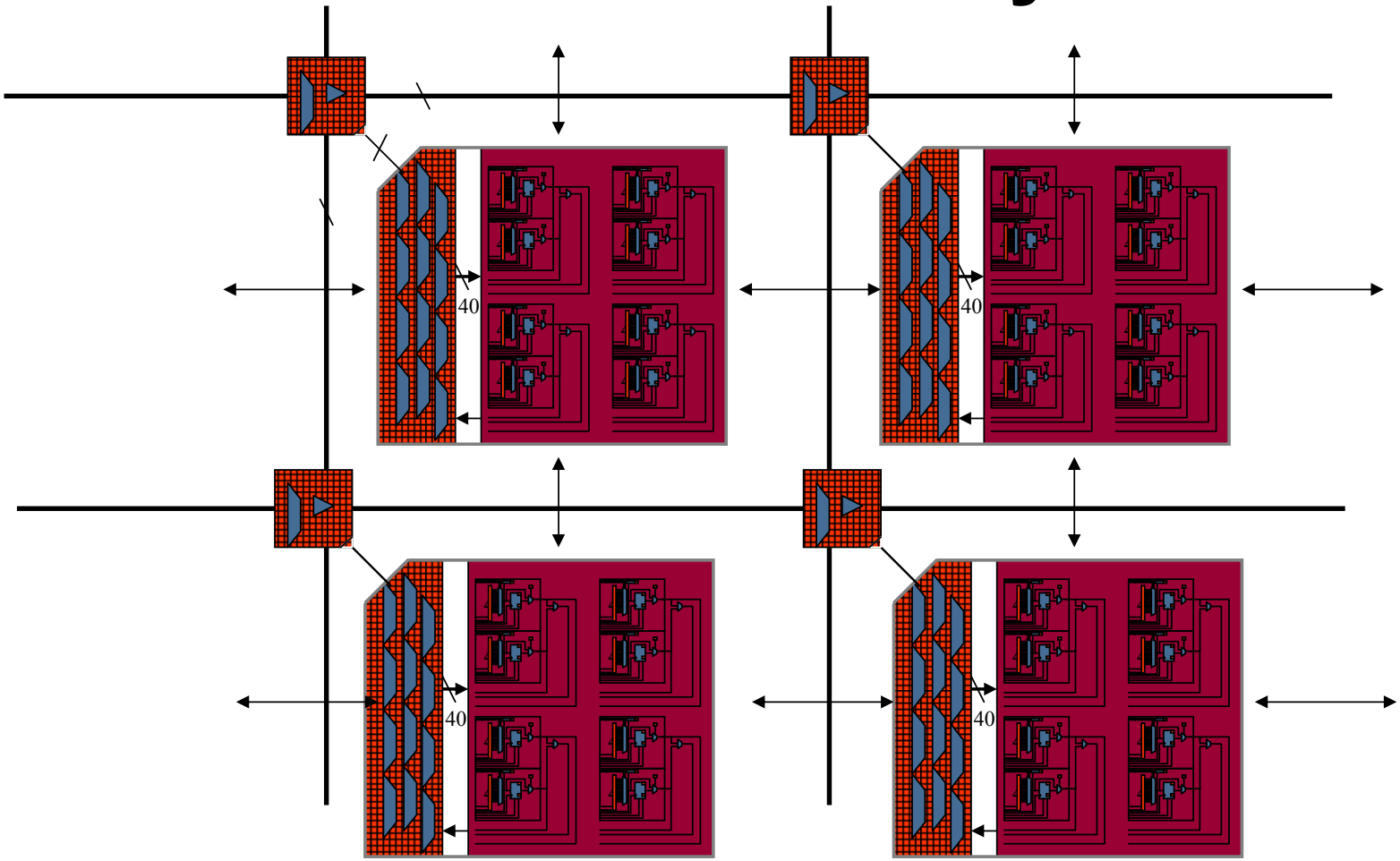
- Make LUT RAM a user resource.
- Fast carry ripple to neighbor.

Add Interconnect



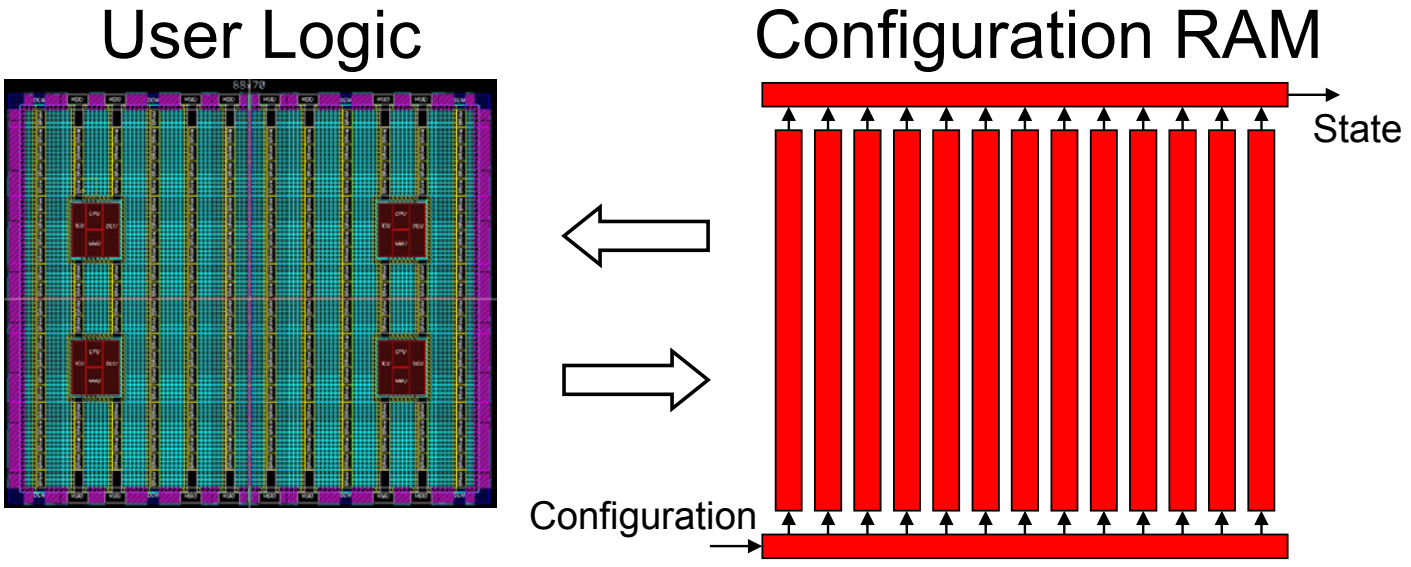
- Group logic cells to reduce overhead.
- Add H, V routing channels with switchboxes.
- Add input, output MUXing between logic and routing.

Build an Array

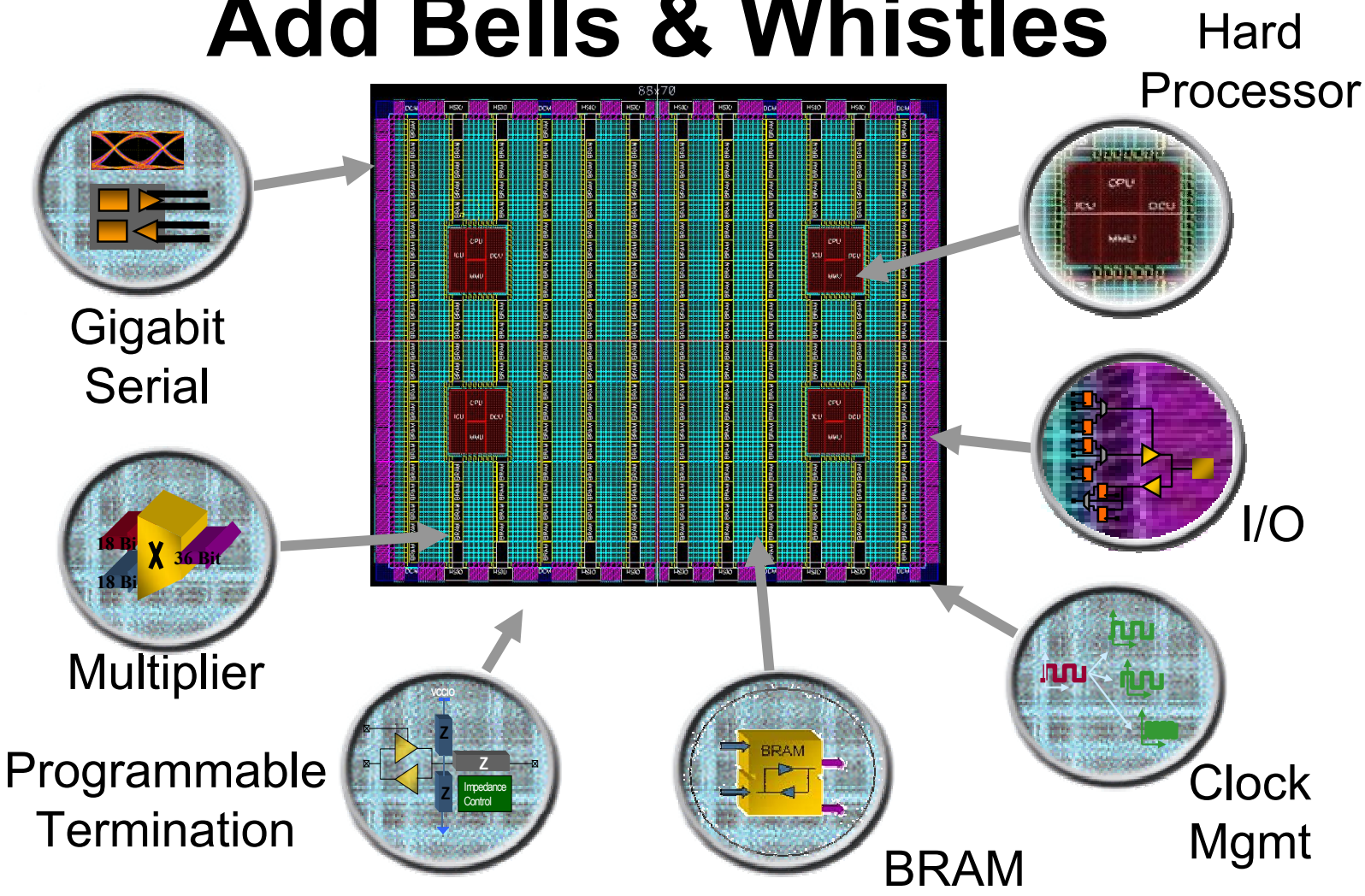


Putting the ‘R’ in RC

- Fine-grained FPGAs are the platform of choice for Reconfigurable Computing.



Add Bells & Whistles



Problem definition

- Perform processing on a stream of data
- Sampling rates in the order of 100KHz to 100MHz
- per sample 1000 – 100,000 operations

Perform 10^{10}-10^{11} operations/sec, like add, multiply etc.

Note: performance is a required part of the solution!

So when do I need what?

- Processor + Cache
- LUT
- Embedded Memory
- Bus
- Reconfigurable interconect
- Internal Memory
- External Memory
- I/O

OUTLINE

- Historical perspective
- Conventional FPGAs
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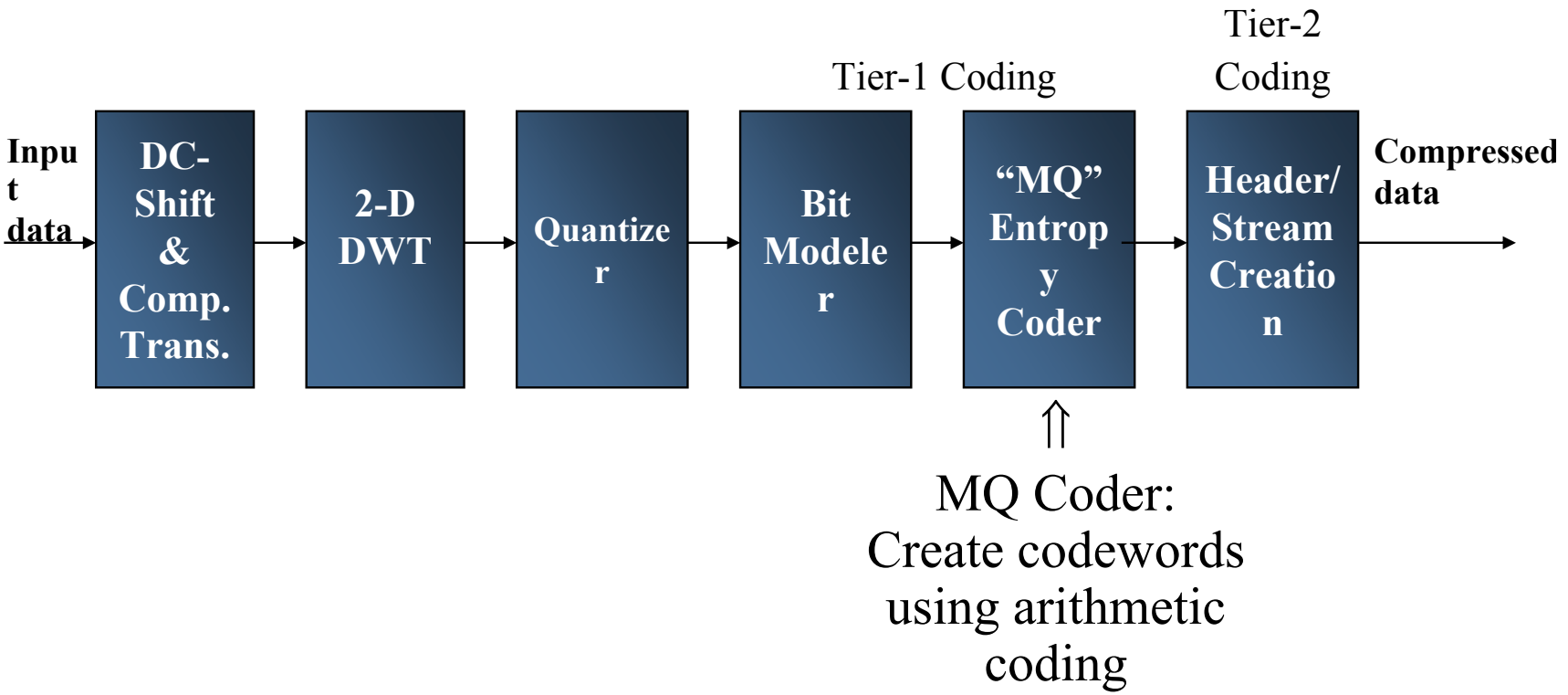
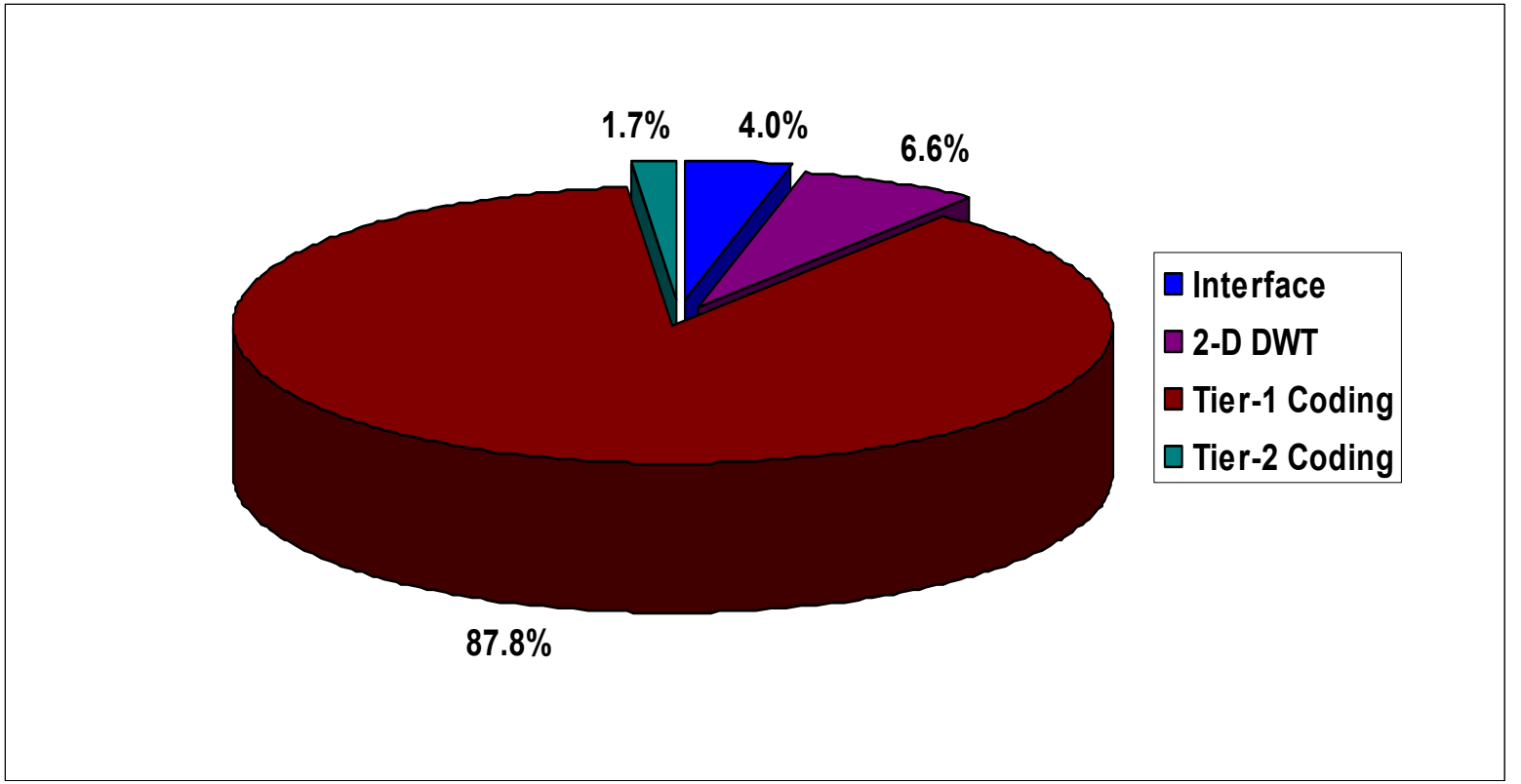
- Future Directions

JPEG2000 Encoder: Functional Block Diagram

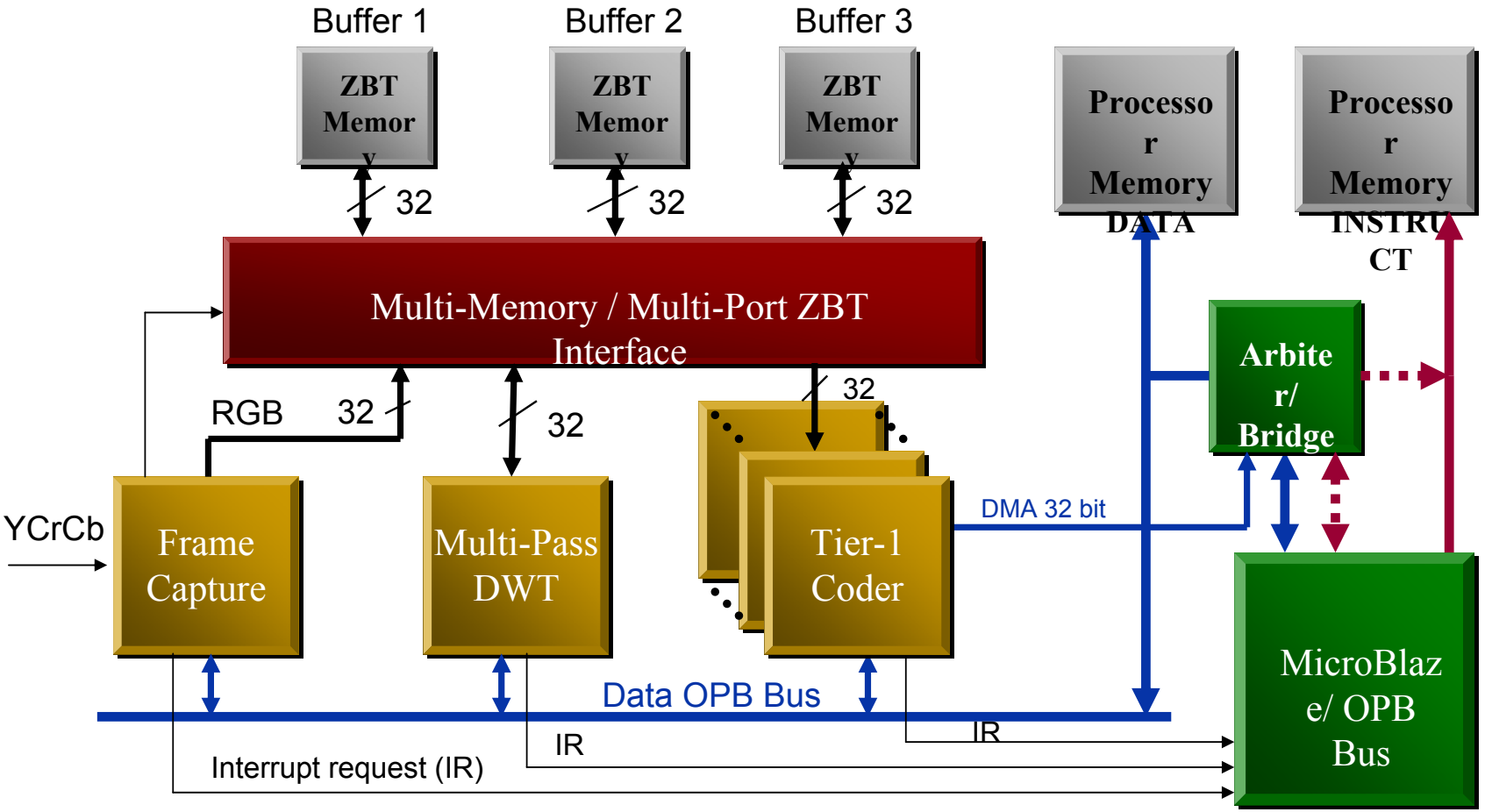


JPEG2000: Run-Time Profiling



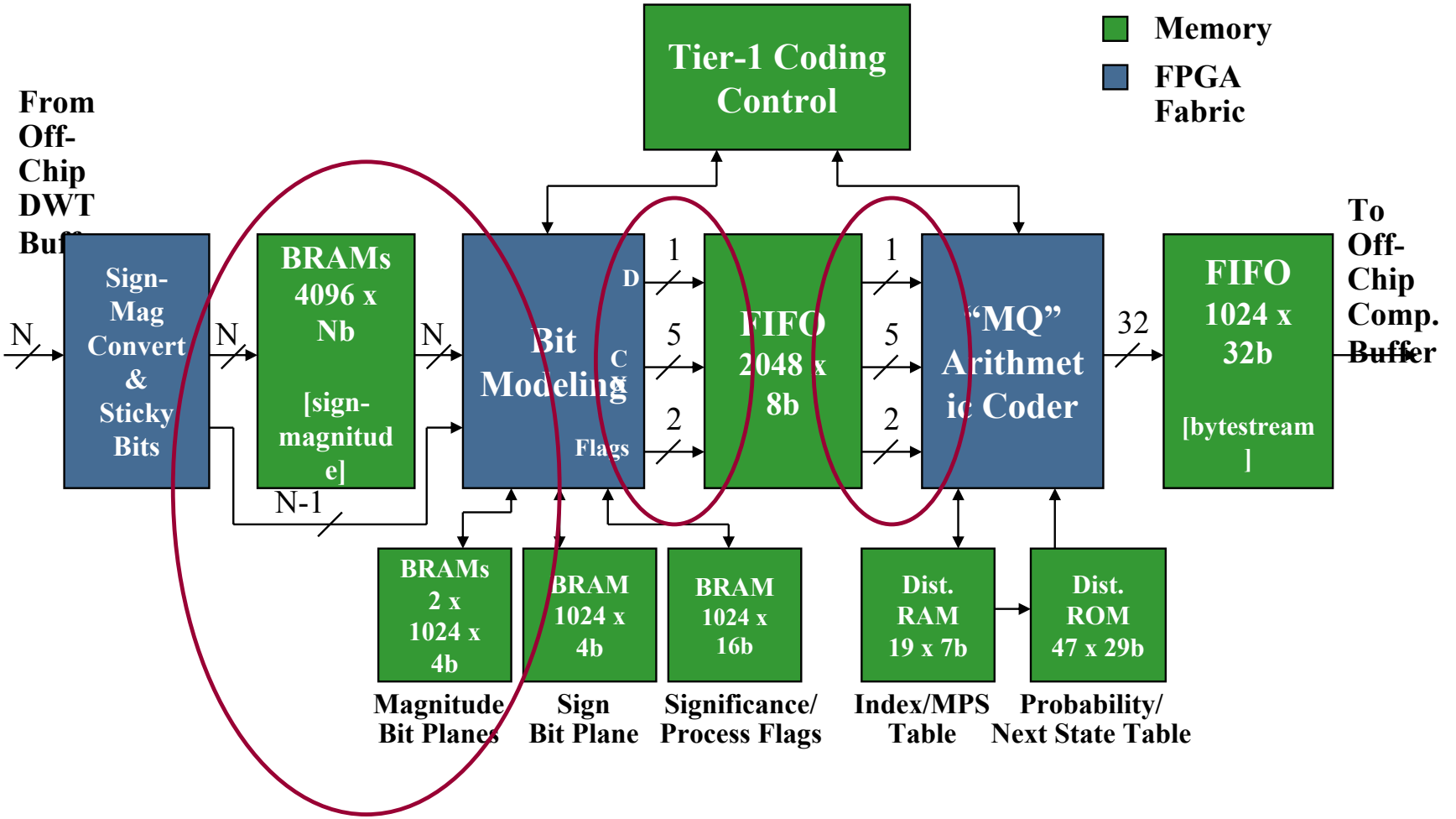
* Run on XRL's JPEG2000 ANSI C code

JPEG2000 Encoder on Multimedia Board

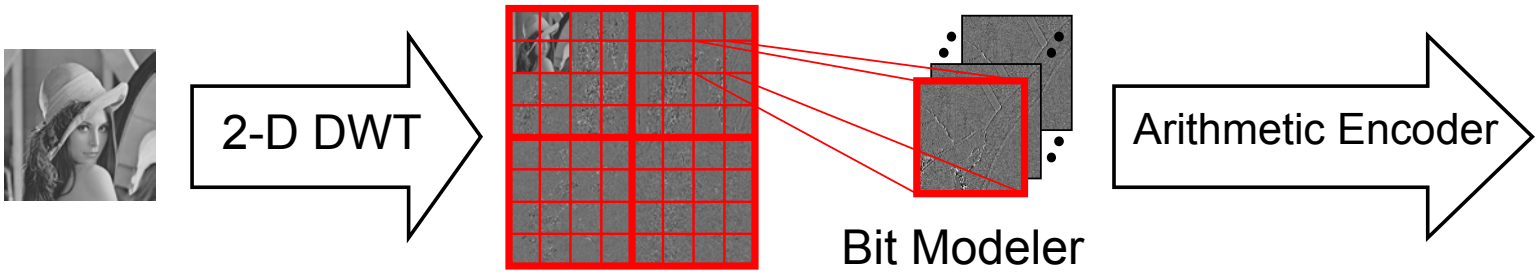


Tier-1 Coder: Block Diagram

[Original Design]



JPEG2000 Example



Technology	Application Performance	Input Data Rate (Msamples/sec)	Compression Ratio	System Clock Rate (MHz)
FPGA[1]	640 x 480 @ 30 fps	18.4	10:1	54
DSP Processor[2]	352 x 240 @ 8 fps	1.35	10:1	600
ASIC[3]	720 x 480 @ 30 fps	20.7	N/A	27

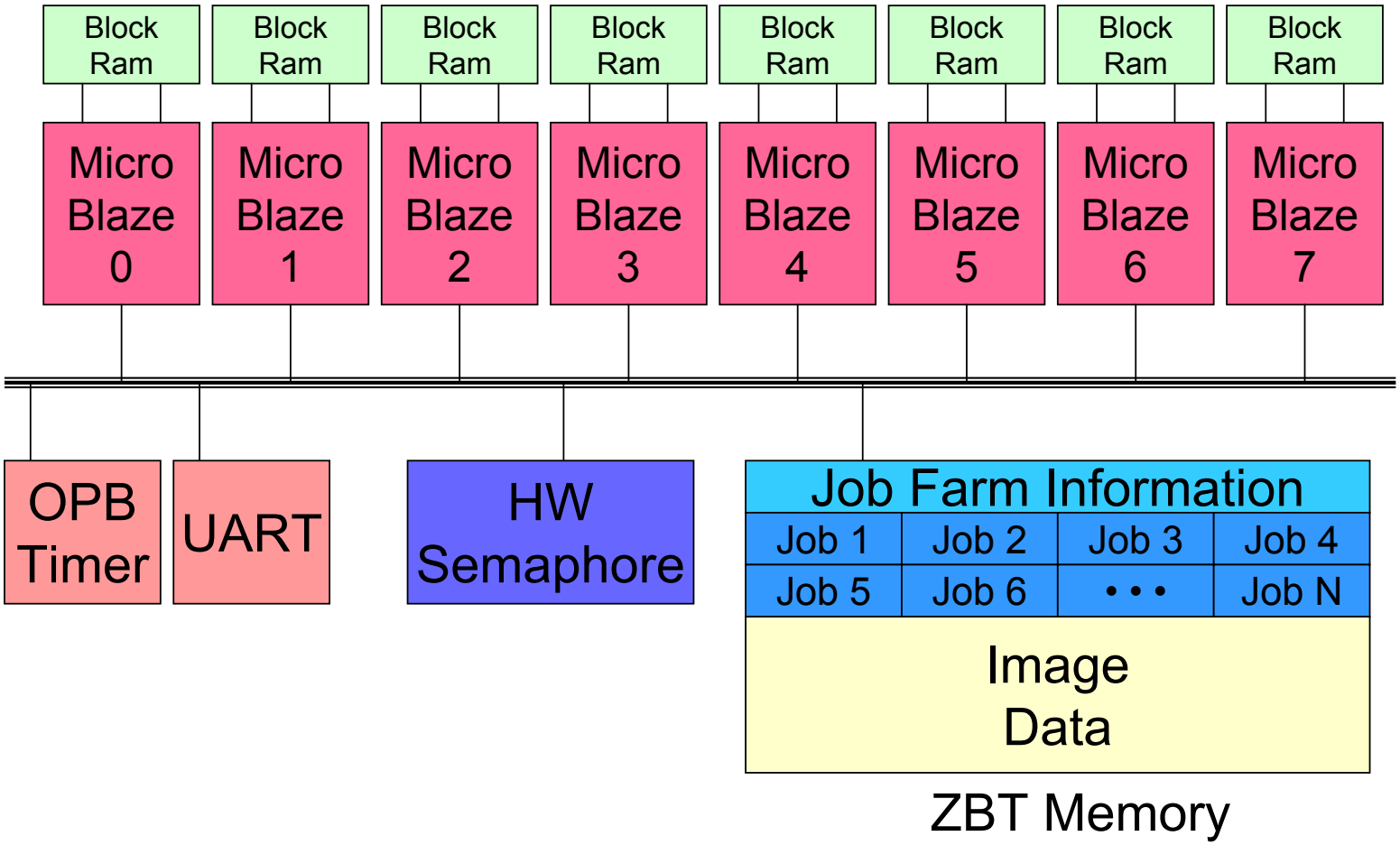
Sources: [1]Schumacher [2]Aware Inc. [3]Yamauchi

Power Efficiency Results

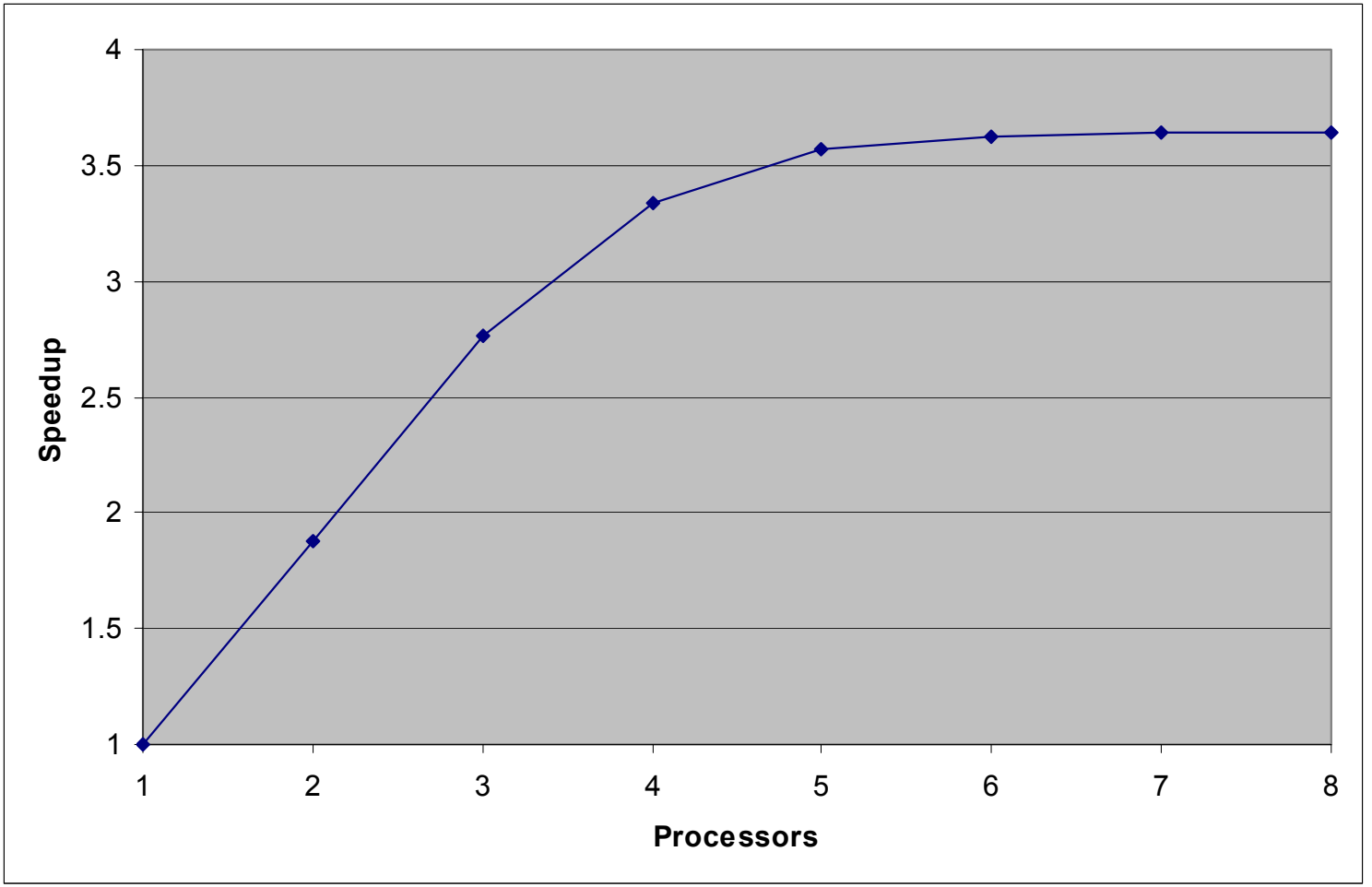
Technology	Power Dissipation (in Watts)			Relative Power Efficiency (Relative MOPS/mW)
	Device	External Memory	Total	
FPGA	3.5	3.5	7.0	1
DSP Processor	1.7	2.4	4.1	0.13
ASIC	2.0	0.2	2.2	3.6

- FPGA has 8x efficiency of processor
  - 14 x throughput
  - 1/10 x system clock
- More on-board memory would help. Look for evolving memory hierarchies.

Job Farm w/ Eight MicroBlazes



Multiple MicroBlaze DWT Results



Job Farm

- Make sure the ‘bus’ or the internal network can handle the required bandwidth
- Make sure that the latency is under control: drive towards multi-threading/multi context
- The granularity of the communication matters

OUTLINE

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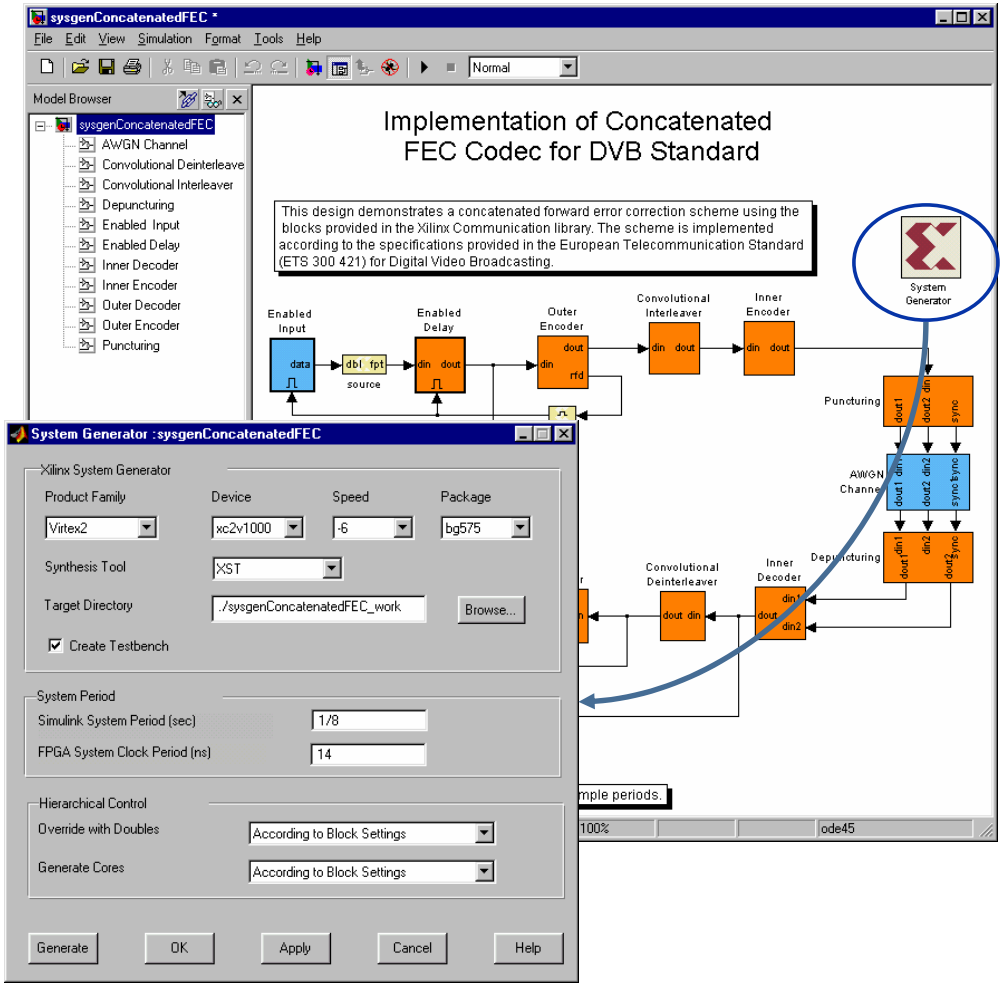
System Generator for DSP

- Library-based, visual data flow
- Polymorphic operators
- Arbitrary precision fixed-point
- Bit and cycle true modeling

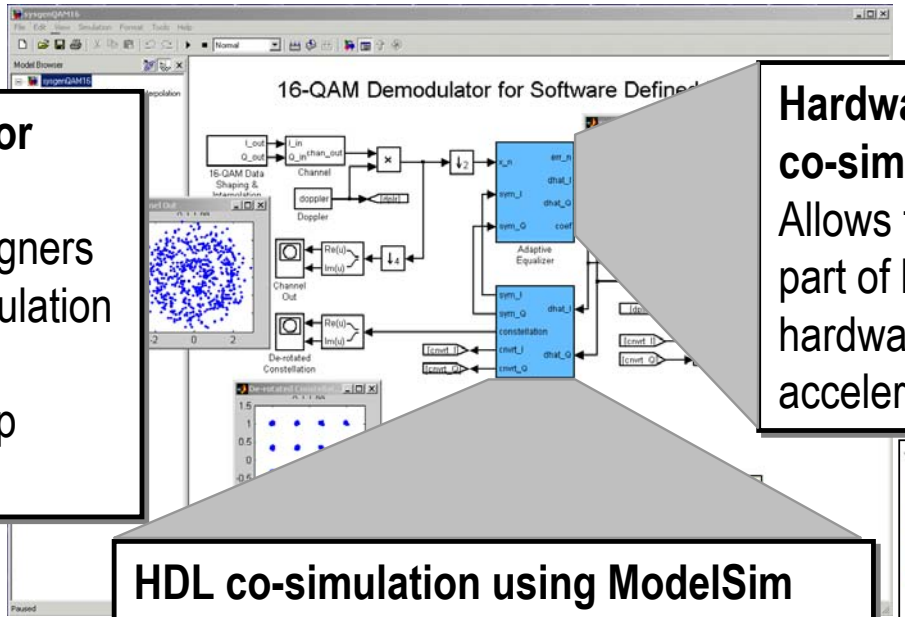
- Seamlessly integrated with Simulink and MATLAB
  - Test bench and data analysis

- Automatic code generation
  - Synthesizable VHDL
  - IP cores
  - HDL test bench
  - Project and constraint files

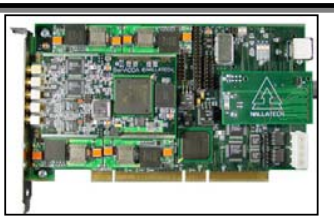


System Generator for DSP

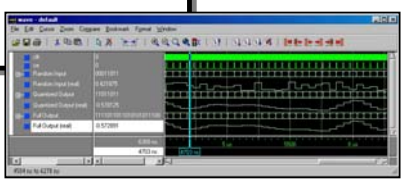
System Generator for DSP v3.1
Allows Systems Designers to target external simulation engines
- Hardware in the loop
- HDL co-simulation



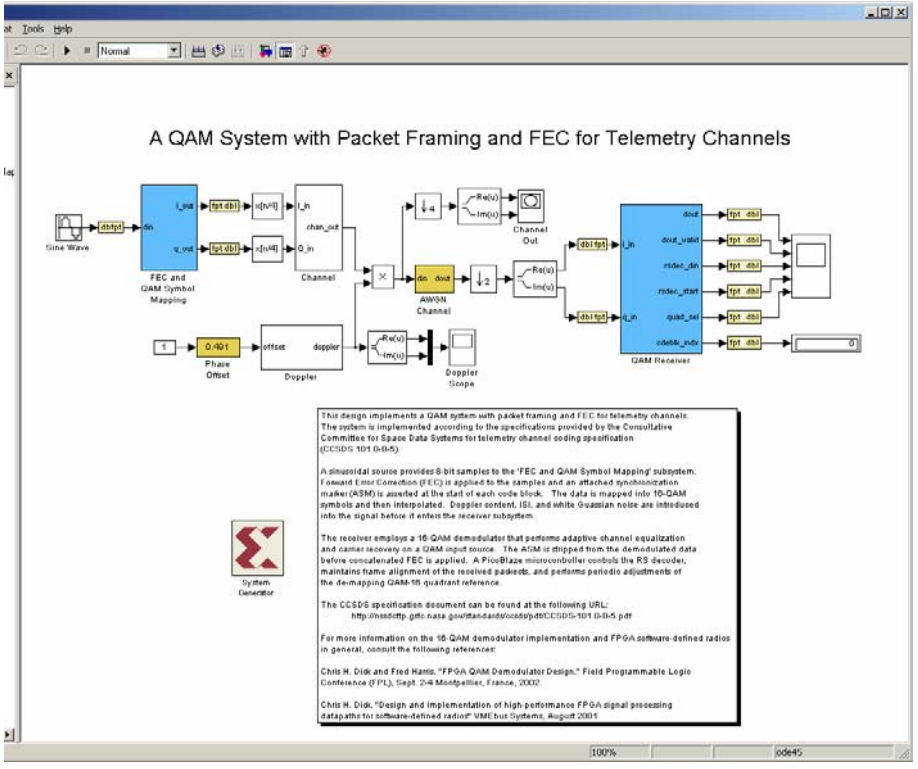
Hardware in the loop co-simulation
Allows the user to simulate part of his system on actual hardware. This means acceleration & verification



HDL co-simulation using ModelSim
Allows the user automatically invoke ModelSim and simulate his Verilog/VHDL directly from Simulink.



Documented Reference Designs



- 16-QAM receiver, including LMS based equalizer and carrier recovery loop
- A/D and delta-sigma D/A conversion
- Concatenated FEC codec for DVB
- Custom FIR filter reference library
- Digital down converter for GSM
- 2D discrete wavelet transform (DWT) filter
- 2D filtering using a 5x5 operator
- Color space conversion
- CORDIC reference design
- Polyphase MAC-based FIR
- Streaming FFT/IFFT
- BER Tester using AWGN model

OUTLINE

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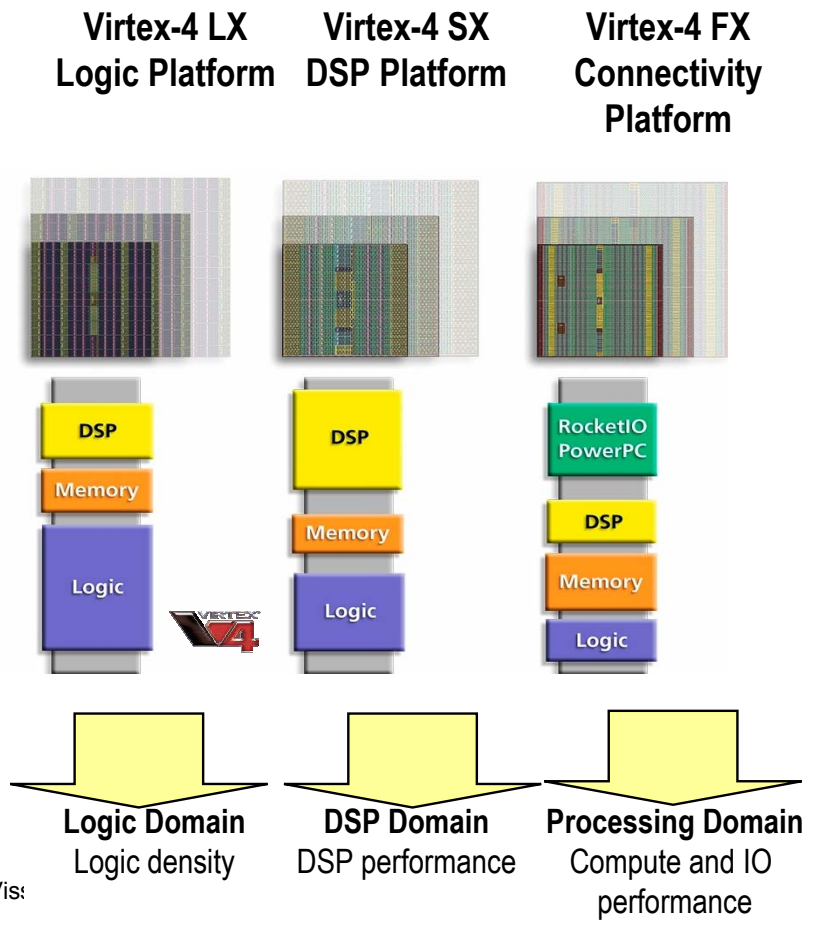
The mix revisited

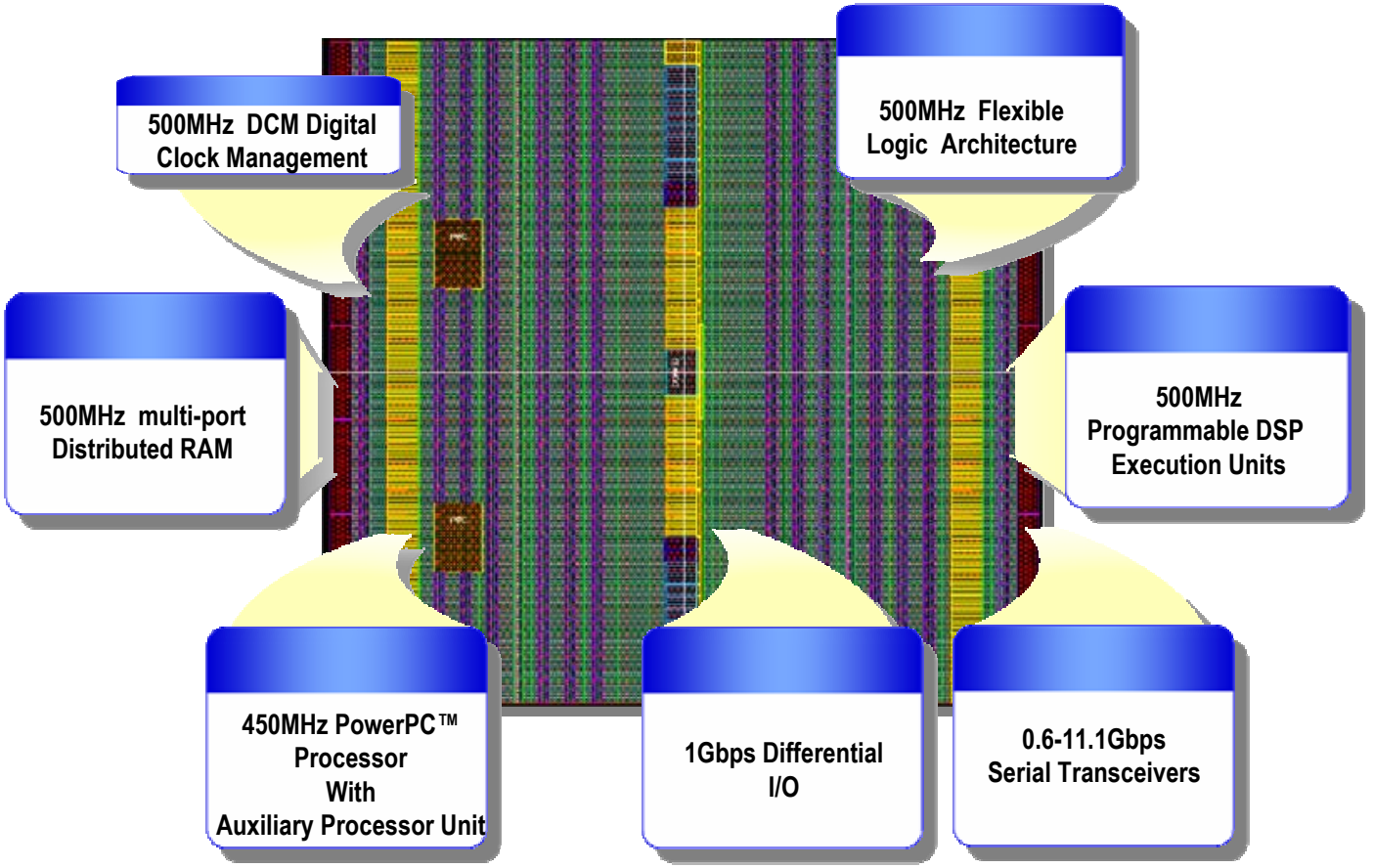
- Processor + Cache
- LUT
- Embedded Memory
- Bus
- Reconfigurable interconect
- Internal Memory
- External Memory
- I/O

The Future : Domain Optimized Programmable Platforms

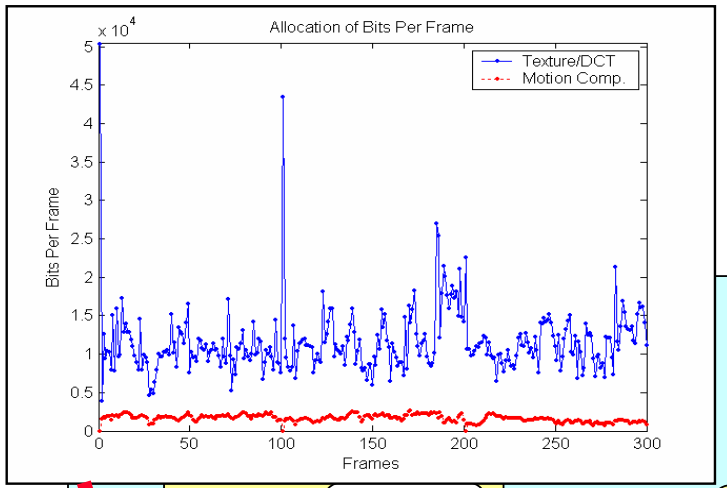
- Programmable
  - mass market of one
- Parallelism
  - performance and power
- Scalable
  - ride Moore's Law
- Distributed memory
  - data transfer bottleneck
- Regular
  - manufacturable
- Domain optimized
  - cost
- Hyper-programming
  - more degrees of freedom,
  - spatial computing

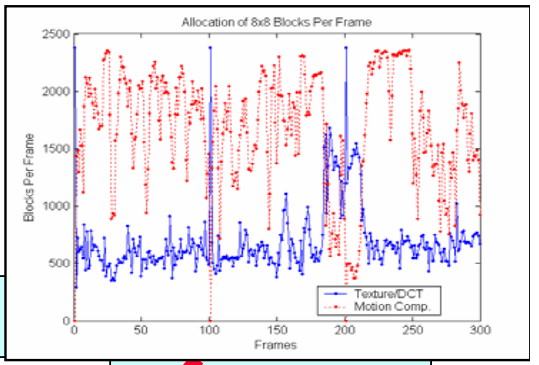


The Characteristics



The tool we need





External SRAM Current Frame

Current Frame Memory Controller

Input stream

8

FIFO

8

Decode Headers (VOL, VOP)

DMUX

Motion Decoder

Texture VL Decoder

VLD

Motion Vectors

FIFO

Motion Vectors

Motion Compensation

8×8 Block

Object FIFO

8×8 Block

8×8 Block

Object FIFO

8×8 Block

Coeffs and DC

Object FIFO

Inverse Scan

Inverse AC DC Prediction

FIFO

DCT Coeff

Inverse Quantisation / IDCT

8x8 Block

Not Coded

MPEG-4 Decoder

Acknowledgements

The author gratefully acknowledges the contributions of material, insight and feedback from:

David Parlour, Steve Trimberger, Robert Turney, Paul Schumacher, Rick Ballantyne, Mark Paluszkiewicz- *Xilinx Research Labs*

André DeHon - *California Institute of Technology*

Kristof Denolf, Adrian Chirila-Rus, Bart Vanhoof, Jan Bormans - *IMEC*

University donations

- http://www.xilinx.com/univ/xup/ubroch/qform.htm
- http://www.xilinx.com/univ/ML310/ml310_mainpage.html

What is it?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Return to XUP Home Page
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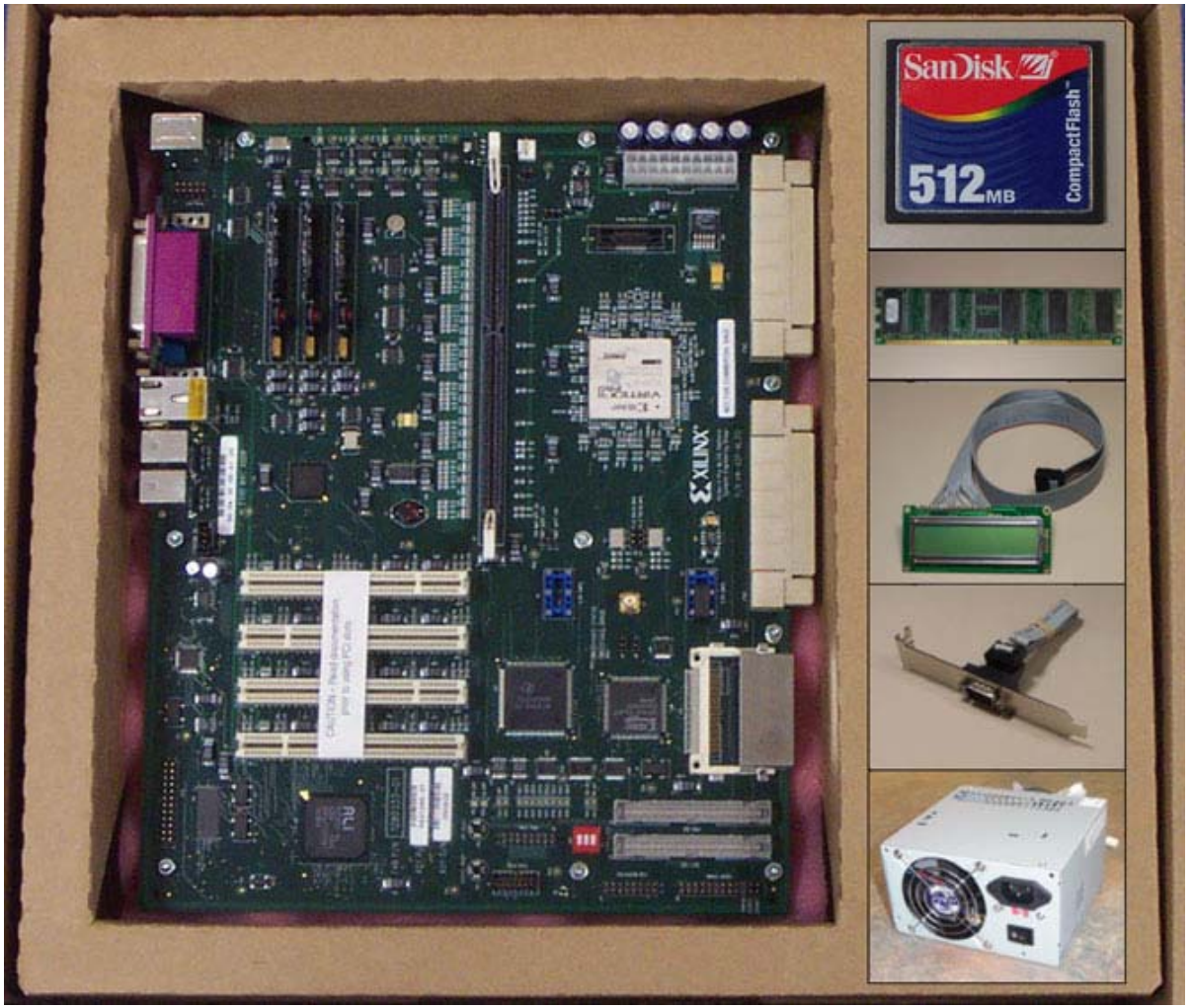
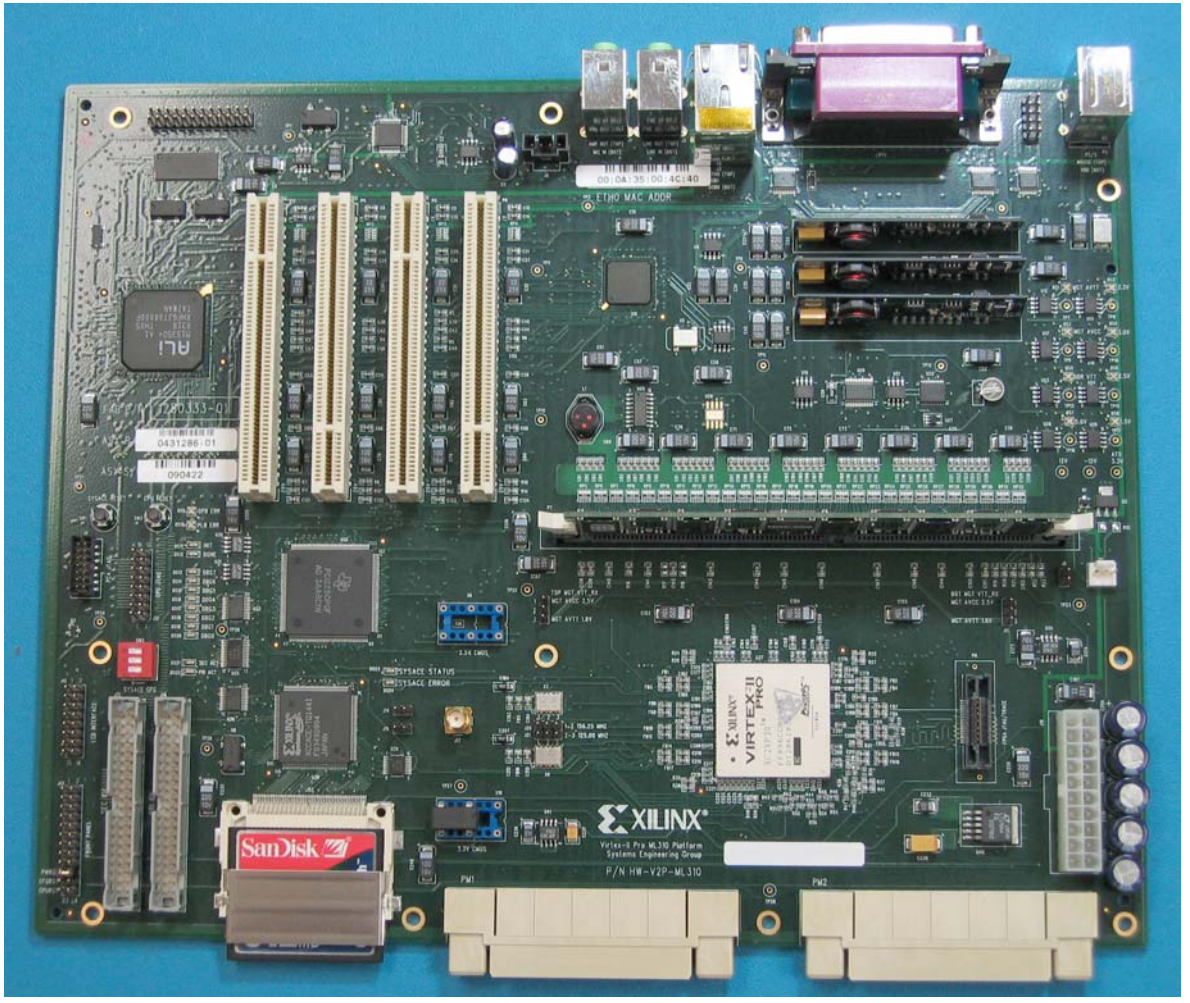
CompactFlash
Personality Module Interface
Board and Component Data
Utilities
Box
Board
Block Diagram
Platform Features
ML310 board (ATX form factor)
256 MB DDR DIMM
System ACE™ CF Controller
512 MB CompactFlash card
Onboard 10/100 Ethernet NIC
4 PCI slots (3.3V and 5V)
LCD character display and cable
FPGA serial port connection
RS-232 mini-cable
Personality module interface for RocketIO and LVDS access
Standard JTAG connectivity
ALi Super I/O
1 parallel and 2 serial ports
2 USB ports
2 IDE connectors
GPIO
SMBus Interface
AC97 Audio CODEC
PS/2 keyboard and mouse ports
ATX power supply
Documentation CD
Ordering Information
As a member of the Xilinx University Program, you will receive the special price of $995.00 USD.
The ML310 is normally priced at $2,495.00. Purchases can only be made through our distributors by referring to the following part numbers:

Box



Board



Block Diagram