Memory Issues in SoC

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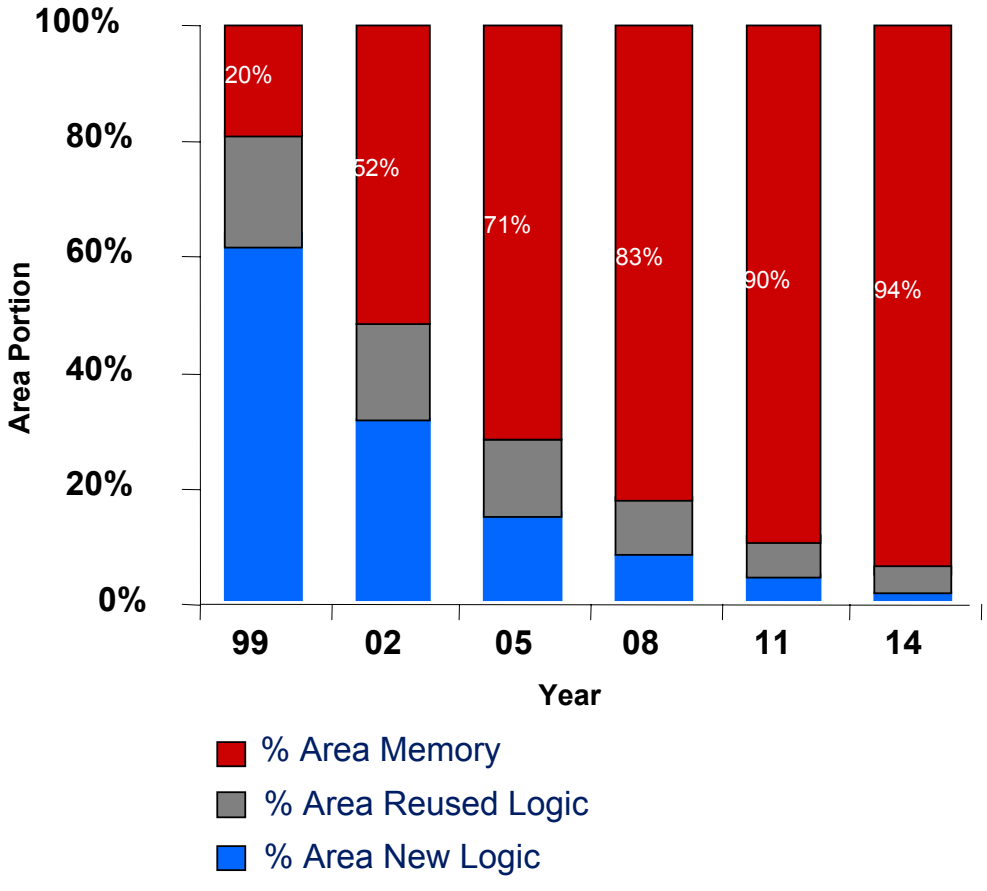
Memory Issues in SoC

- Trends of memory content in SoC
- Memory solutions and trade offs
- New memory technologies

Memory Content Forecast (ASIC type)



Source: IC Insights, SIA Roadmap and others

Advantages

lower power consumptio
higher bandwidth
‚form factor'

Disadvantages

cost (mask, ramp..)
decreased flexibility
process complexity
yield limitations

Challenges

Devices are becoming memories with ‚programmable' or reconfigurable logic

Embedded Memory

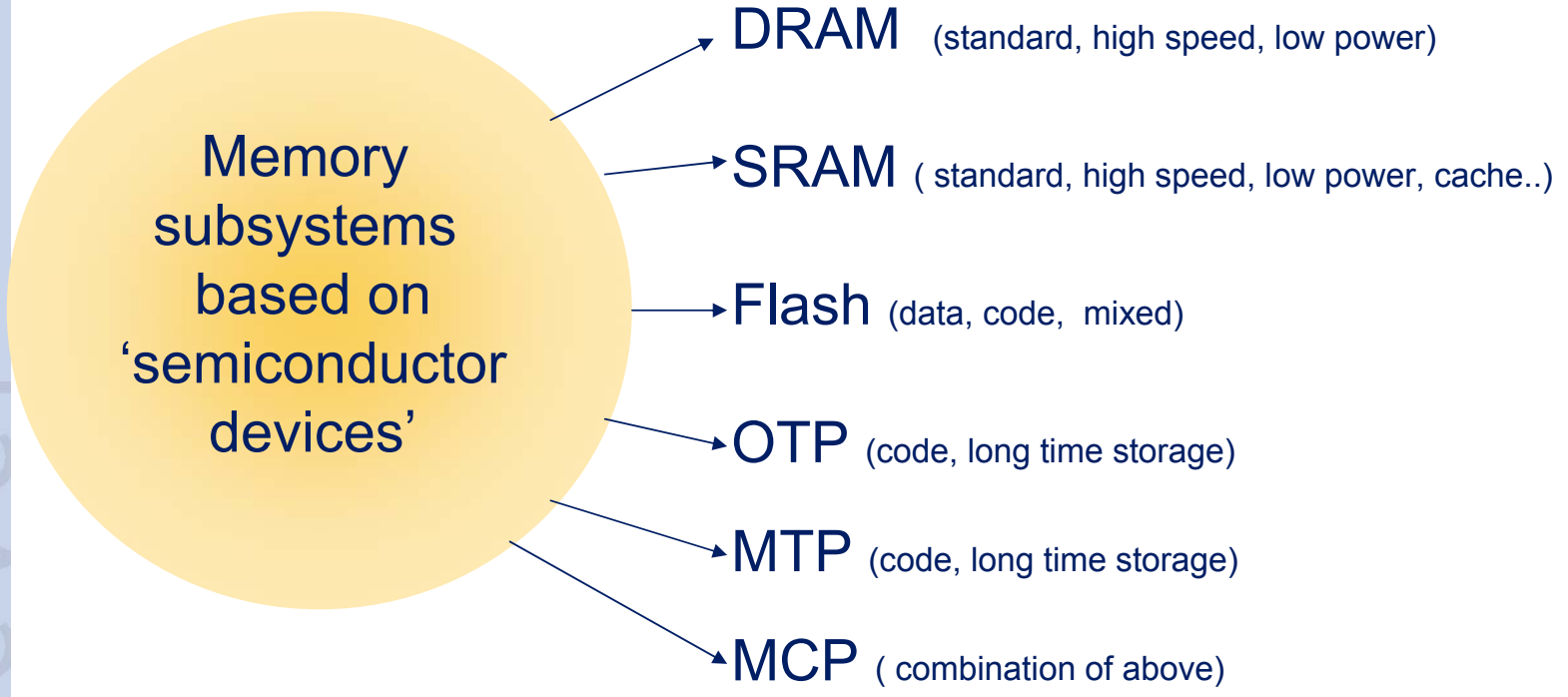
- ✓ bandwidth adapted to the application
- ✓ less driver and interconnect delay
- ✓ optimized (multi bank) architectures
- ✓ reduced I/O power
- ✓ on-demand memory activation
- ✓ Optimized memory size (vs commodity)

Possible cost reduction using embedded Memory

- ✓ **Reduction of packaging costs**
- ✓ **Form factor enabling portable applications**
- ✓ **Board space saving**
- ✓ **Less magnetic interference**
- ✓ **Take advantage of ‘loose areas’ due to pin/ pad limited designs**

This however is extremely dependent on the commodity market

Possible semiconductor solutions for memories



Memory Core Concepts

Requirements

- ✓ Quick and first time right implementations of compilers or customized memories
- ✓ Building block architecture with fine granularity of memory sizes
- ✓ Large range of interface width
- ✓ Interfaces have to comply with high level design methodologies
- ✓ Configurable multi-bank architectures and variable page sizes
- ✓ Flexible redundancy concept
- ✓ Inexpensive test methodology in place

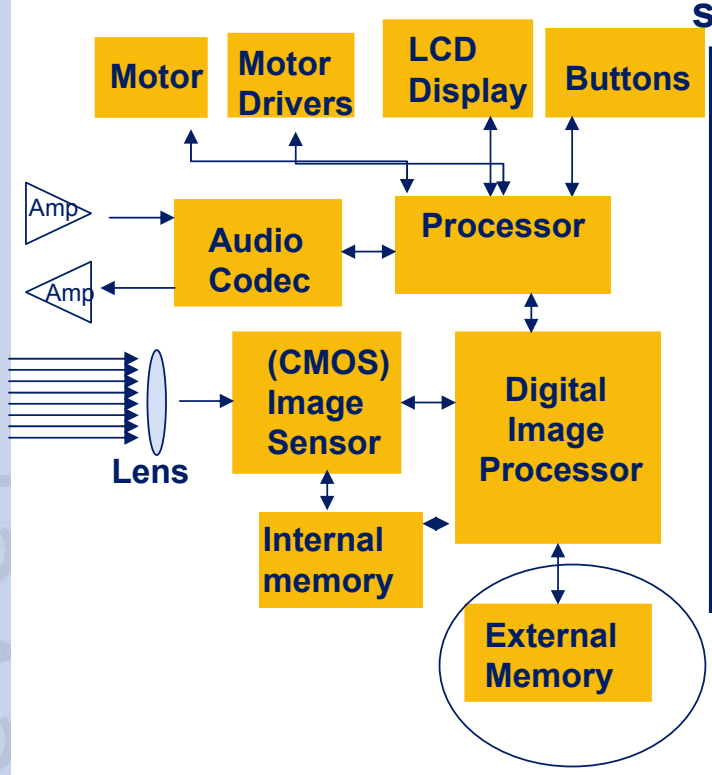
Integration of memories

Main challenge for integration

functionality vs process costs
performance vs process features
package cost vs power
special process vs area utilization
typical market behavior for commodity products
MCP vs integration
yield estimates
reliability issues

Applications
Digital still camera (high end)

Technical requirements impacting the internal memory and the memory subsystems



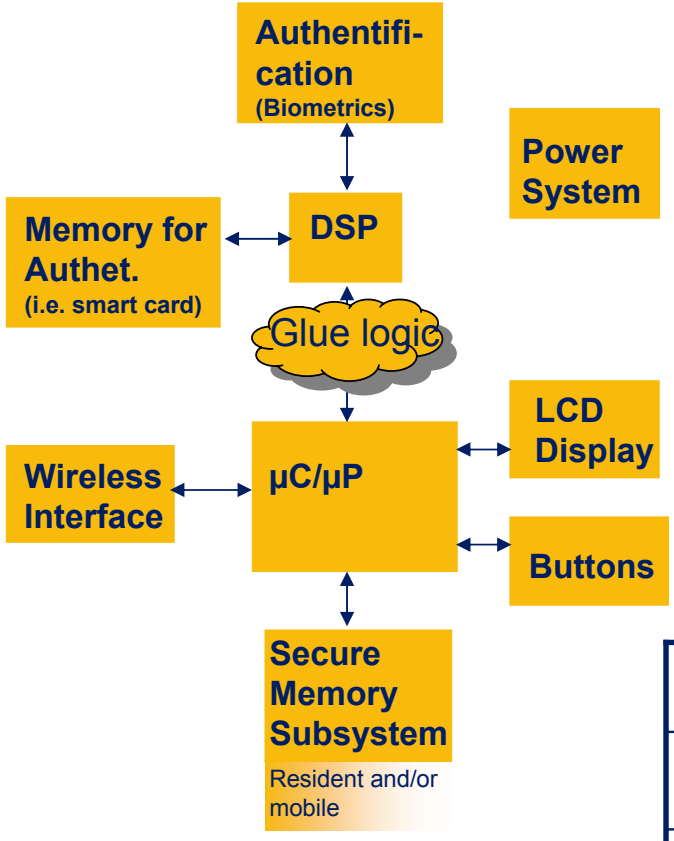
	today	2005	2007
Total memory capacity (card)	256MB	4GB	10GB
DRAM (if available)	64Mb	512Mb	2Gb
Typical high end picture	3 MB	6 MB	9 MB
Typical number of active pixels	4 Mega	8 Mega	12 Mega
Typical mainstream picture (no new compression mode)	1,7MB	3,5MB	**5,3 MB**

Direct storage to card

Storage to internal DRAM and streaming to card later

Applications
Security/Safety Monitoring Systems

Technical requirements impacting the internal memory and the memory subsystems



	today	2005	2007
Total memory capacity (card)	256MB	4GB	10GB
Micro drive capacity	1GB	8 GB	10-12GB

Comparison existing technologies

	SRAM	eFlash	eDRAM
Write time	<< 10 ns	~ 100 µs	< 20 ns
Write endurance	> 10^{15}	~ 10^{6}	> 10^{15}
Read time	<< 10 ns	~ 20 ns	< 20 ns
Volatility	no refresh req.	Non volatile	Refresh req.
SER immunity	- -	+	+
Cell size	> 100 F^2	~ 10 F^2	~ 8 F^2
Mask adder compared to standard CMOS	0	5-8	4-8

New Memory Technologies – next candidates (1)

Ferro RAMs

polarization of an internal dipole in i.e. PZT material
reading of displacement current; destructive read
low power consumption

Phase Change RAM

Chalcogenides (CDs , DVDs) are changing from amorphous to crystalline status through heating
Resistance measurement; medium power required

MRAM

Switching of magnetic polarity of the sense layer
fast write/read, high endurance
high write current

CBRAM

Chalcogenides or other materials which can built a conducting path by ‘reordering’ dissolved silver
fast write plus rel. low power

New Memory Technologies – next candidates (2)

Polymer Memory

- change in resistance
- all polymer vs hybrid

Molecular memory

- Cross point cells which contain molecules which change electronic stated in Redox process
- Multibit capabilities

Carbon Nanotubes

- resistance sensing
- nanotube ‘ordering’ in a crossbar architecture

Millipede Memory

- little bit like ‘old fashioned punch cards’
- PMMA

End

Thank you for listening