MPSoC'05 PROGRAMME

MONDAY JULY 11

8.30 Registration

OPENING SESSION: KEYNOTES

9.30 Digital Media: The New Frontier for Supercomputing
Lisa T. Su, VP, Technology Development and Alliances, IBM Systems and Technology Group, Hopewell Junction NY, USA

10.30 Break

11.00 Nomadik: an MPSoC Solution for Advance Multimedia
Alain Artieri, Director of Engineering, Application Processor and Portable Platforms Division, ST, Grenoble France

12.00 Discussion with keynote speakers

12.30 Lunch

TUTORIAL SESSION T1: MPSOC: HW CHALLENGES

14.00 Reliability and Reliable Design
Giovanni De Micheli, EPFL, Switzerland

14.45 Configurable Core Generation for Multi-Processor SoC
Masaharu Imai, Graduate School of Information Science and Technology, Osaka University, Suita, Japan

15.30 Break

TUTORIAL SESSION T2: MPSOC: SW CHALLENGES

16.00 Foundations for Model-Based Design
Janos Sztipanovits, ISIS-Vanderbilt University, USA

16.45 Software-Centric System-Level Design
Hiroaki Takada, Nagoya University, Graduate School of Information Science, Japan

17.30 Discussion with tutorial speakers

18.00 Participants' presentation

TUESDAY JULY 12

SESSION 1: FROM NETWORKING TO NETWORK-ON-CHIP

8.30 On-Chip Interconnects: Circuits and Signaling from an MPSOC Perspective
Wayne Burleson, ECE Dept., University of Massachusetts Amherst, USA

9.15 Global Networking versus Networking-on-Chip
Martina Zitterbart, Institute of Telematics, University of Karlsruhe (TH) Germany

10.00 Break

SESSION 2: NETWORK-ON-CHIP

10.30 NoCs: pushing toward the back-end
Luca Benini, DEIS, University of Bologna, Italy

10.42 From Spaghetti wires to NoC
Marcello Coppola, ST, France

10.54 NoC: the Arch key of IP integration methodology
Alain Fanet, Arteris, France

11.06 Systems on Chips: Personal Computers or correct performance?
Kees Goossens, Embedded Systems Architectures on Silicon (ESAS) group, IC Design sector, Philips Research, The Netherlands

11.18 Design-for-Yield
Yervant Zorian, Virage Logic, USA

11.30 Discussion with the lecturers of the session

12.30 Lunch

SESSION 3: THE CELL ARCHITECTURE

14.00 Cell Architecture and Broadband Engine Processor
Ted Maeurer, IBM Systems and Technology Group, Austin, USA

14.45 The Design and Implementation of a First-Generation CELL Processor: A Multi-Core SuperComputer SoC
Dac C. Pham, IBM Systems and Technology Group, Austin, USA

15.30 Break

SESSION 4: MPSOC PLATFORMS

16.00 Formal methods in MpSoC architecture optimization
Rolf Ernst, TU Braunschweig, Germany

16.12 Multiprocessor Architecture for Consumer Electronics SOC
Takao Nishitani, Kochi University of Technology, Japan

16.24 SoC Platforms of the Future: Challenges and Solutions
Pierre G. Paulin, ST, Ottawa, Canada

16.36 Optimization of Reliability and Power Consumption in MPSoCs
Tajana Šimunić Rosing, UC San Diego, USA

16.48 Breaking the Interleaving Bottleneck in Communication Applications for Efficient SoC Implementations
Norbert Wehn, University of Kaiserslautern, Germany

17.00 Discussion with the lecturers of the session

WEDNESDAY JULY 13

SESSION 5: MPSOC: THEORY & PRACTICES

8.30 Real Time Ray Tracing Algorithms for Next Generation CMP GPUs
Donald S. Fussell, The University of Texas at Austin, USA

9.00 New challenges in Smart Card design
Jean-Pierre Tual, Axalto, France

9.30 Power and Security Management in an NoC for Next Generation Mobile MPSoC's
Drew Wingard, CTO, Sonics Inc. USA

10.00 Break

SESSION 6: TECHNOLOGIES FOR MPSOC

10.30 Surfing the wave of Moore's law?
Rafael Peset Llopis, Philips Consumer Electronics, The Netherlands

10.42 Bridging the gap between semiconductor technology and design: a memory case study
Rudy Lauwereins, IMEC, Belgium

10.54 Multi-level Co-Simulation of Mixed Technology Microsystems
Steven P. Levitan, University of Pittsburgh, USA

11.06 Soft Errors: Tools and Interactions with Power Optimizations
Vijaykrishnan Narayanan, Embedded and Mobile Computing Design Center, Pennsylvania State University, USA

11.18 System level Stimuli Generation for the Cell processor
Roy Emek, IBM Labs in Haifa, Israel

11.30 Discussion with the lecturers of the session

12.30 Lunch

SESSION 7: HW & SW PROGRAMMING FOR MPSOC

14.00 Configurable Processor - the new NAND gate for MPSOC
Beatrice Fu, Tensilica Inc., USA

14.30 The Sandbridge Sandblaster SB3000 Multithreaded CMP Platform
John Glossner, CTO & EVP, Sandbridge Technologies Inc., USA

15.00 Flexible multi-processing memory architectures
Kees Vissers, Xilinx, USA

15.30 Break

SESSION 8: APPLICATION OF PROGRAMMING MODELS

16.00 Measuring SMP
John Goodacre, ARM Ltd., UK

16.12 A class-based programming model for heterogeneous MPSoC
Mark Lippett, Ignios Ltd., UK

16.24 Linux real-time capabilities for SMP SoC platforms
Philippe Kajfasz, Thales, Land and Joint Systems, France

16.36 Redefis: An SoC Platform for Implementing Application-Specific or User-Custom Logic
Kazuaki Murakami, Kyushu University, Japan

16.48 SOC: Security-on-chip!
Srivaths Ravi, NEC Laboratories America, USA

17.00 Discussion with the lecturers of the session

18.00 Social Event

THURSDAY JULY 14

SESSION 9: BEYOND SOC PRACTICES

8.30 Sub-Lithographic Semiconductor Computing Systems
André DeHon, California Institute of Technology, USA

9.00 Self-Calibrating Interconnects: Breaking the Worst-Case Design Paradigm
Paolo Ienne, EPFL, Switzerland

9.30 MPSoC Clock and Power Challenges
Olivier Franza, Intel Corp., USA

10.00 Break

SESSION 10: PROGRAMMING MODELS FOR MPSOC

10.30 HW-SW Interfaces CoDesign for Multi-Processor SoC
Ahmed Jerraya, TIMA Laboratory, France

10.42 Cross-layer Modelling for Heterogeneous MPSoCs
Jan Madsen, Technical University of Denmark, Denmark

10.54 Specification and Validation for Heterogeneous MP-SoCs
Gabriela Nicolescu, Ecole Polytechnique de Montréal, Canada

11.06 Parallel Programming Model for Distributed Architecture MPSoC
Yuriy Sheynin, St. Petersburg State University of Aerospace Instrumentation, Russia

11.18 Introducing Mixed Signal into FPGA based MPSoC
Yankin Tanurhan, Actel Corporation, USA

11.30 Discussion with the lecturers of the session

12.30 Lunch

SESSION 11: CORE BASED DESIGN ENVIRONMENTS

14.00 MeP (Media Embedded Processor), a configurable and extensible microprocessor designed for heterogeneous multi-processor SoC
Masataka Matsui, Toshiba Corp., Japan

14.30 Industrial Usage of C-based Synthesis and Verification
Kazutoshi Wakabayashi, NEC Corp., Japan

15.00 Synchronous Debugging of Multicore Systems
Vojin Zivojnovic, VP ESL Tools, ARM Inc., USA

15.30 Break

SESSION 12: APPLICATION FOR CORE BASED DESIGN

16.00 Multithreaded processors in Embedded Applications
Steffen Buch, Infineon Technologies AG, Germany

16.12 Using Configurable CPUs on SOC Platforms
Trevor Mudge, The University of Michigan, Ann Arbor, USA

16.24 A Service Based Component Model for Multi-Level HW/SW Specifications
Frédéric Pétrot, TIMA Laboratory, France

16.36 Communication Platforms for Network-on-Chip
Hannu Tenhunen, Royal Institute of Technology (KTH), IT-Universitet, Sweden

16.48 Everything I know about software radio in 10 minutes or less
Wayne Wolf, Dept. of EE, Princeton University, USA

17.00 Discussion with the lecturers of the session

FRIDAY JULY 15

BUSINESS SESSION B1: DESIGN METHODS TRENDS

8.30 Designing Programmable Platforms: From ASIC to ASIP
Heinrich Meyr, Coware Inc.,USA & ISS, Aachen University of Technology, Germany

9.00 Parallel Programming Models for Heterogeneous MPSoCs
Pieter van der Wolf, Philips Research, The Netherlands

9.30 Security Technologies for SoCs
Hiroto Yasuura, System LSI Research Center, Kyushu University, Japan

10.00 Break

BUSINESS SESSION B2: BUSINESS MODELS FOR MPSOC

Moderator: **Richard Goering, Managing editor, EDA, EE Times, USA**

10.30 DFM: Where Design, Lithography and Process Meet
Raul Camposano, Sr. VP, GM and CTO, Synopsys, USA

10.42 Multimedia SoC Design Trends
Santanu Dutta, nVIDIA Corporation, Digital Media Processor Group, USA

10.54 SOC Design Foundry
Youn-Long Steve Lin, National Tsing Hua University & Global Unichip Corp., Taiwan

11.06 Coo-Petition for SoC Process and Infrastructure
Philippe Magarshack, FTM Group VP, ST, France

11.18 Prospects of SDR for Multi-Standard Radios
Ulrich Ramacher, Infineon Technologies AG, Germany

11.30 Discussion with the lecturers of the session

12.30 Lunch