Infineon

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Multithreaded Processors in Embedded Applications

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Never stop thinking.

Outline

- Motivation
- Design for Efficiency
  - Multithreaded embedded processors
  - Application case study
- Conclusions

Never stop thinking

Motivation: Design for Efficiency

- (Embedded) Standard Processor: **Performance driven** design
  - Large flexibility for a wide range of applications
  - Clock frequency has been a main feature

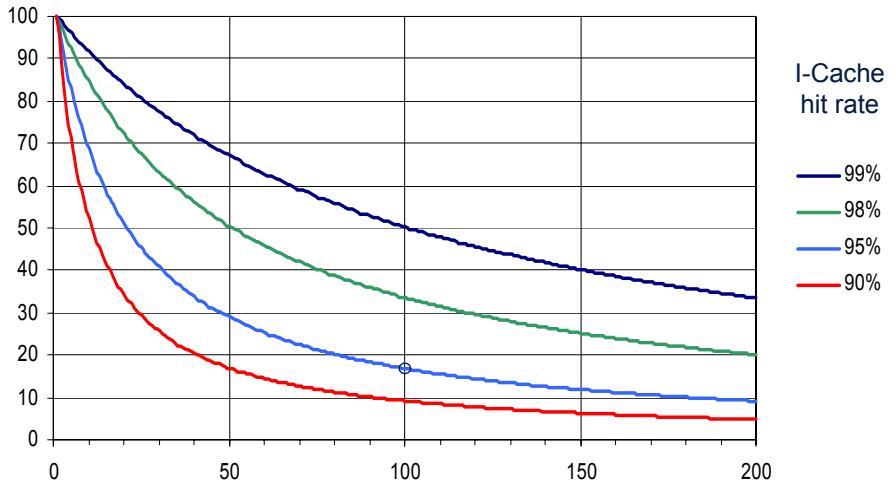
- (Deeply) Embedded Processor: **Efficiency driven** design
  => High performance with
  - Area efficiency: Throughput / Area (silicon cost)
  - Power efficiency: Throughput / Watt (battery cost)
  - Hardware design efficiency: design flow, reuse (design cost)
  - Software design efficiency: tool chain, programming model, API

Efficiency of Multi-Processor SoC

- **Area efficiency** E_a = Th / S (internet packet per s per mm²)
- **Power efficiency** E_p = Th / P (internet packet per s per µW)
- **Throughput:** Th = CR*L*M / CPI
  with
  CR = clock rate
  CPI = clocks per instruction (average)
  L : speedup of ILP
  M: speedup of parallel processors
- Key to achieve **maximum efficiency**
  - Reduce CPI
    i.e. reduce latencies of memory access, inter processor communication etc

Latency Caused by Memory Bottleneck

remaining CPU performance in %



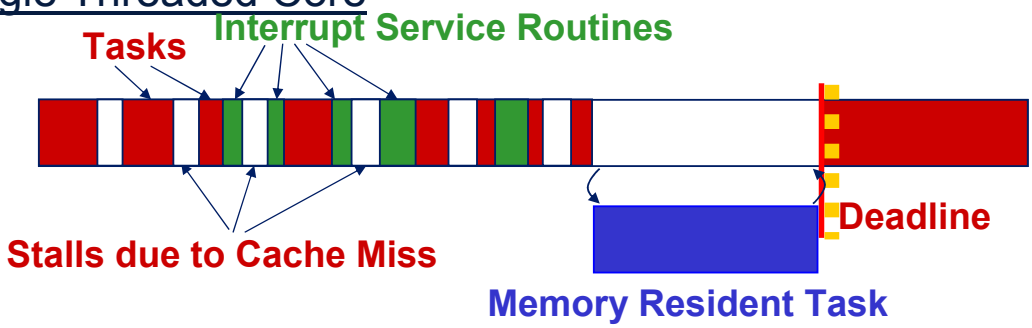
CPU clocks per cache miss

Introduction to Multithreaded Processor

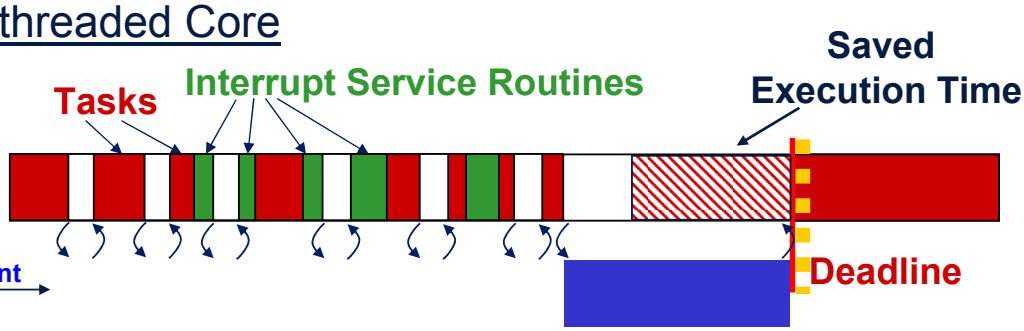
- Definition of HW-Thread
  - "Light process" ~ PC + register states
  - Each thread can be executed concurrently.
- Motivation
  - Communication Applications are multi-threaded in Nature
    - E.g. Functions for receive and transmit
    - Interrupt service routines for different interrupt sources
    - Independent packets
  - Multithreading avoids latency
    - (Cache-)Memory access
    - Peripheral access
    - Inter-processor communication
  - Multithreading allows extremely fast context switch
    - Interrupt service routines

Hiding Latency by HW-Multi-Threading

Single Threaded Core



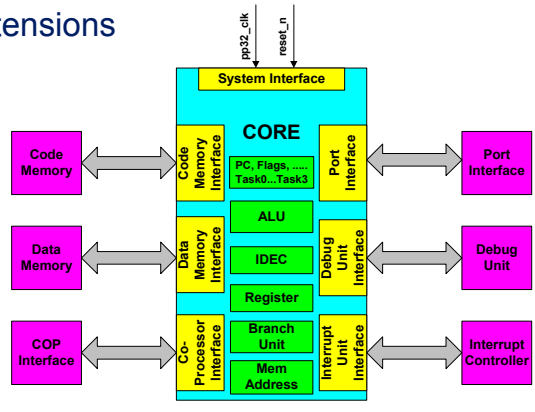
Multithreaded Core

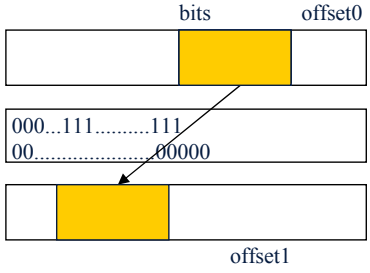


Case Study 1: Infineon Protocol Processor PP32

RISC-based load-store architecture with extensions optimized for Protocol Processing:

- Ports
  - Effective HW I/F integrated into ISA and pipeline
  - Enhancing data stream processing (Read-modify-write)
- Advanced bit-field manipulation
- Conditional execution
- Multithreading
  - exploiting the packet-level or link-level parallelism
  - fast context switch avoiding latency

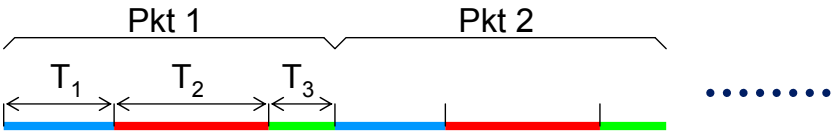




Case Study 1: Exploit Packet Level Parallelism

Conventional Solution:

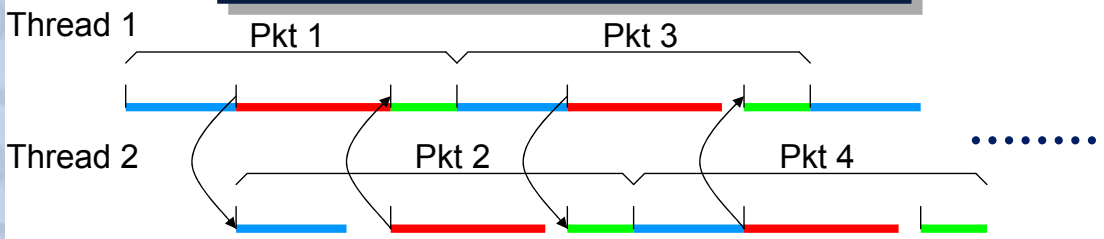
Convergate:
T_1 = 40 cycles
T_2 = 50 cycles
T_3 = 20 cycles



- Low switch overhead SPMD
- 40% throughput improvement using multithreading

0 cyc/pkt

With 2 worki



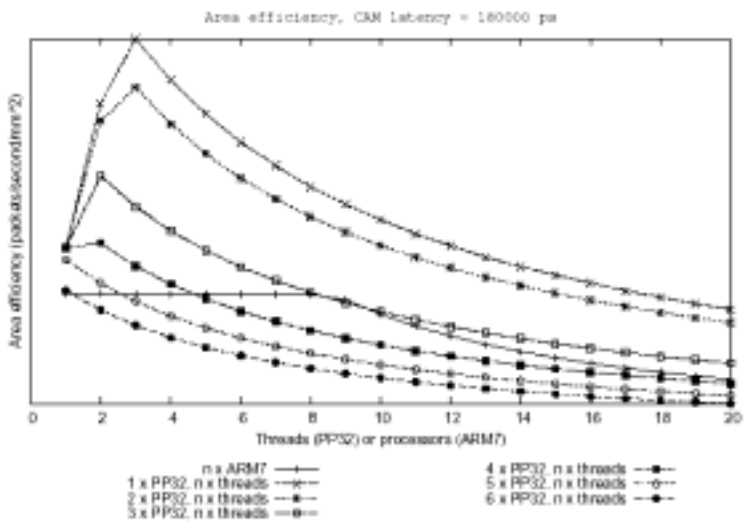
$(T_1 + T_3 + 8) = 68$ cyc/pkt

Case Study 1: Optimization of Number of Threads

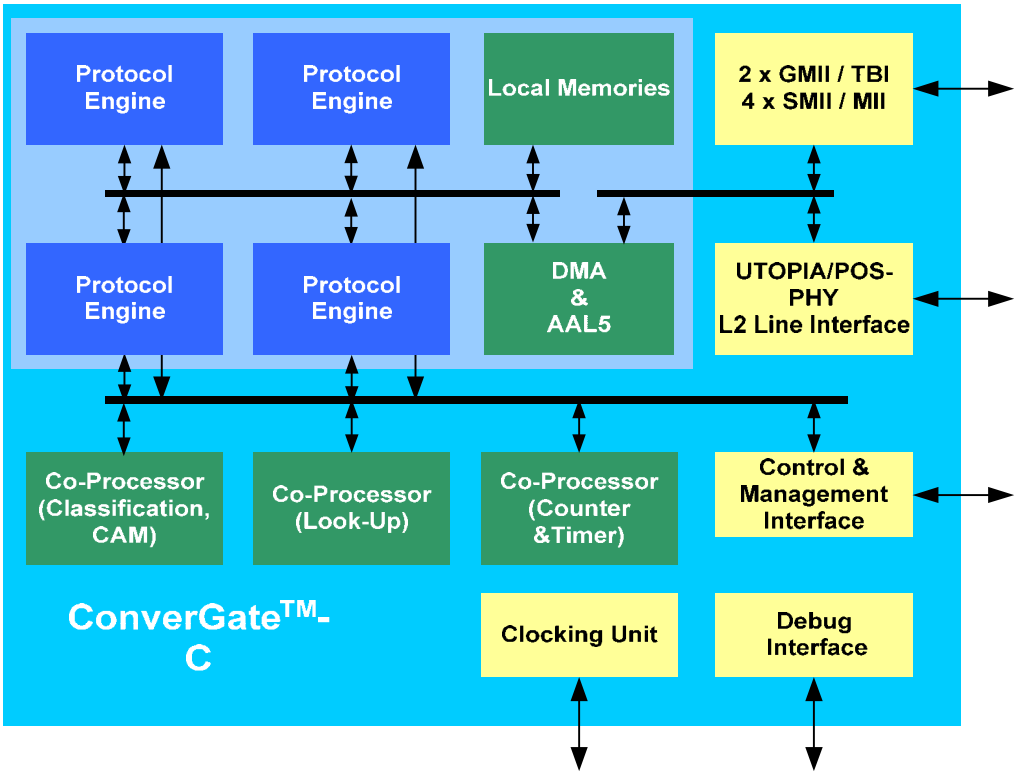
- Optimization of number of contexts
  - CPI decreases with number of contexts
  - Area increases at the same time
  - How many threads can be utilized by application?

$$E = E0\_area * (1 - a^n) / [1 + (n-1)c]$$

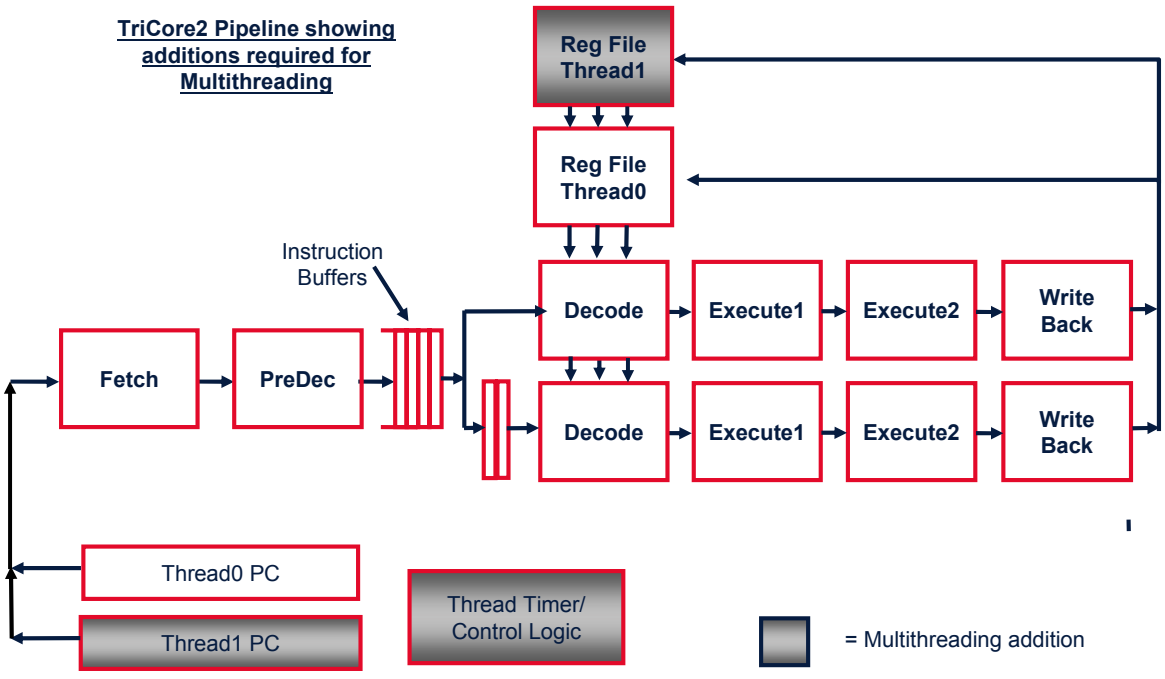
a: blocking probability
n: # of threads
c: area overhead



Infineon's Access Network Processor ConverGate™-C V1.1 Block Diagram

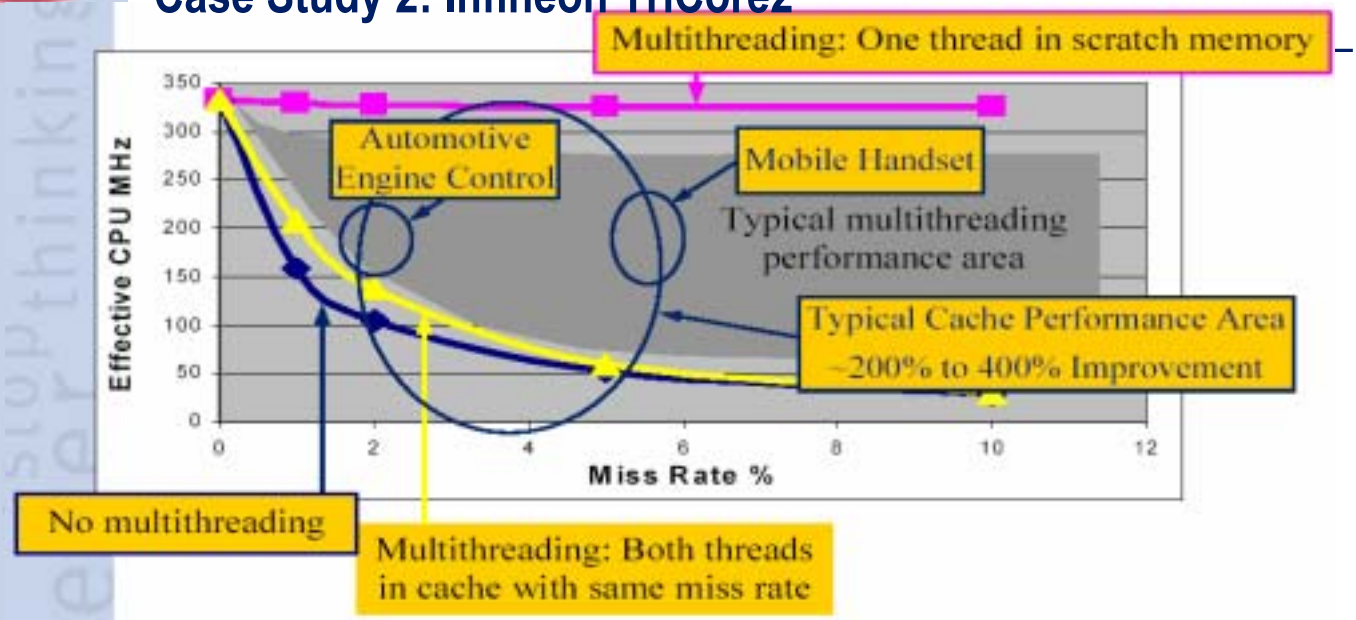


Case Study 2: TriCore 2 – Low Overhead Multi-Threading



~5% area overhead, <1% performance impact

Case Study 2: Infineon TriCore2



In all cases:

- CPU at 333MHz;
  66MHz 32-Bit Flash on Crossbar

TriCore2

Conclusions

- Multiprocessor is the way to go for scalability
- Multithreading is the way to go for optimized area-/power-efficiency
- Use the knowledge about the application in HW and SW architecture considerations

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