Converge to Silicon Success

DFM: Where Design, Lithography and Process Meet

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SYNOPSYS

Cost Relationships

Feature Size	Design Cost		Reticle Costs		Manufacturing Costs		Total	
	$M	%	$M	%	$M	%	$M	%
0.25 µm	2.12	13%	0.085	0.5%	14.18	86%	16.4	100
0.25µm	4.18	13%	0.195	0.6%	26.75	86%	31.2	100
0.13µm	6.37	13%	0.685	1.2%	48.16	87%	55.3	100
90 nm (300 mm)	10.73	22%	1.496	3.1%	35.96	74%	48.3	100

IBS May 2004

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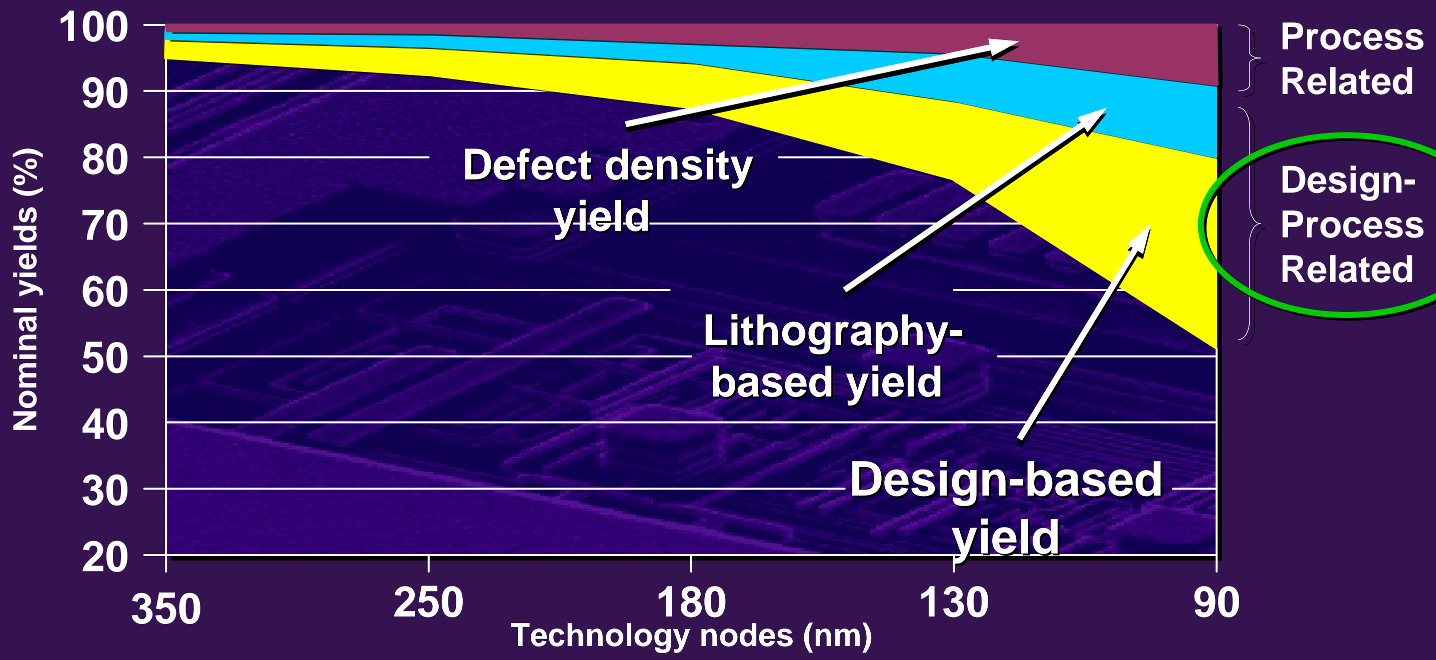
Yield



	Functional	Parametric
Random		
Systematic		

Source: IBS Report

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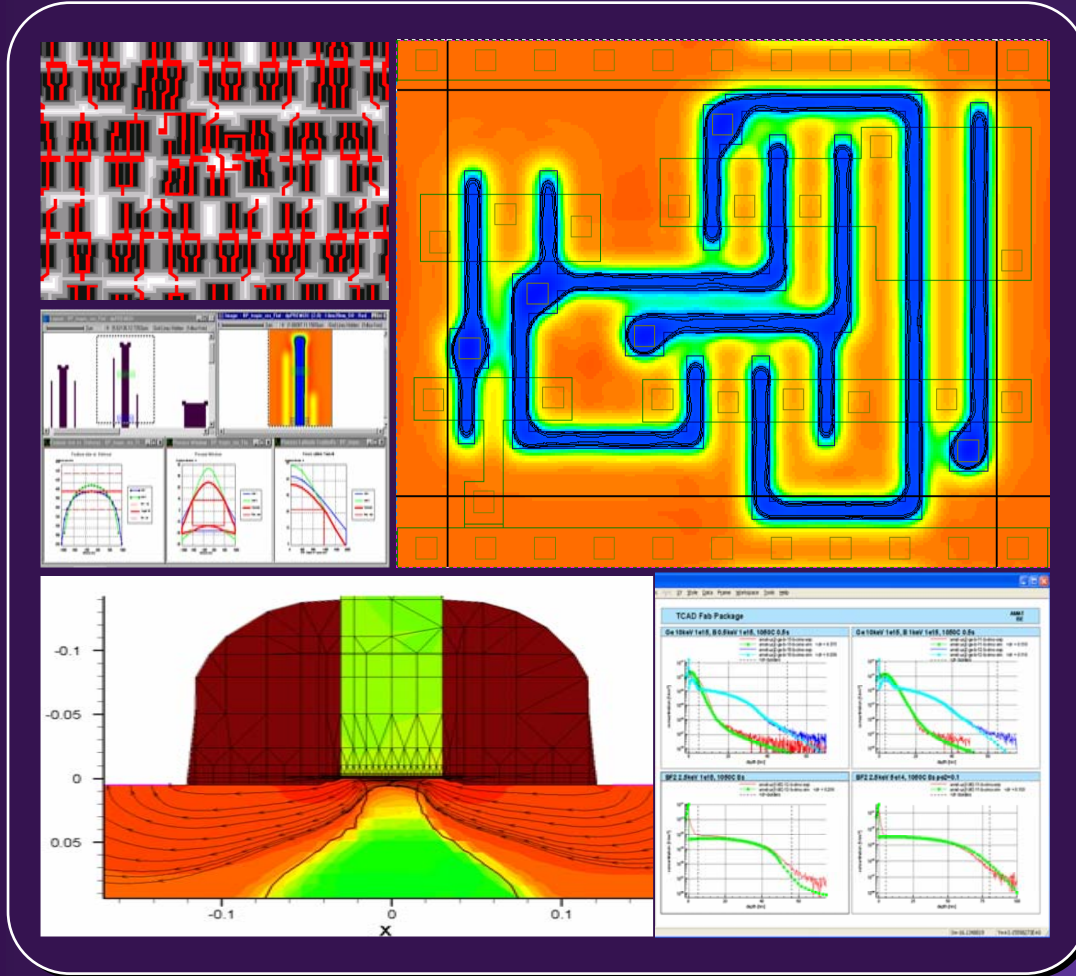
Manufacturability Becomes Key



- Implementation
- Physical Verification
- Mask Synthesis
- Mask Inspection
- TCAD

Process Litho Design

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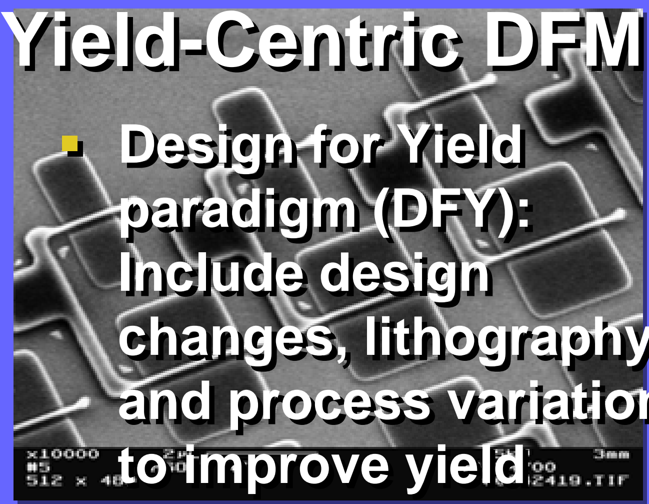
DFM: From Printability to Yield

- Litho-Centric DFM

  - Mask Synthesis paradigm (MS): The printed and processed feature should be as close as possible to the original design
  - Aspects of lithography and design are linked to enhance printability

- Yield-Centric DFM



  - Design for Yield paradigm (DFY): Include design changes, lithography and process variations to improve yield
  - Aspects of processing, lithography and design are linked for yield improvement

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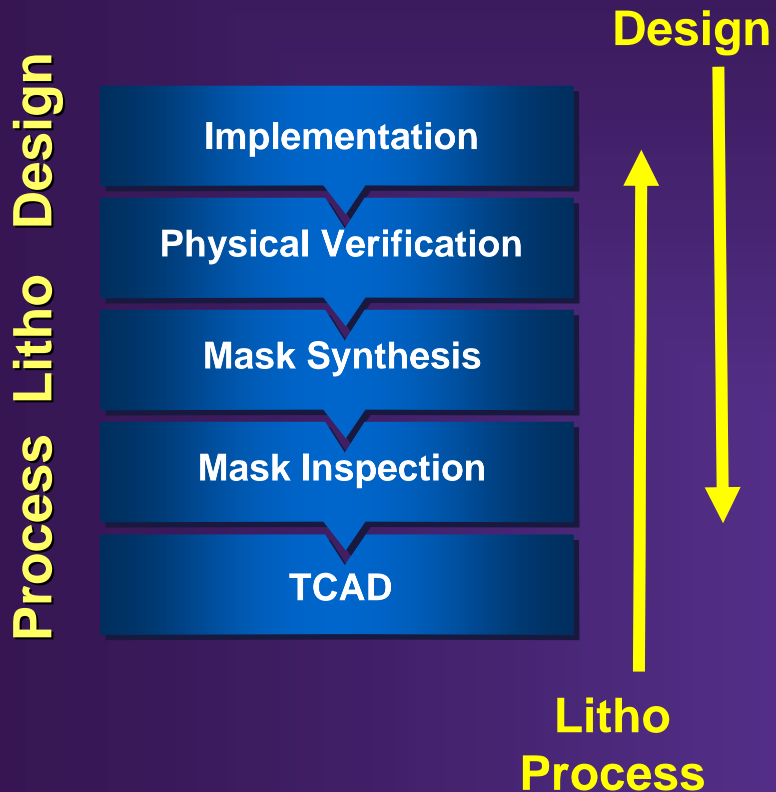
Where Can EDA Influence Manufacturability?



Design

Litho
Process

- Implementation
- Physical verification
- Mask synthesis
- Mask inspection
- TCAD

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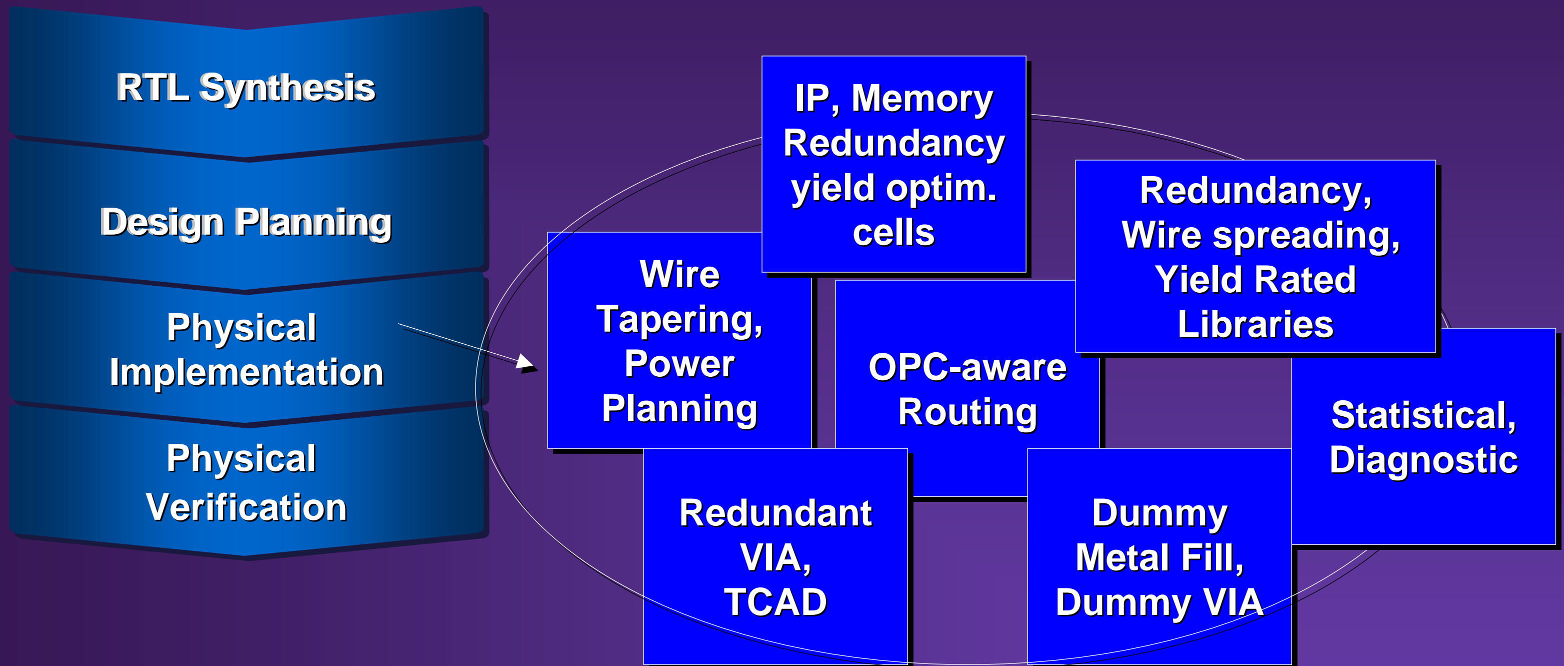
Yield Acceleration During Design



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Yield Aware Physical Synthesis

- Functional yield recovery during physical synthesis
  - Concurrent optimization for yield along with other timing, area, power and xtalk
- Requires yield characterized cell libraries
  - Yield for a gate varies
  - Driven by ANF* data in library

Cell Name	Area	ANF
BUF1	17.35	15.11303
BUF2	17.35	15.11303
BUF4	21.63	36.63756
BUF6	25.43	61.20557
BUF8	34.71	91.73009

ANF = Average Number of Faults [faults/billion]

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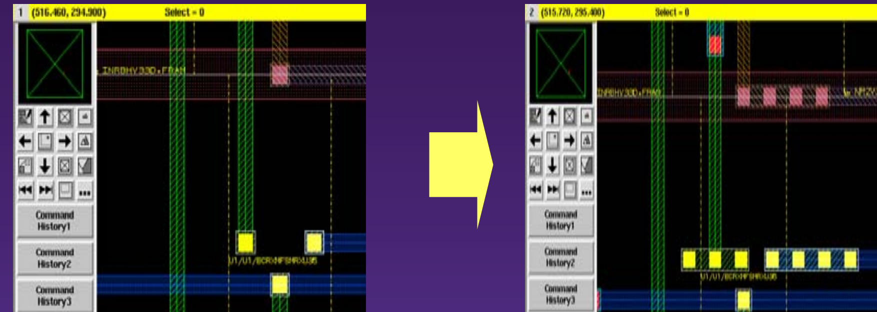
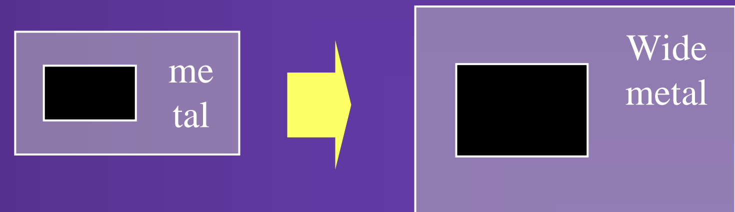
Examples in Physical Design

- Redundant via (post processing)
- Via array rule
- Wire spreading



- ***fatTblMinEnclosed AreaMode***



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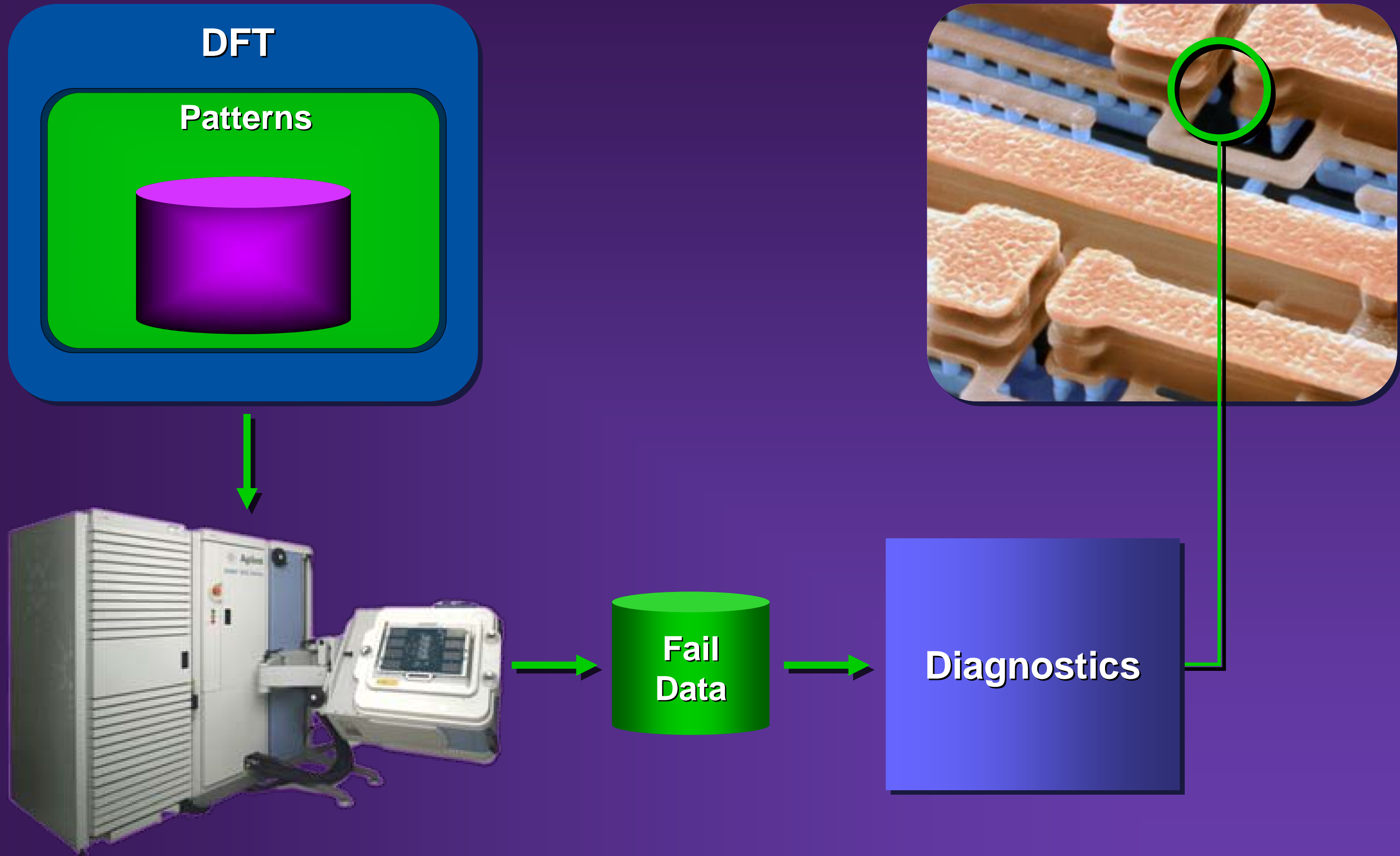
Enabling Faster Yield Ramp



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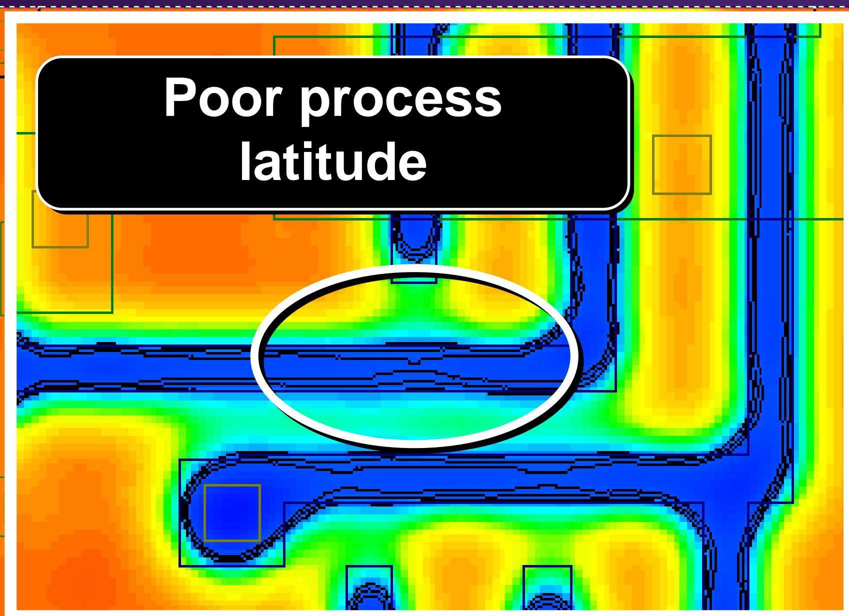
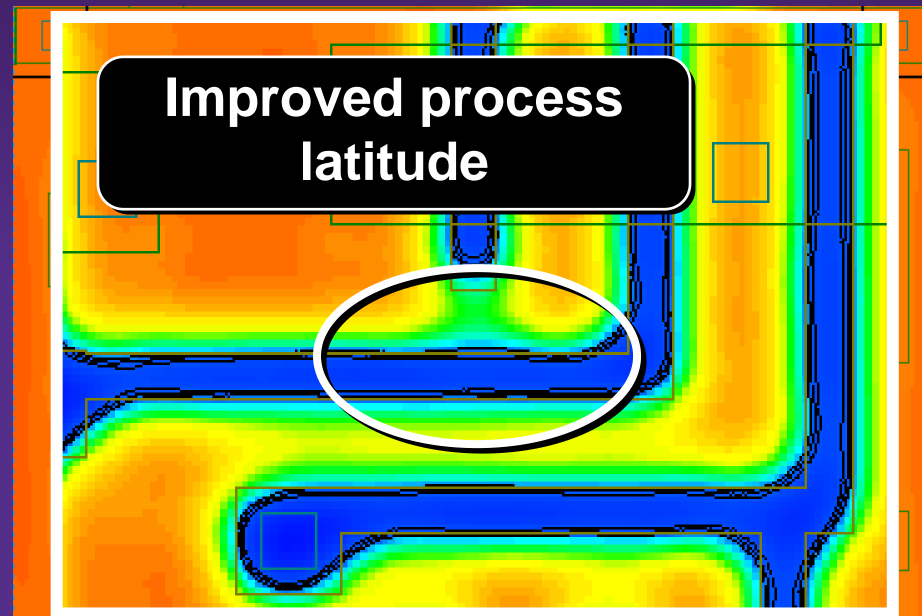
Courtesy IBM

Recommended Rules Improve Yield / Manufacturability

Layout created with Cadabra KAZAM	Layout migrated with Cadabra KAZAM SAME AREA





DRC correct - Minimum Spacing Rule	Recommended Spacing Rule

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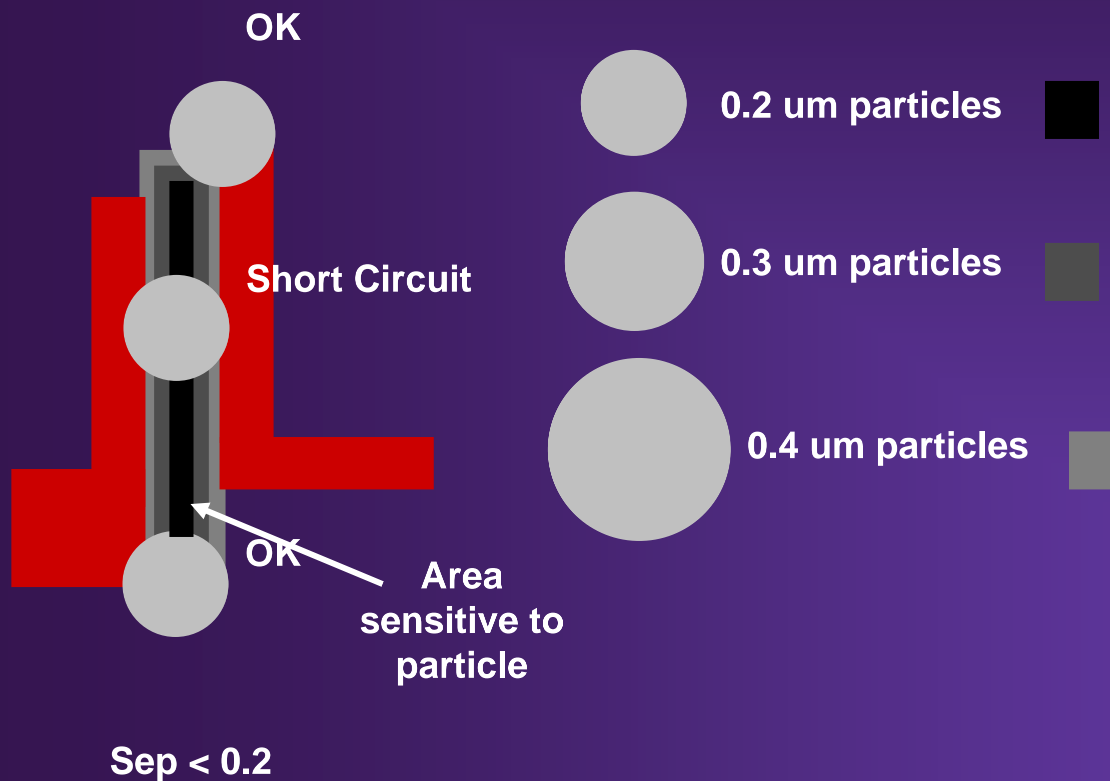
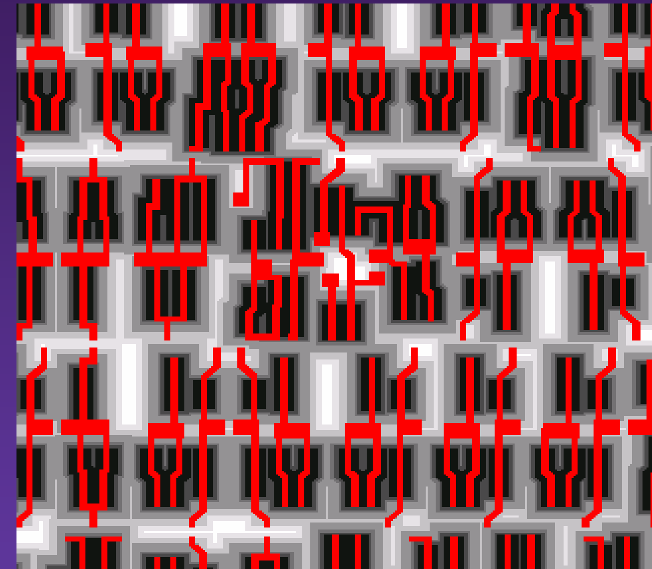
Yield Grading: Critical Area Estimation





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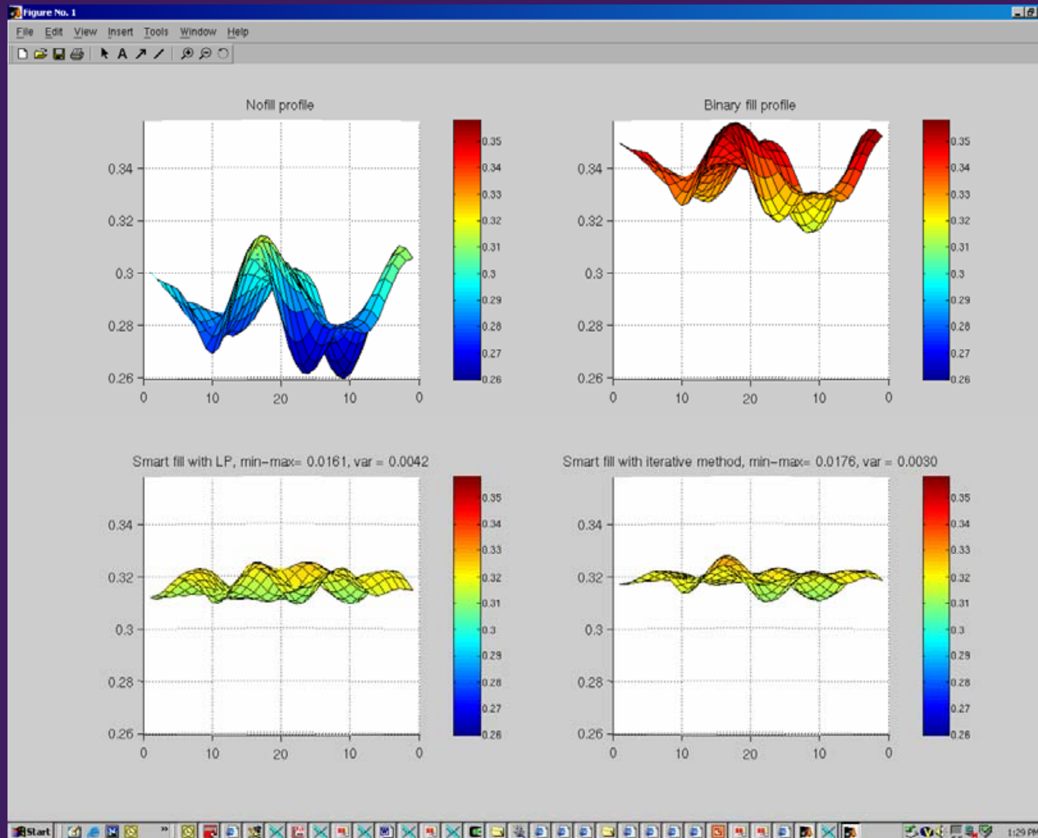
CMP Simulation and Metal Fill

Effective density profile

No-fill

rule-based filling



LP method.
(Optimal solution)

new method

LP:
Peak-Peak = 0.0161
Standard deviation
= 0.0042

New method:
Peak-Peak = 0.0176
Std = 0.0030

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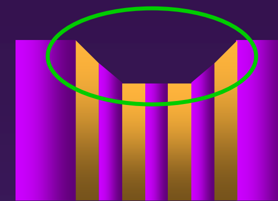
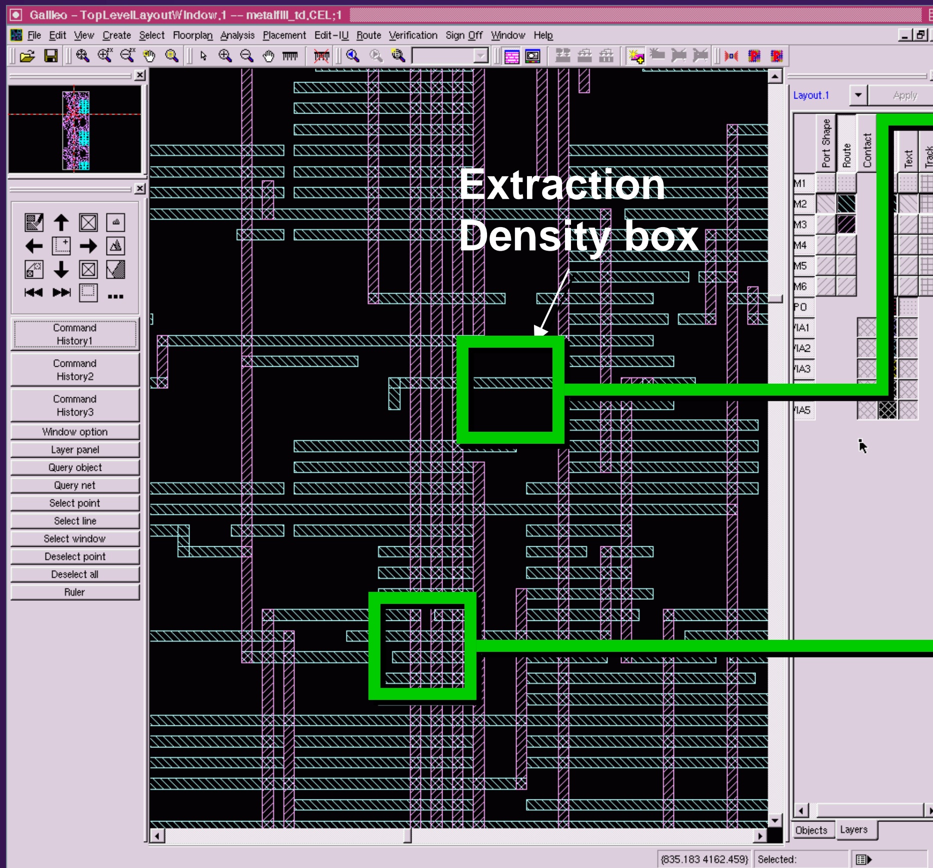
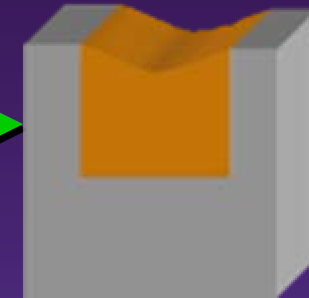
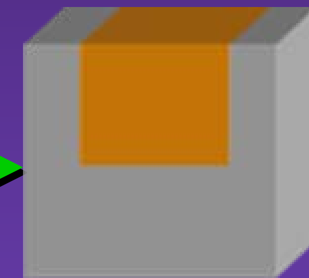
Accurate Modeling







Higher resistance due to dishing



Less resistance but more coupling cap

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Timing-Driven Metal Fill

Concurrent Yield And Timing Closure

Traditional M-fill
Density requirement: Met
Worst Path: +110ps
After M-fill: -10ps

Timing-Driven M-fill
Density requirement: Met
Worst Path: +110ps
After M-fill: +100ps

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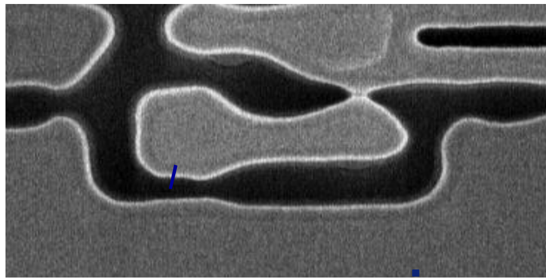
Need for Physical Verification Futures

Is My DRC-Clean Design Manufacturable?

DRC Clean Layout



Actual Silicon

Gate

?

PSM conflict

1 micron

1 micron

DRC Clean

Unwanted artifact due to light interference

Geometric rules do not capture all process constraints

PSM-check Verifies PSM compliance

Requires simulation based checks

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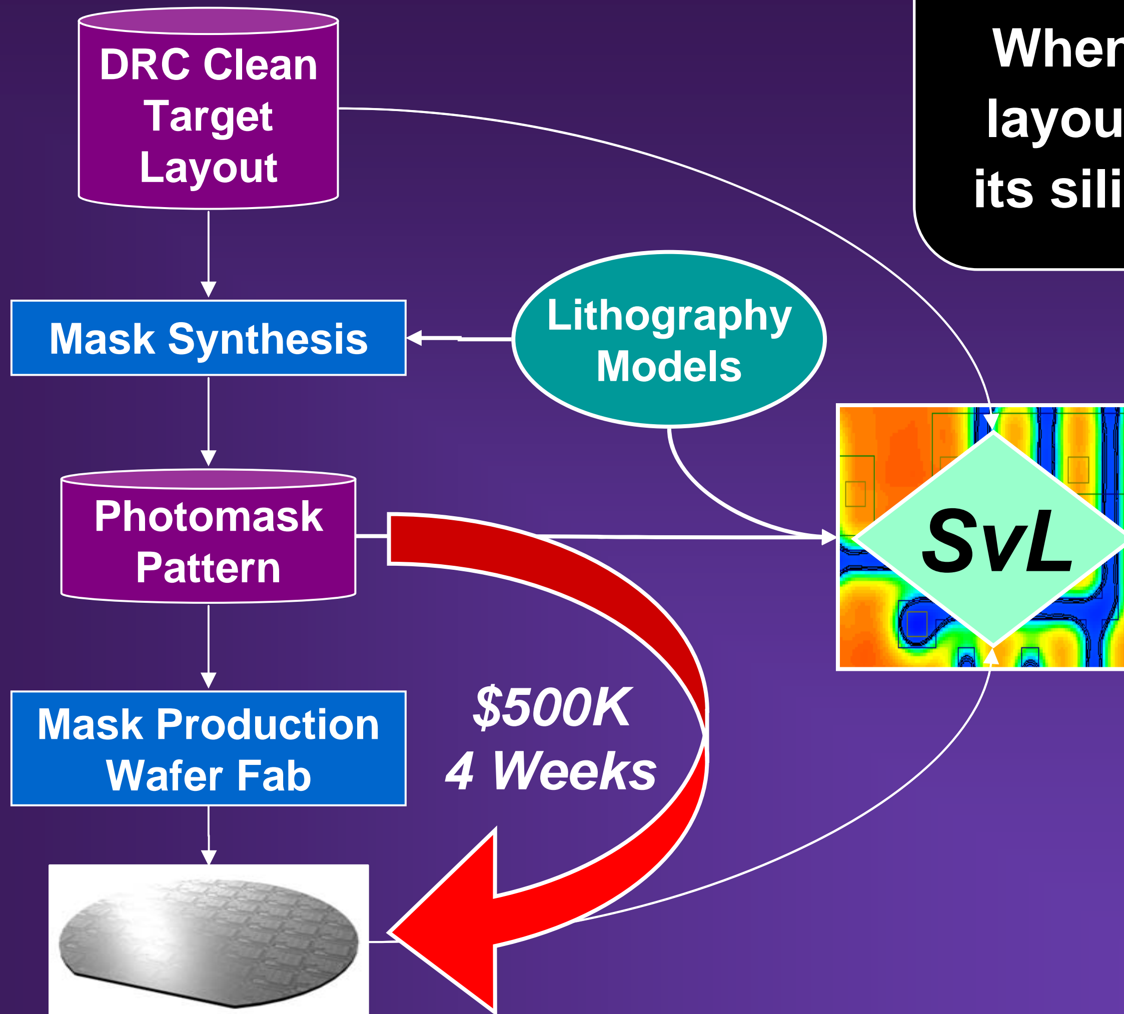
RET Closure



RET Closure:
When a design layout matches its silicon image

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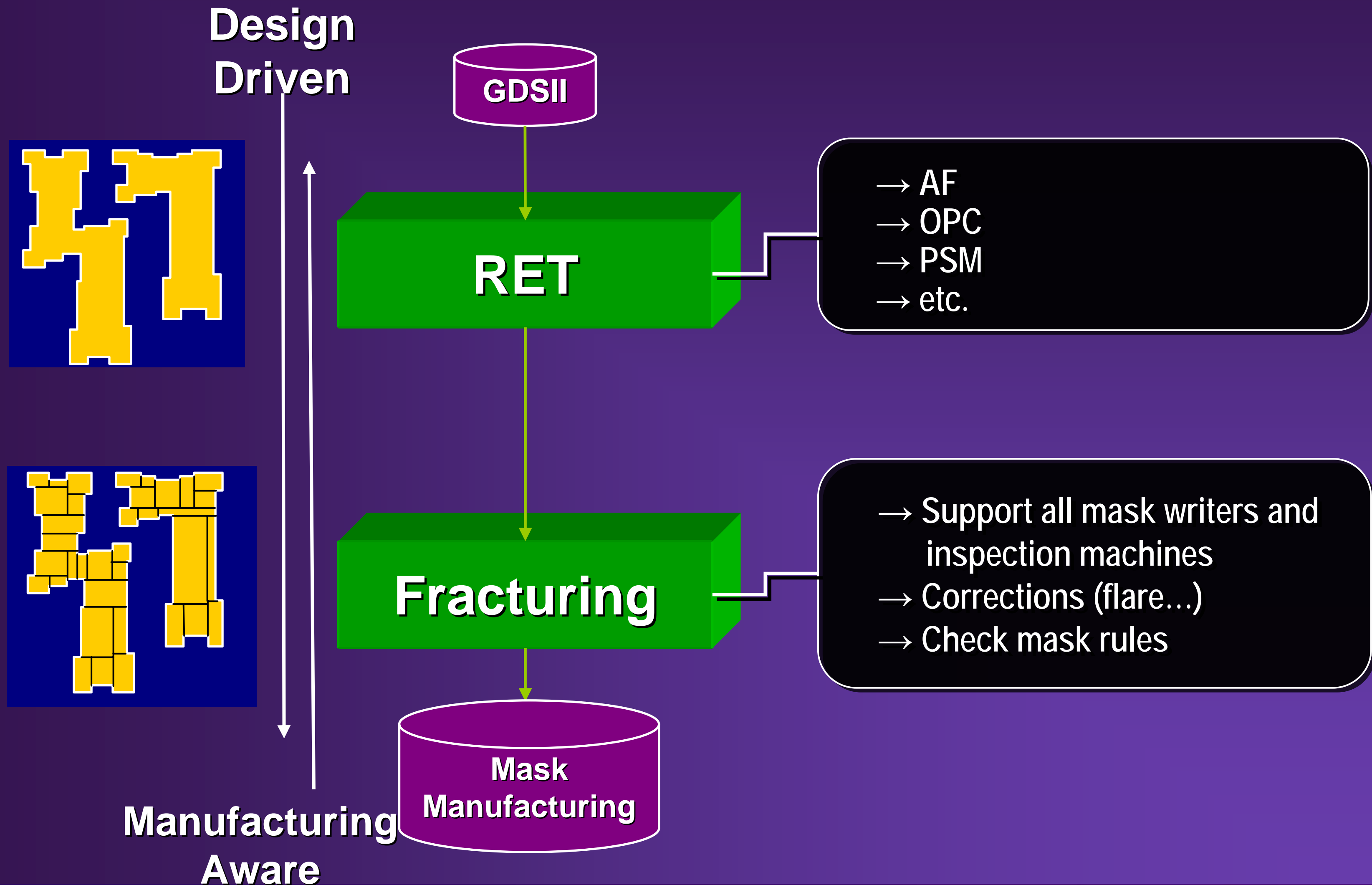
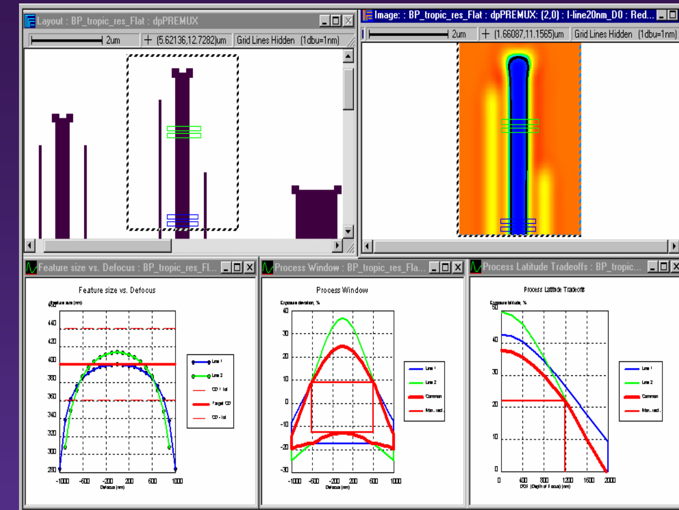
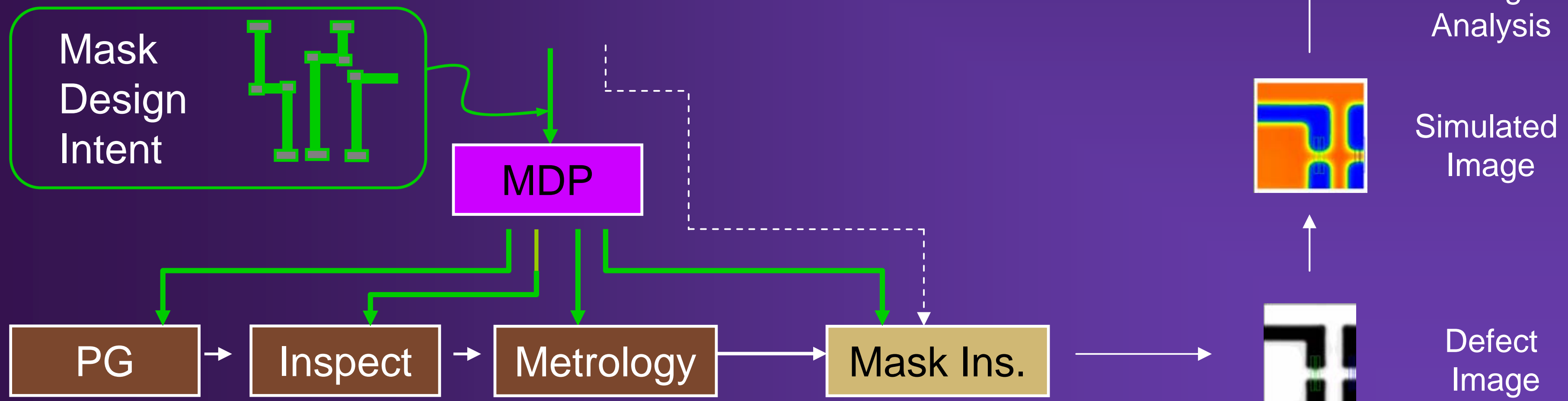
Mask Synthesis Flow



Mask Inspection

- **Uses simulation to determine effect of mask defect on silicon image without actual exposure**





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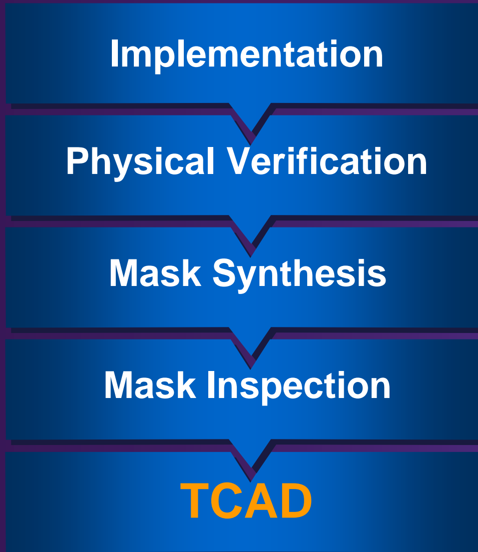
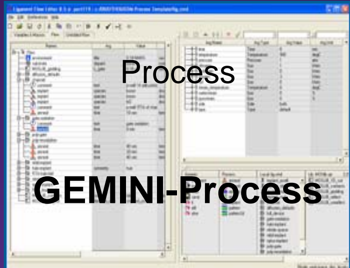
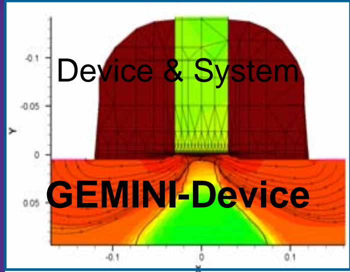
TCAD Links Process and Design

Process Litho Design



Layout & Process Recipe





Compact Model Extraction
Parasitics Extraction

Support
Consulting and Engineering

Examples
- Statistical Parameters
- Stress
- Reliability
- Accurate Device Extraction

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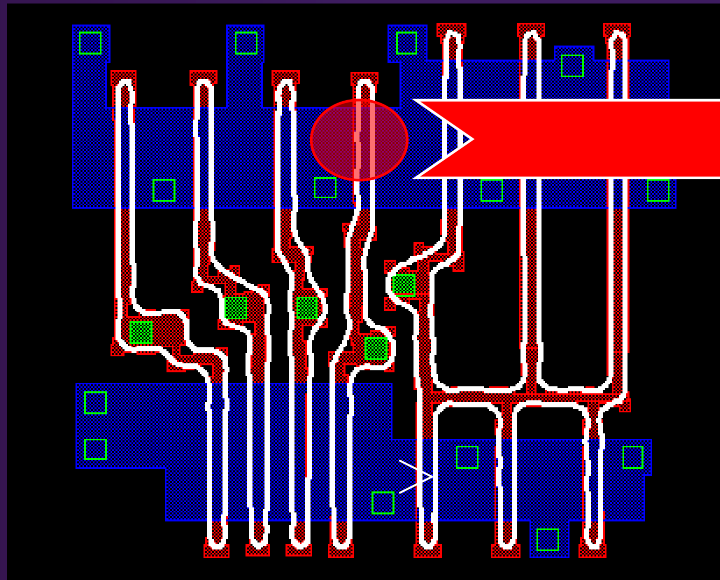
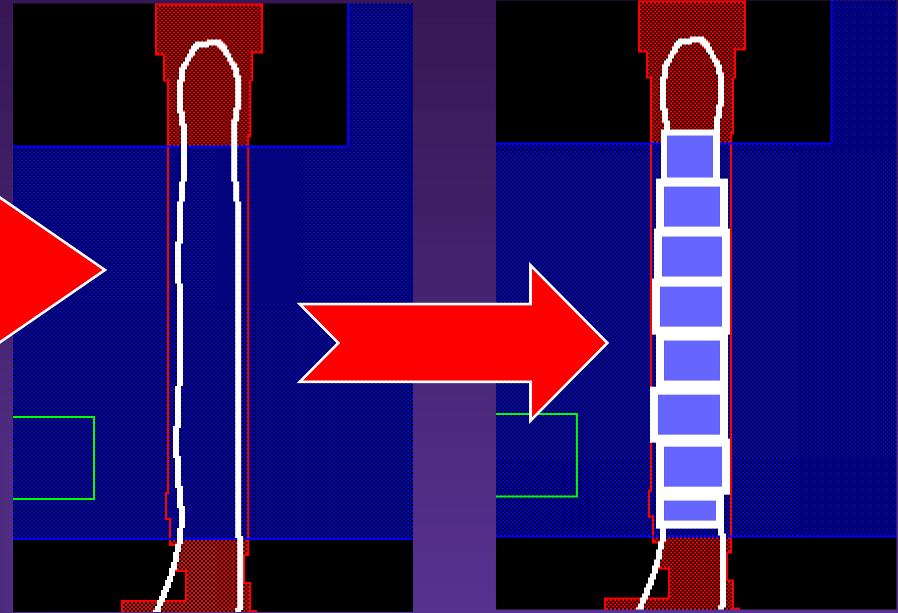
Accurate Device Extraction from Image



Actual image of poly layers



Device extraction

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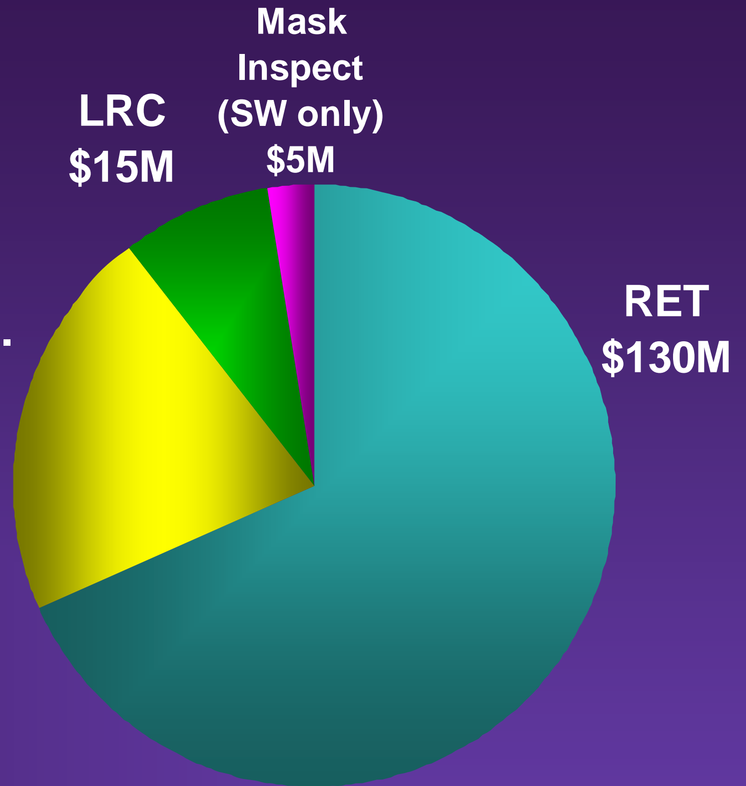
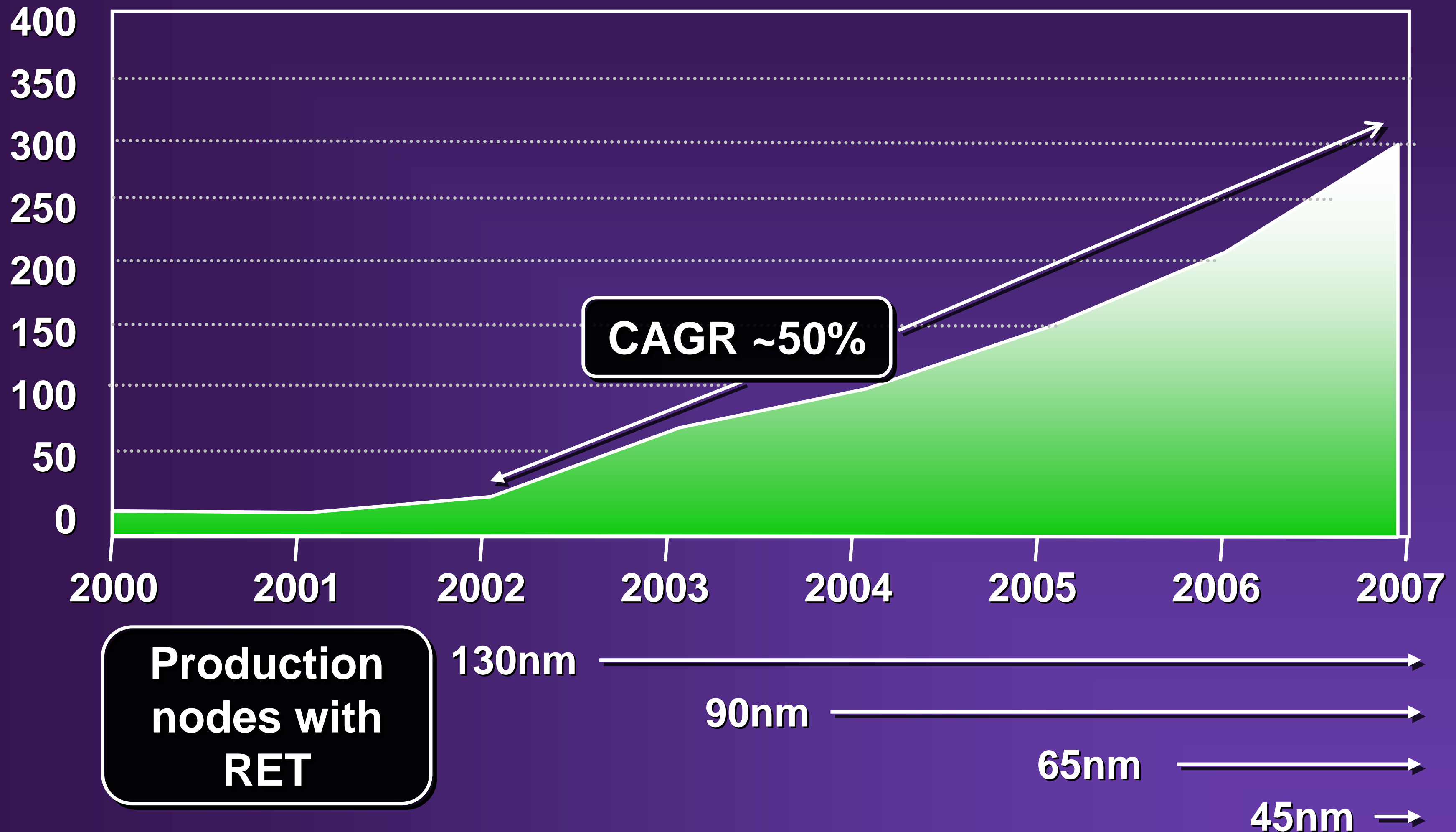


TCAD market: ~$50 million

Source: Internal estimates

RET Growth: Fastest Segment in EDA



Source: Industry estimates

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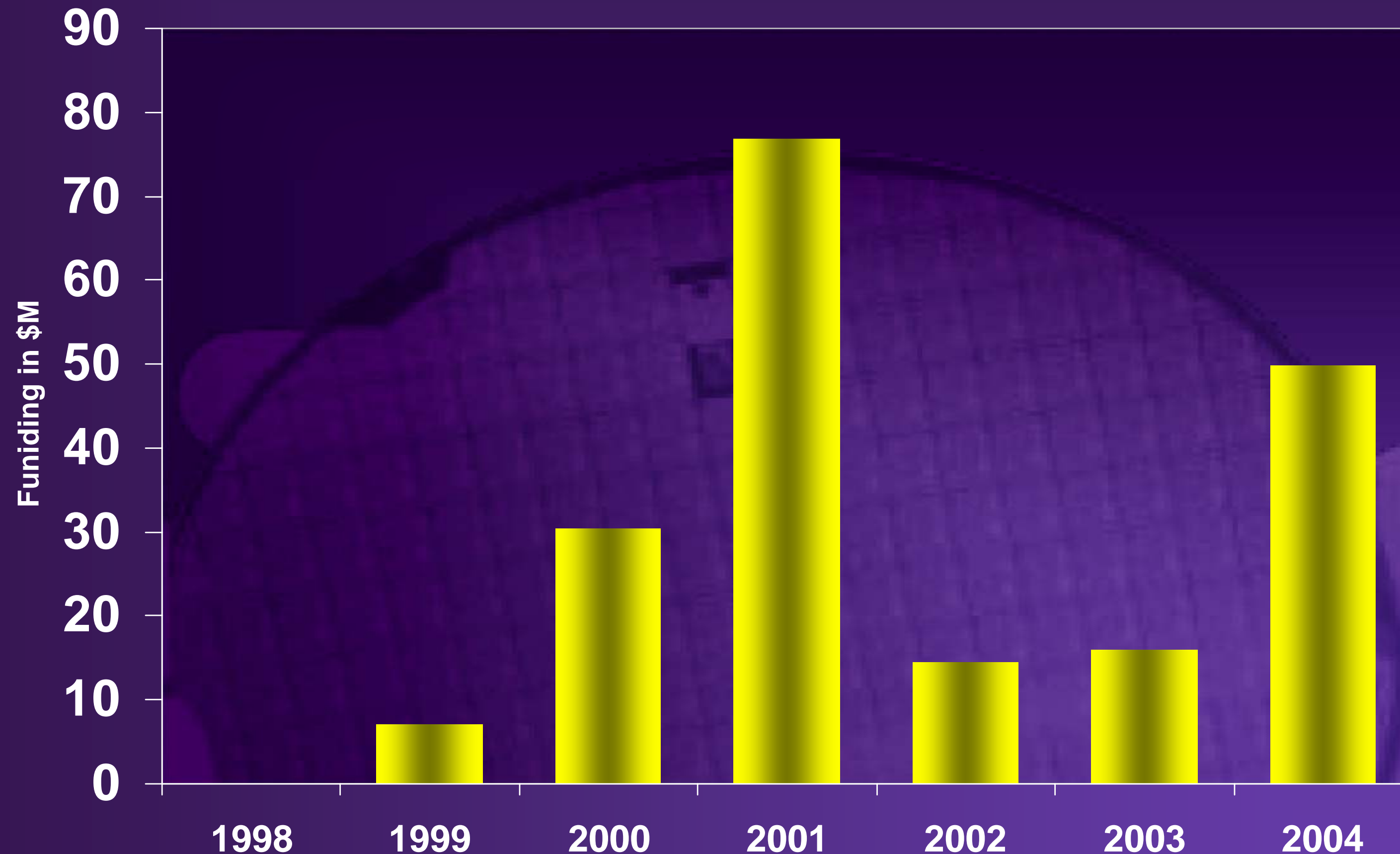
VC Funding in DFM Segment



Source: VentureSource Database-aggregate an
nual funding totals to date through 12/2004

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Design

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