NoC: the Arch key of the IP integration methodology

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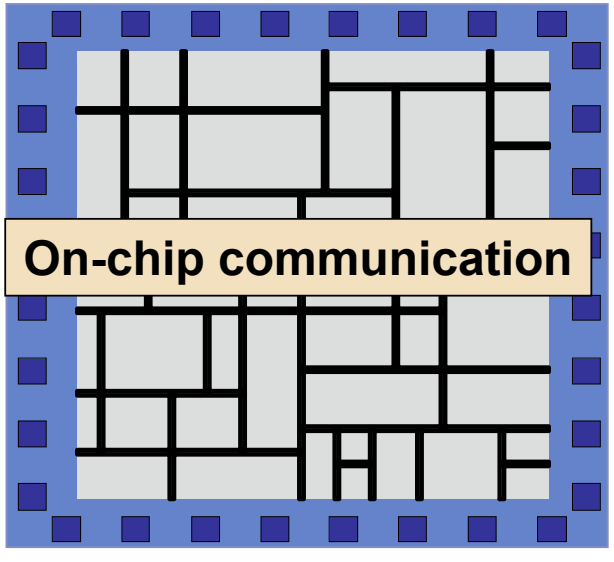
Chip Design Problem #2
Design Effort Š Chip Level



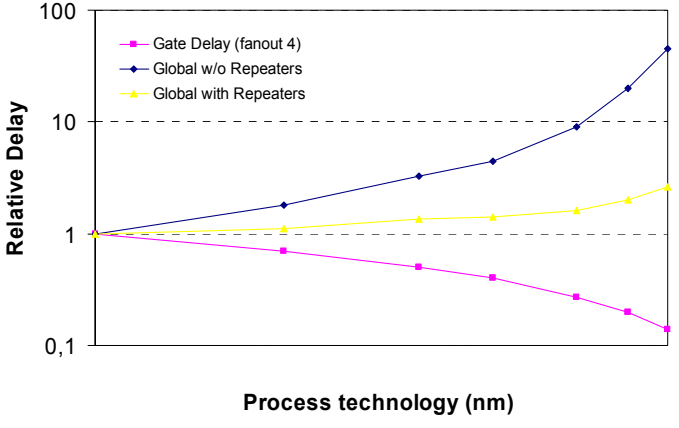
Putting the blocks together posed tough questions:

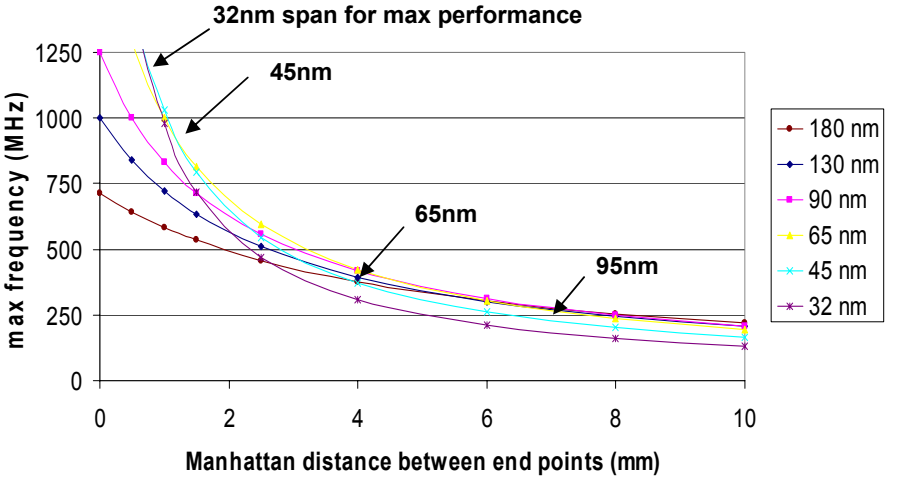
- Do the hardware interfaces work with one another?
- Do the chip have enough bus and memory bandwidth under worst-case loads?
- Do software tasks communicate without deadlock?
- Do all applications and features of the full system meet functional goals?
- Does the system meet performance goals? Is there headroom?
- Are the cost, power and memory footprint acceptable?
- What happens when (not if) bugs are found?

SoC in DSM

- **Challenges increase exponentially below 130 nm.**
  - CMOS Process performance impacts
  - SoC On-chip Communication design issues
  - IP Re-use

CMOS Process Performance Impact





- **Gates get faster – global wires (communications) get slower**
- **Process evolution forces clusters of IP building blocks**

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SOC On-chip communication design issues

- Timing closure, Cross talk, Wire routing congestion, SoC verification ….
- Compounded by the exponential increase of wires in the traditional approach; Buses
- Wire efficiency must be improved !!!

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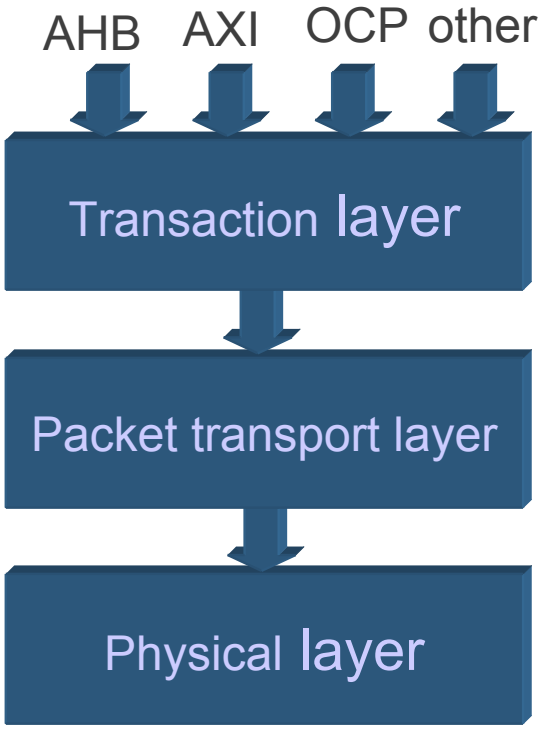
IP-Reuse

- **Challenges drive cost of IP Re-use - can impact silicon cost by a significant factor.**
  - Integration,
  - configurability,
  - Interoperability
  - verification
- **Designs MUST capitalize on existing IP libraries**
- **Communication MUST adapt to the IPs**

Arteris NoC layered architecture



Reconfigurable IP interface

IP reuse

Packet based protocol

Scalability
Flexible topology
Wire efficiency

Point to point links, GALS (Global asynchronous and locally synchronous)

Timing closure
Cross talk
Signal integrity

Independently optimized NoC layers

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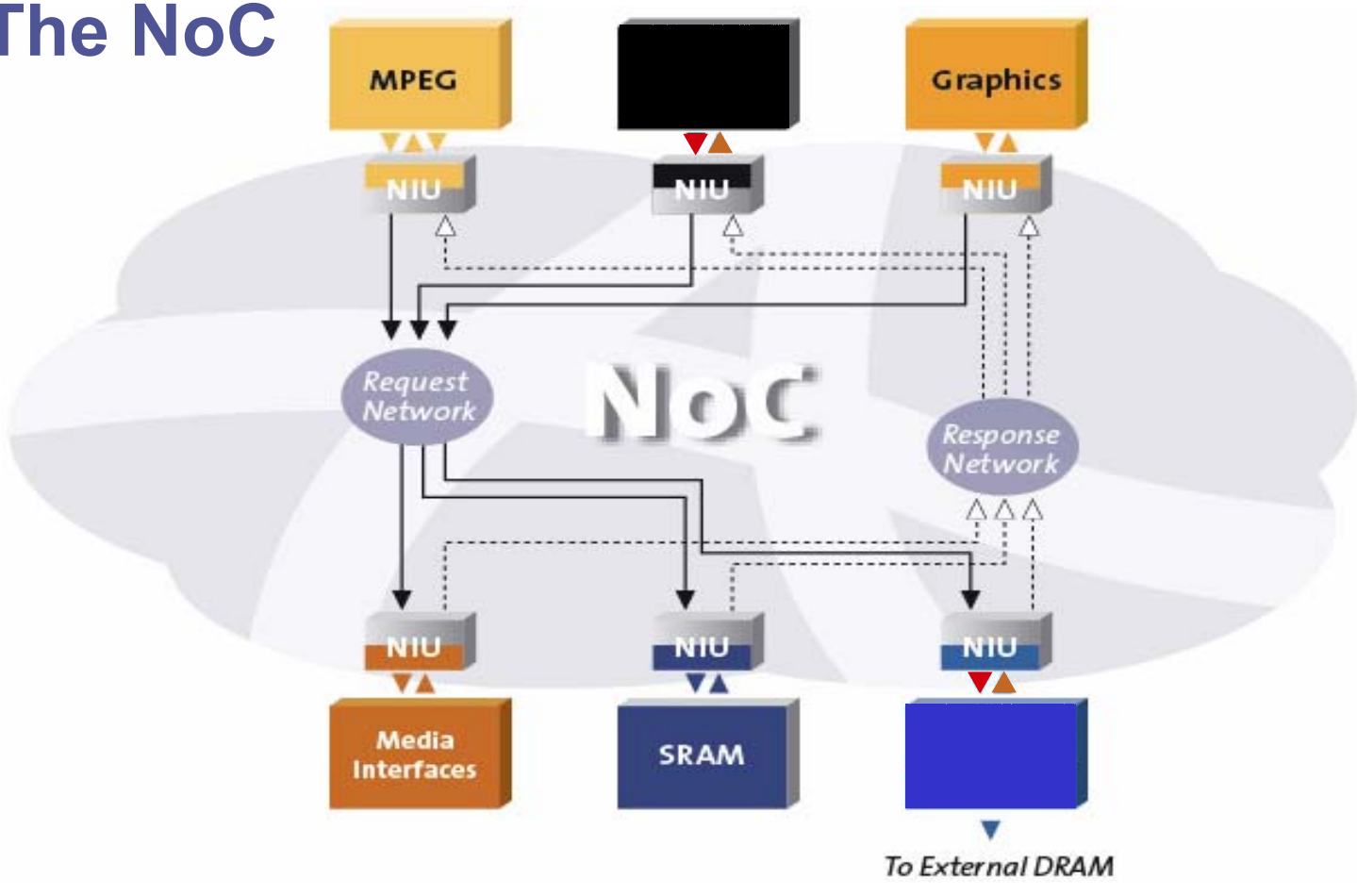
The NoC



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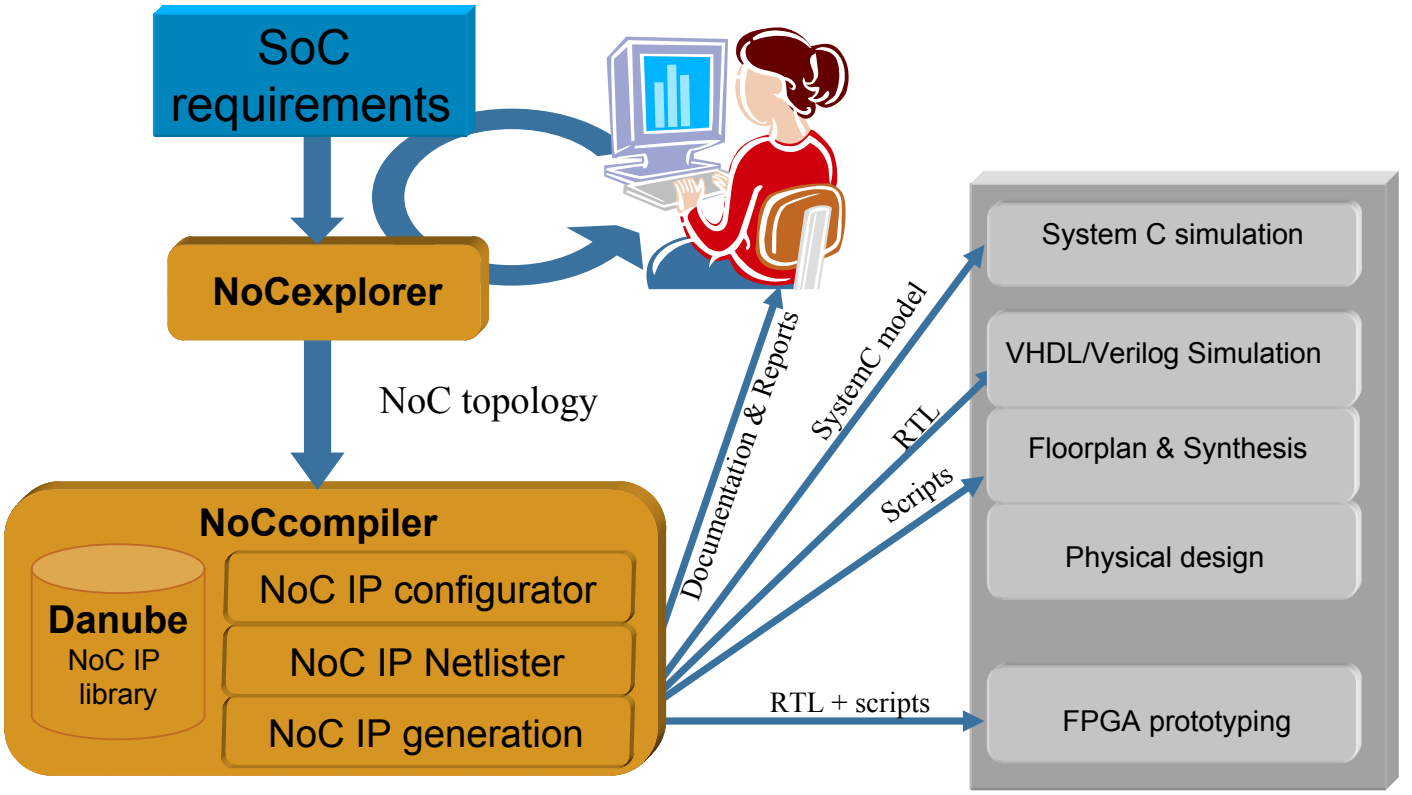
NoC integration with EDA design flow



Standard CAD Flow

Return On Investment

Higher because:
Higher performance
More Features
Resource allocated to value-added

Lower because:
Gates & wires saving

$$ROI = \frac{volume * (chip\ ASP - chip\ unit\ cost)}{Chip\ development\ cost}$$

Lower because:
Timing convergence speed-up
Faster iteration
Re-usability of IPs

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Enabling 90nm SoC Designs *and Beyond*

Alain FANET
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