Measuring SMP

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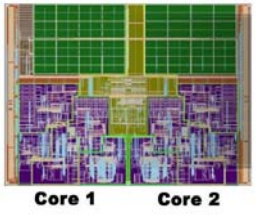
The Topic

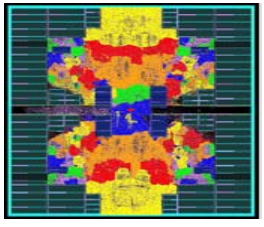
With symmetric multiprocessing (SMP) being asked to answer the hardware's challenge of power consumption and design cost, directly comes the question of logical vs. physical performance from the software designer. This talk takes a peak into the ongoing work inside www.eembc.org to bring a cross-platform industry standard benchmark suite for SMP devices. The comparison with uniprocessors, the challenge of portability and the layers of abstraction needed to show that your SMP device is the best!

The Industry Problem

- Something MPSoC has known for years…
  - Processors happy to work together get more done!

- Today, most embedded solutions have some form of MP, and many general processor sockets are also now moving to MP architectures.





- But….
  - How can I know really what performance I'll get from the solution?
  - How can I compare different hardware solutions?
  - What's the cost tradeoffs
  - ..and what about the efficiency of the middleware ?

EEMBC: Committee of Industry Players

Embedded Microprocessor Benchmark Consortium

Markus Levy
EEMBC President

Alan R. Weiss
EEMBC Certification Labs Chairman and CTO

Committee Chairs

Automotive/Industrial
Manfred Choutka, Infineon

Consumer
Sergei Larin, Motorola

Java
Graham Wilkinson, ARM, Inc.

Networking
Bill Bryant, Sun Microsystems

Office Automation
Ron Olson, IBM

Telecom
Gil Naveh, StarCore

8-/16-Bit Microcontrollers
David Lamar, NEC Electronics

Multiprocessor Benchmarks

Chair: John Goodacre
ARM Ltd.

Charter:

Extend the EEMBC benchmarking suite to provide a mechanism to comparatively compare the ability of devices to execute the multi-function, multi-task activities of rich embedded devices.

The Complexity of MP Benchmarking

- First hurdle, to classify the various forms of what is called MP?
  - SoC Multiple heterogeneous processor cores (eg MPSoC)
  - Uniprocessor with accelerators allowing synchronous offloading
  - Homogeneous multiple processor ‘farms / seas / nets / etc’
  - Multiple register-banked ‘threaded’ uniprocessors
  - Symmetric multiprocessors (of various forms)

Conclusion, benchmarking is about the costs of running software, so need to focus around a software model that encompasses MP - initial focus will be using the Symmetric Multiprocessors (SMP) software threading and shared data model. This also allows comparison with current uniprocessor solutions

But then many aspects to SMP

- Decomposition of a single task
  - This is where you take a single algorithm and parallelize it to share its workload between the multiple processors.

- Execution of multiple different algorithms concurrently
  - This looks more at how the bigger system, including the OS, handles the workloads from multiple concurrent algorithms.
- Execution of a single algorithm over multiple data sets
  - This looks again at the bigger system, but concentrates more on the data throughput, and how a system can handle multiple 'channels' of data.

Conclusion, We'd apply these three SMP techniques to individual and groups of existing EEMBC consumer benchmarks

Example Benchmarks

- Single task decomposition
  - Decoding MPEG4 using existing benchmark data sets
    - Using mid-grain parallelism
  - High-pass grey filter from the image processing benchmark
    - Working at a fine-grain level of parallelism
- Multiple data set
  - Decoding of multiple different jpeg images
    - As may occur when viewing a web page
  - Decoding of multi-channel audio
    - Uses a coarse-grain parallelism
- Multiple Algorithm
  - Concurrent execution of the tasks within a video/data conference
    - cjpg/djpg, mpeg encode/decode
  - STB/PVR - maybe….

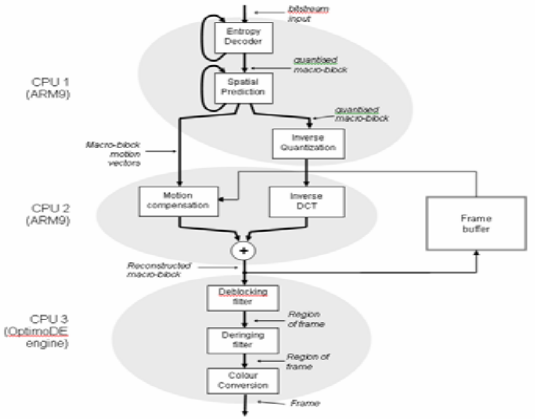
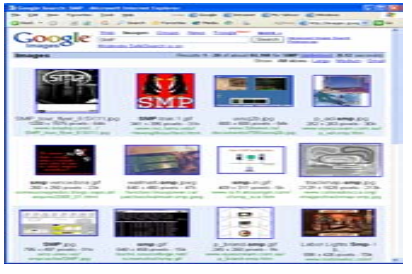
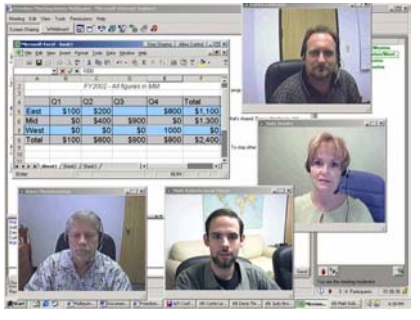


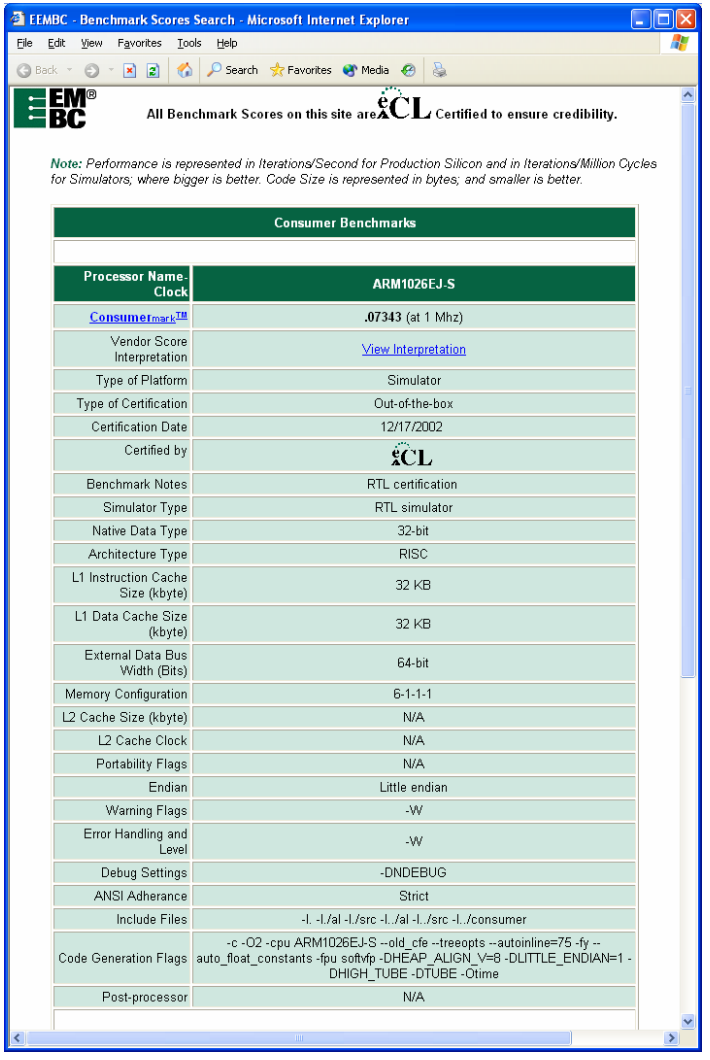
Figure 1: Data flow diagram of an MPEG-4 Decoder, partitioned across two ARM processors and OptimoDE





Reporting the results…

- Time to complete / MHz per iteration
  - CPU and bus frequency
- Tested platform type
  - Cache arrangement / sizes etc
  - Number of ‘processors/threads’ available in the hardware
- Processor die area
- Code image size
- Memory type and performance / latency
- AAL implementation version
  - (this is the thread API abstraction layer)
- OS version
- Tools version and flags etc.
- Number of thread used by the benchmark (user defined)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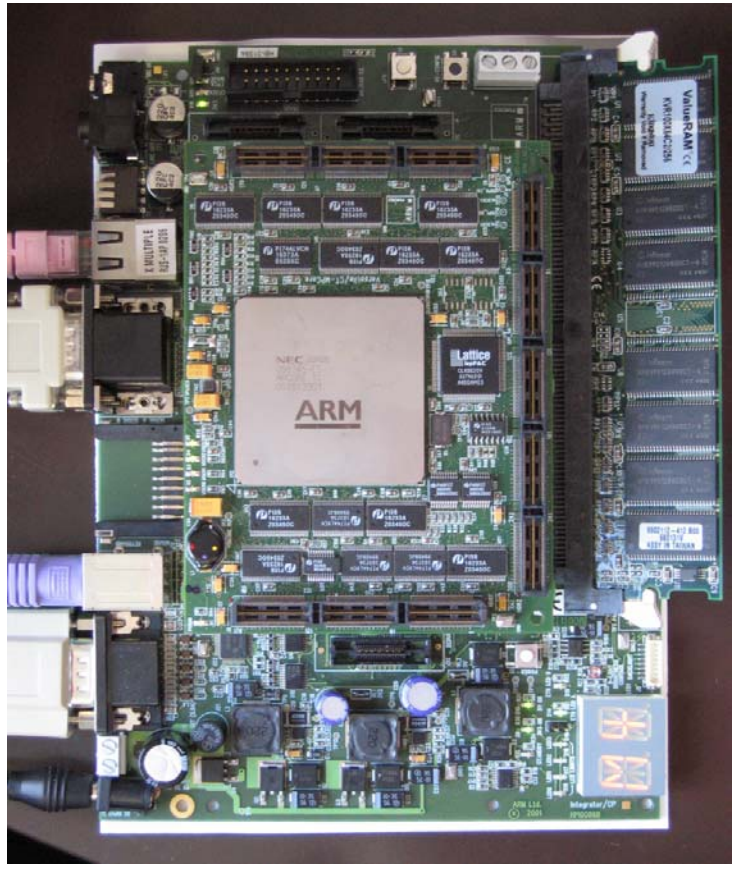
Note: Performance is represented in Iterations/Second for Production Silicon and in Iterations/Million Cycles for Simulators; where bigger is better. Code Size is represented in bytes; and smaller is better.

Consumer Benchmarks

Processor Name-Clock	ARM1026EJ-S
Consumermark™	.07343 (at 1 Mhz)
Vendor Score Interpretation	View Interpretation
Type of Platform	Simulator
Type of Certification	Out-of-the-box
Certification Date	12/17/2002
Certified by	EEMBC
Benchmark Notes	RTL certification
Simulator Type	RTL simulator
Native Data Type	32-bit
Architecture Type	RISC
L1 Instruction Cache Size (kbyte)	32 KB
L1 Data Cache Size (kbyte)	32 KB
External Data Bus Width (Bits)	64-bit
Memory Configuration	6-1-1-1
L2 Cache Size (kbyte)	N/A
L2 Cache Clock	N/A
Portability Flags	N/A
Endian	Little endian
Warning Flags	-W
Error Handling and Level	-W
Debug Settings	-DNDEBUG
ANSI Adherance	Strict
Include Files	-I. -I./al -I./src -I../al -I../src -I../consumer
Code Generation Flags	-c -O2 -cpu ARM1026EJ-S --old_cfe --treeopts --autoinline=75 -fy --auto_float_constants -fpu softvfp -DHEAP_ALIGN_V=8 -DLITTLE_ENDIAN=1 -DHIGH_TUBE -DTUBE -Otime
Post-processor	N/A

Thank you

..and a photo of ARM11 MPCore at work!



Quad-core MPCore @ 300MHz (testchip)
32K Instruction & 32K Data L1 cache
1Mbyte L2 (optional)
1500 DMIP aggregate performance @ ~600mW - The highest performance ARM !