SOC Design Foundry

Youn-Long Lin

Department of Computer Science

National Tsing Hua University

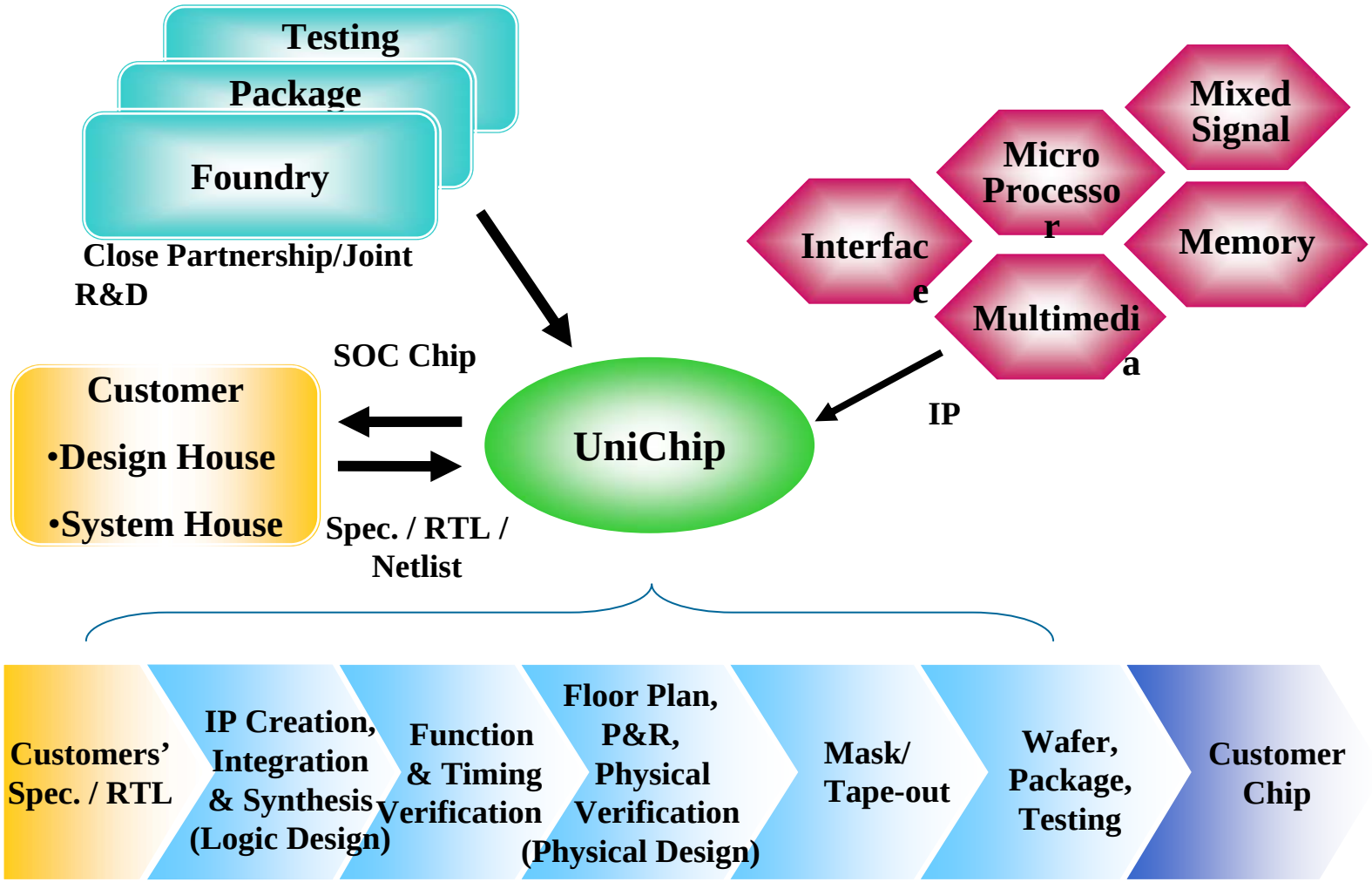
Taiwan

- Wafer Foundry
  - Huge Capacity
  - Increasing Service Items
    - Wafer Processing
    - Mask Tooling
    - Library
    - Macros
    - …

- Electronics System Houses
  - Huge Demand
  - Low Margin
  - Need Differentiator

BusinessWeek May 16, 2005

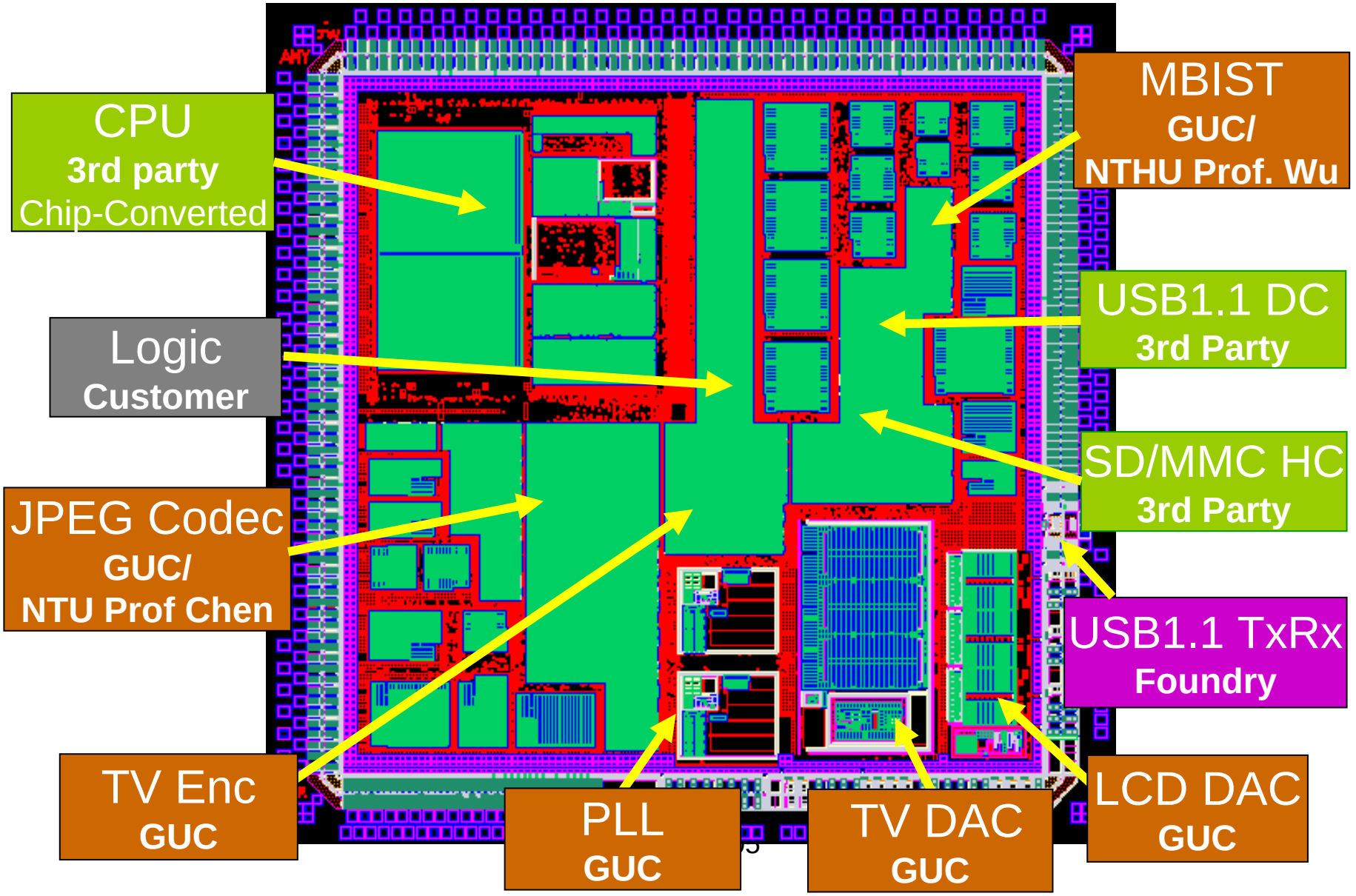
SOC Design Foundry



A Case Study

- Target ASIC: **3M pixel DSC controller for 2002**
- Technology: **0.25um 1P5M CMOS Logic Process**
- Complexity: **300K gates, 128/81MHz, TFBGA256**
- IP Sources:
  - Six Internal IPs: **JPEG Codec, MBIST**, **PLL, 8-bit LCD DAC, 10-bit TV DAC, TV encoder**
  - Two 3rd party IPs licensed by GUC: **USB1.1 TxRx, 10-bit ADC**
  - Three 3rd party IPs licensed by customer: **USB 1.1 DC, CPU processor, and SD/MMC host**
- Schedule:
  - 10 months from initial contact to mass production
  - Two tape-outs: **Test chip & Mass production chip**
- ~3.5M units over 1.5 years for 8% WWMS

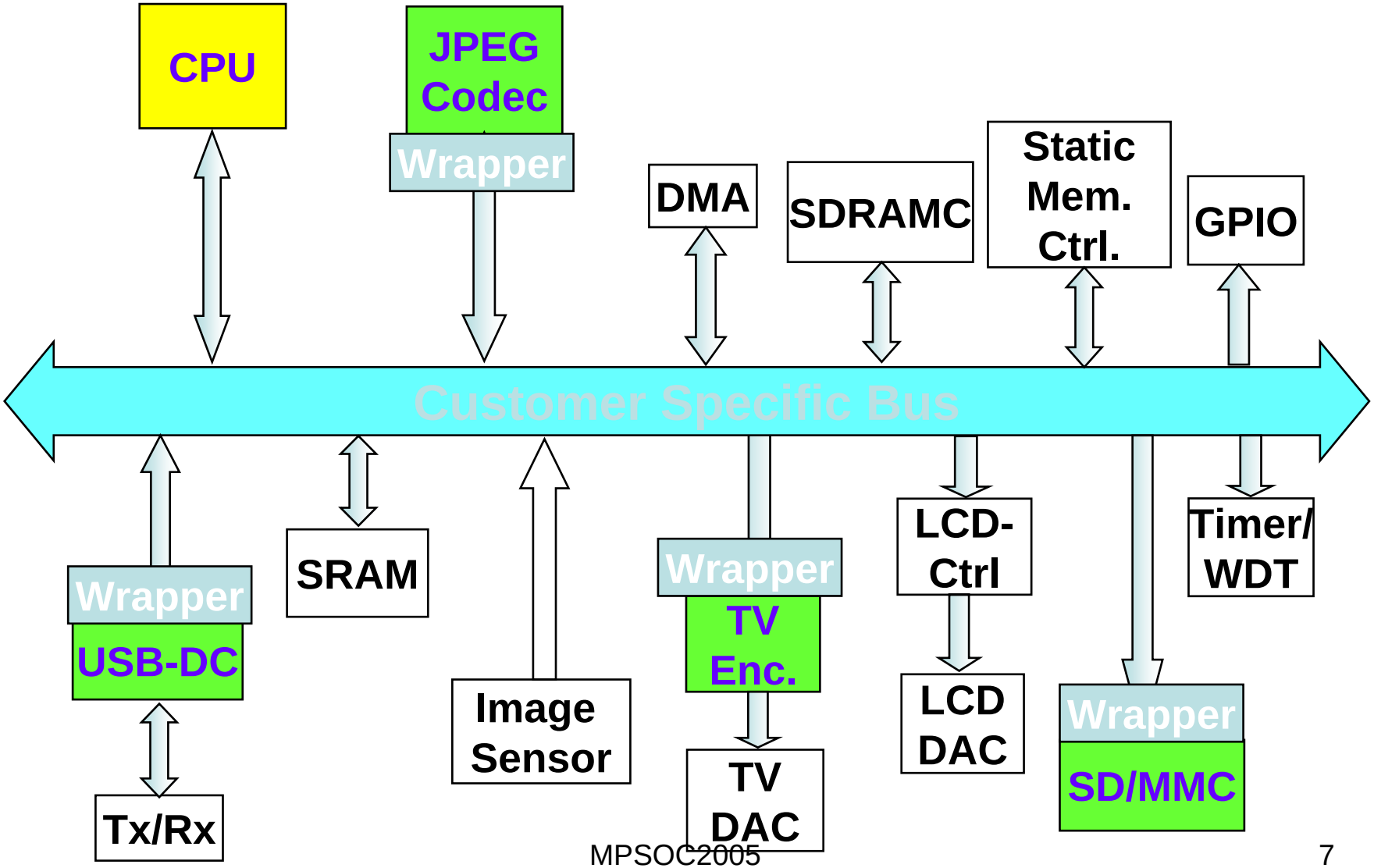
IP Usage


CPU
3rd party
Chip-Converted
Logic
Customer
JPEG Codec
GUC/
NTU Prof Chen
TV Enc
GUC
PLL
GUC
TV DAC
GUC
LCD DAC
GUC
MBIST
GUC/
NTHU Prof. Wu
USB1.1 DC
3rd Party
SD/MMC HC
3rd Party
USB1.1 TxRx
Foundry

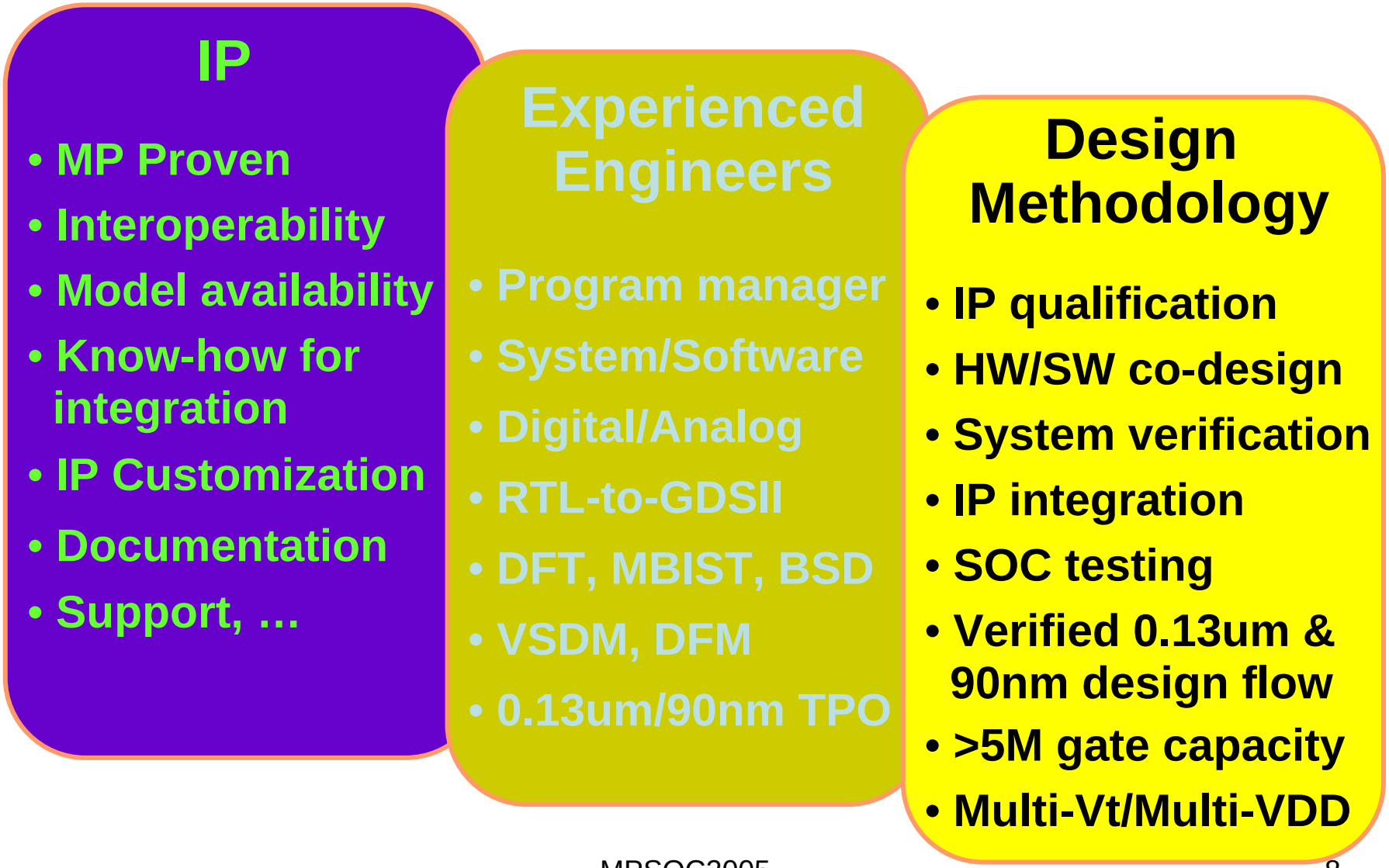
Concerns on IP Usage

- How to qualify 3rd party's IP?
- How to assure their functional correctness?
- How to do IP testing and pattern generation?
- Inconsistent EDA tool versions among customer, IP vendors, and GUC.
- How to do system validation?

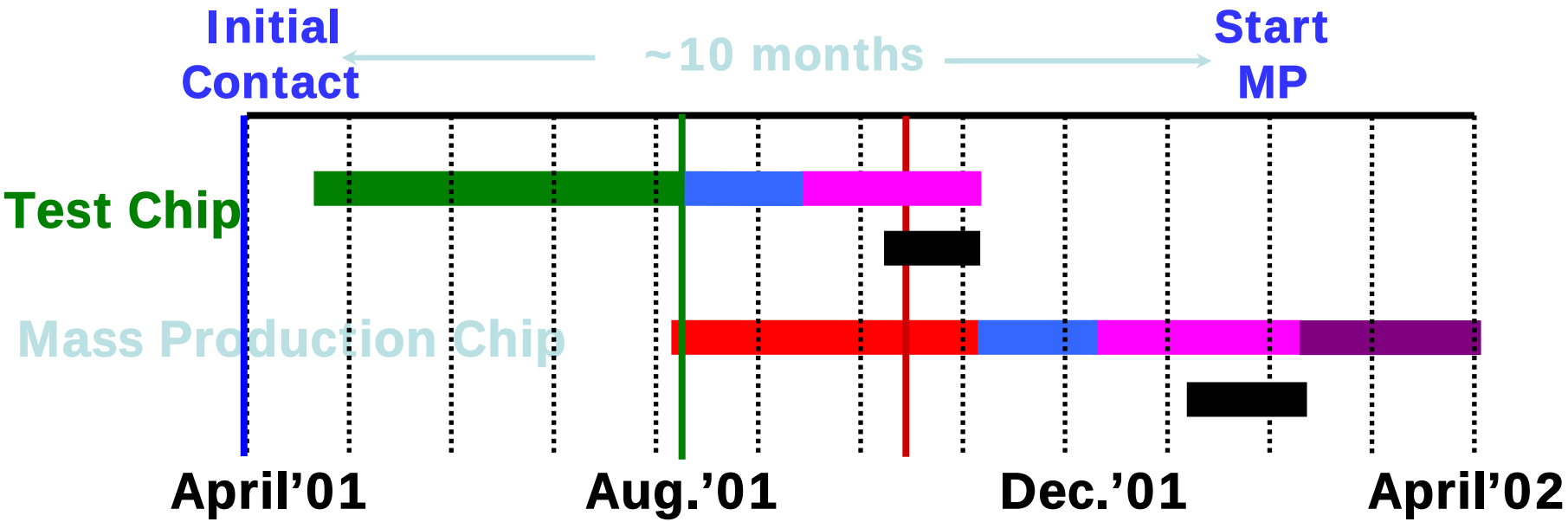
IP Development & Integration Platform



SOC Design Challenges



Schedule



Test chip design:

MP chip design:

Wafer Foundry pilot run:

System verification:

Wafer Foundry production run:

Reliability test:

Major Issues

- Inconsistent simulator tool versions
  - Customer uses PC-based verilog/modelsim. GUC uses NC-verilog as golden simulator
- Too many versions of pin sequence/pad type
  - Did much effort to save substrate cost (from 4-layer to 2-layer)
- No good SOC testing solutions
  - Muxed-out the IPs
  - Run the converted patterns under whole-chip environment

Industrial-Academy Collaboration

JPEG Encoder/Decoder

- Collaboration model
  - NTU: Develop JPEG Encoder and Decoder
  - GUC: Add new features to Enc./Dec., Integrate Enc./Dec. to Codec (share SRAM & DCT)
- New Features:
  - Support encode/decode with Restart Marker, user-defined Quan. table & Huffman table.
  - Add JPEG controller and reg. bank, AHB wrapper
  - Hardware address generator for the conversion from block order to raster order.
- Silicon proven and mass production
- # of customers: 6 (Enc: 2, Dec: 2, Codec: 2)

Memory BIST

- Collaboration model
  - NTHU: Methodology develop., tool & GUI, Alpha QA
  - GUC: Beta QA, test chip, feature enhancement, flow automation, integration utility
- Features:
  - Multi-port architectures, programmability, diagnosis, HW sharing, test scheduling, support various mem.
- Patent:
  - “Programmable Built in Self Test for Embedded Memory DRAM.” US Patent number: 6415403.
- Max # of memories handled:
  - 300+ at 0.13um process.
- # of projects implemented: 50+

Low Power Solution

- Process/library selection
  - Process Selection (G, LP, LV…)
  - Library Selection (Multi Voltage, Multi-Vt)
- Dynamic power optimization solution
  - Gated clock, clock buffer optimization
  - Power domain, skew balance
  - Glitch-free gating clock customized cell
- Leakage power reduction solution
  - Multi-Vt, sleep-mode, power plane
- Multi-Vdd + Multi-Vt Flow
  - Clustered voltage scaling, Timing modeling
  - Level shifter, Cell design

Summary

- **Bridges the gap between electronic system house and semiconductor foundry with SOC integration and verification**
- **Quite risky to employ 3rd party IPs, especially for those IPs not from professional IP vendors**
- **Immature SOC testing solution**
- **Successful industry-academy collaboration**
- **Low power solution, the key factor for successful SOC design**