Specification and Validation for Heterogeneous MP-SoCs

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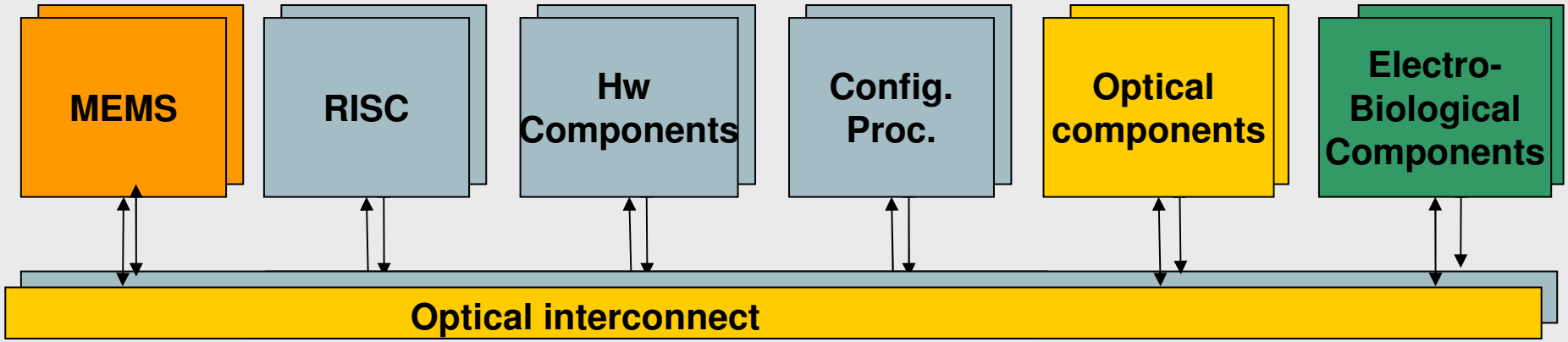
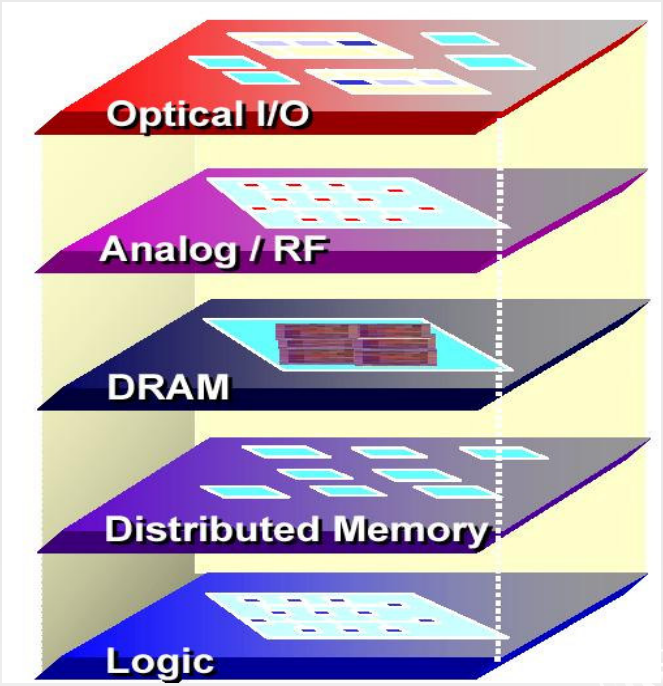
Heterogeneous SoC

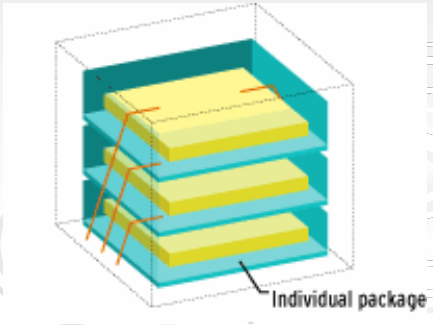


- ✓ Paradigm shift
- ✓ SoCs are drivers for several technologies integration
- ✓ Applications – automotive, communications, medical, defense

New technologies for heterogeneous SoC

- 3D System In Package Integration
  - Specific components are fabricated on individual wafers and then integrated onto a single chip-scaled package
  - Benefits
    - Increased performance
    - Increased integration density
    - Reduced power consumption
  - Wireless communication schemes
    - Based on Capacitive coupling
    - Based on Inductive coupling
  - New system-level trade-off



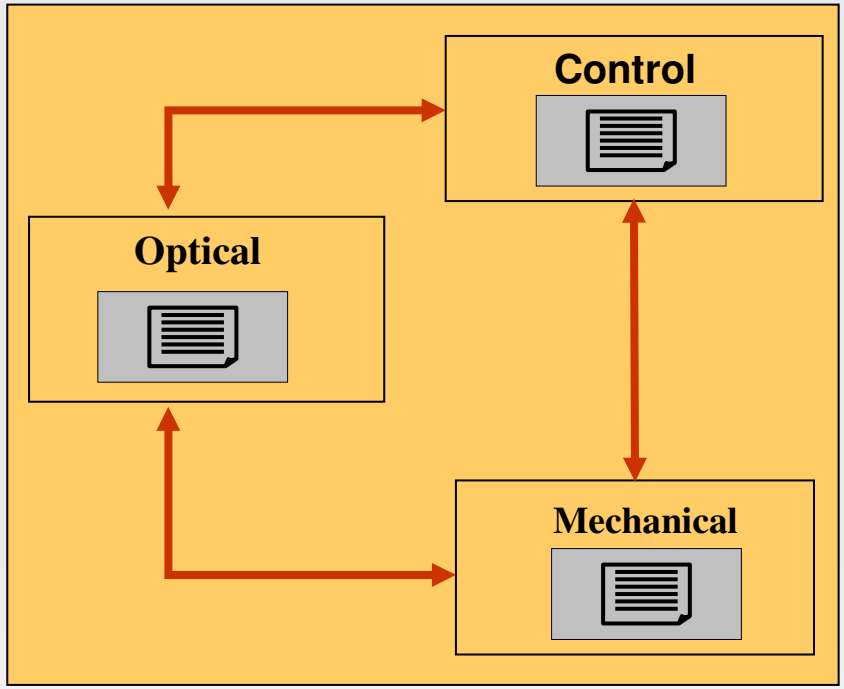


Source : Balinga, Banerjee

Outlook for the design of heterogeneous SoC

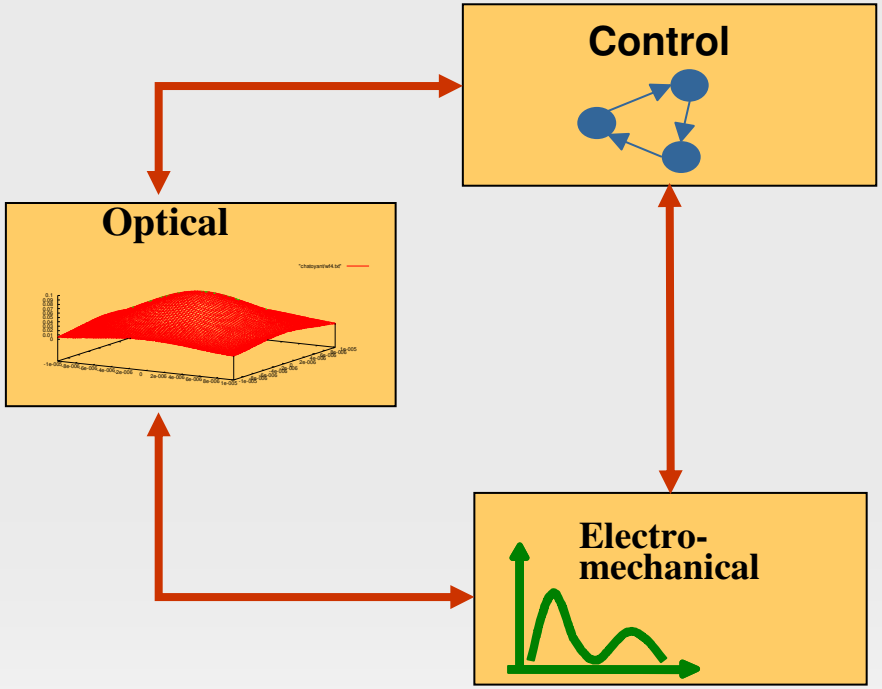
- Access to physical prototyping for multi-technology SoCs is a major challenge
  - Significant cost
  - Harder to influence standard processes
- Modeling and simulation becomes a necessary alternative in design space exploration for these systems
  - Few existing approaches
  - More research needed

Heterogeneous SoC Specification & Validation



- Extensions of existing tools/languages
  - Homogeneous environment
  - Classical HDLs + AMS concepts + new features for sim scheduler
  - VHDL-AMS, Verilog-AMS, SystemC-AMS
  - No powerful libraries

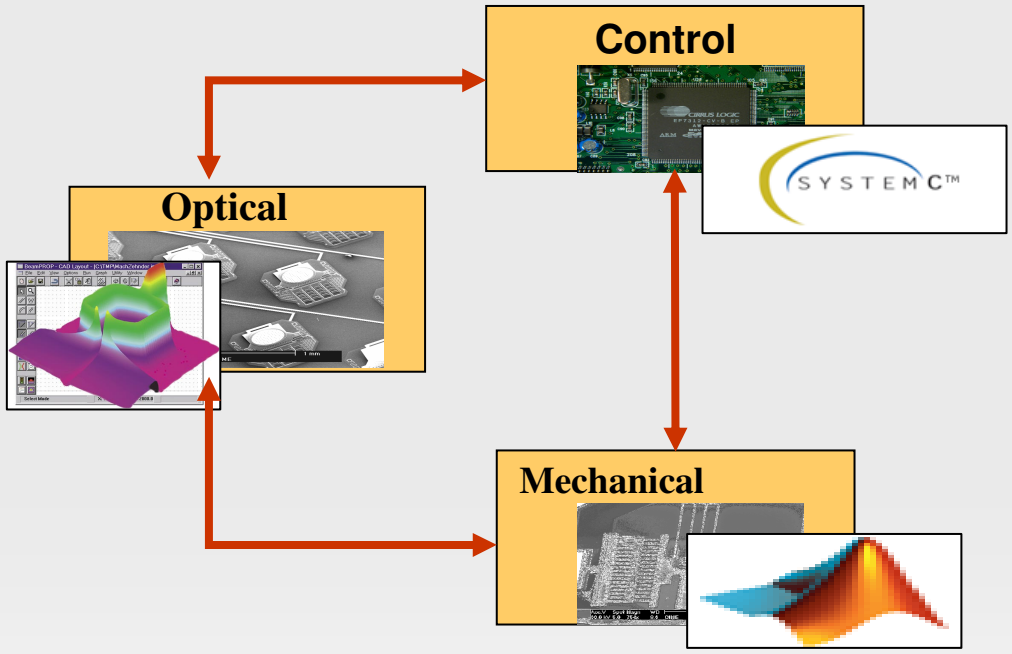
Heterogeneous SoC Specification & Validation



MoC Interfaces

- Heterogeneous Models of Computation (MoC)
  - Single formalism for representing different models
  - Deep conceptual understanding
  - Ptolemy [Lee], Rugby [Jantsch]

Heterogeneous SoC Specification & Validation

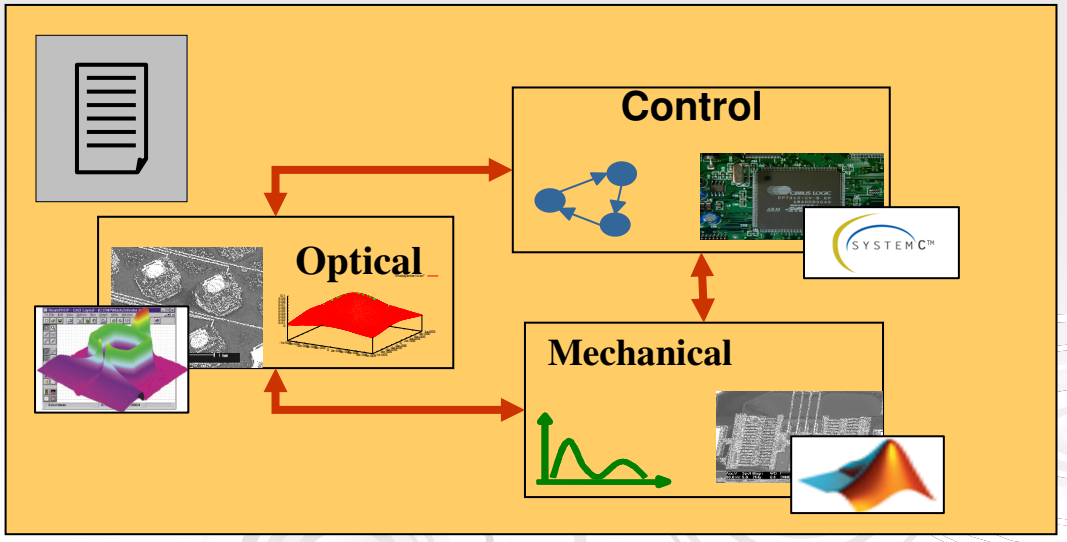


- Heterogeneous execution models
  - Multiple environments
  - Taking into account implementation aspects
  - Application specific efficient libraries
    - LEOM [O'Connors]
    - Pittsburgh [Levitan]
  - Global execution models
    - TIMA [Jerraya & Kriaa]
    - Ecole Polytech Montreal

Interfaces for Execution Models Adaptation

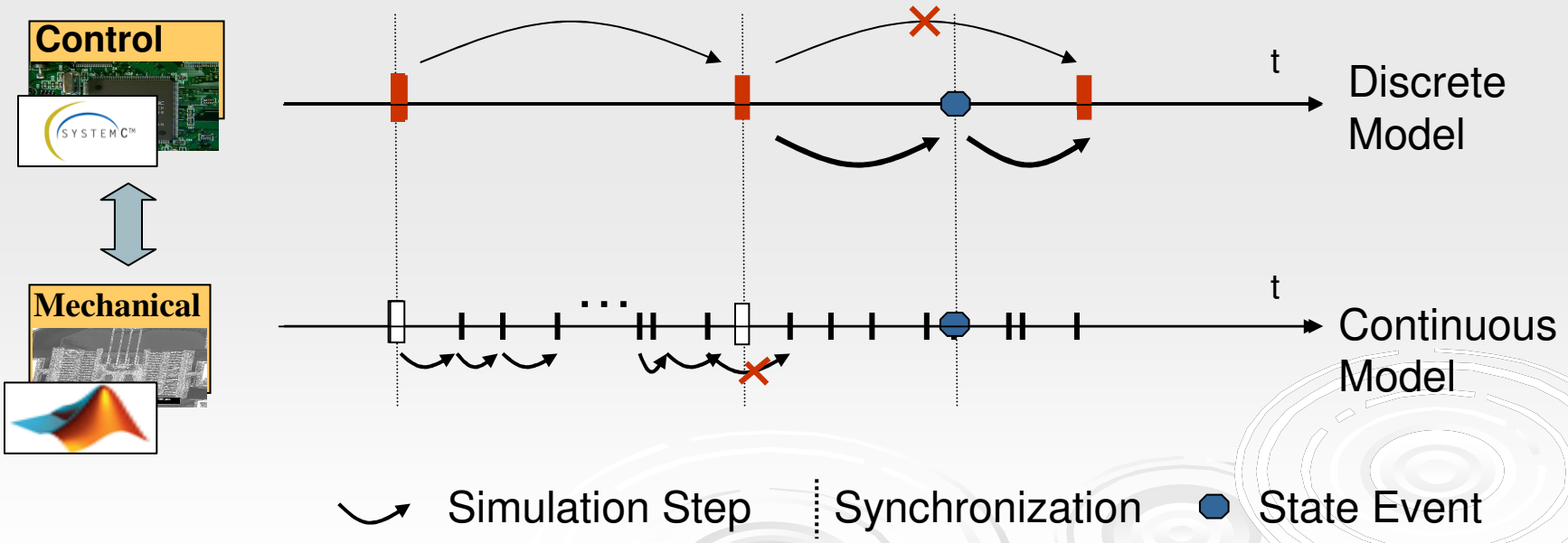
Key Features for Next Specification & Validation Tools

- Homogeneous environment facilitating cooperation between different teams
  - Enabling easy specification, automatic generation for simulation interfaces
  - Taking into account implementation choices
  - Exploiting powerful existing tools (Simulink, SystemC, …)
  - Based on a single well defined formalism for domain interaction



Heterogeneity example
- Continuous vs. Discret -

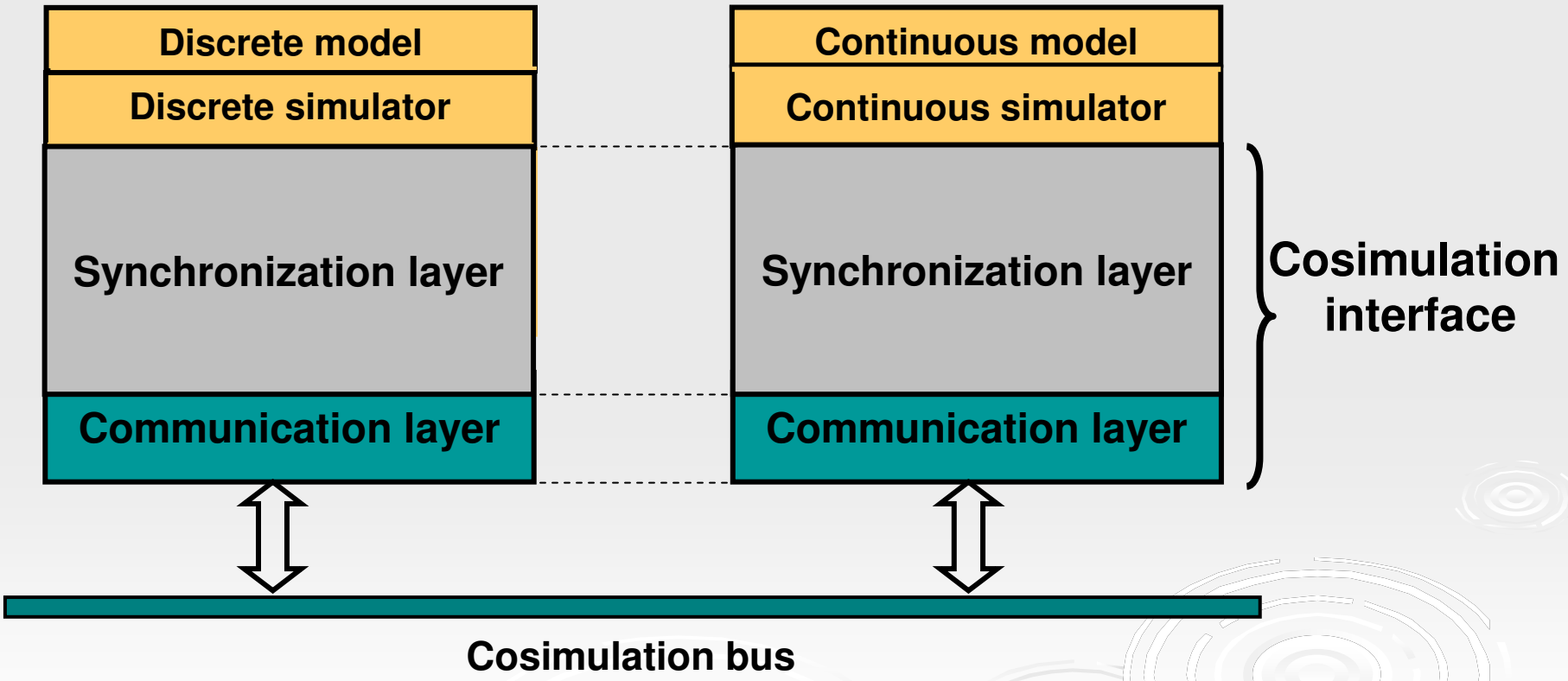
Concept / Model	Time	Communication means	Processes activation rules
Discrete	Advances discretely (constant intervals)	Set of events	Processes are sensitive to events
Continuous	It advances by integration steps (IS)	Piecewise-Continuous signals	Processes are executed at each IS



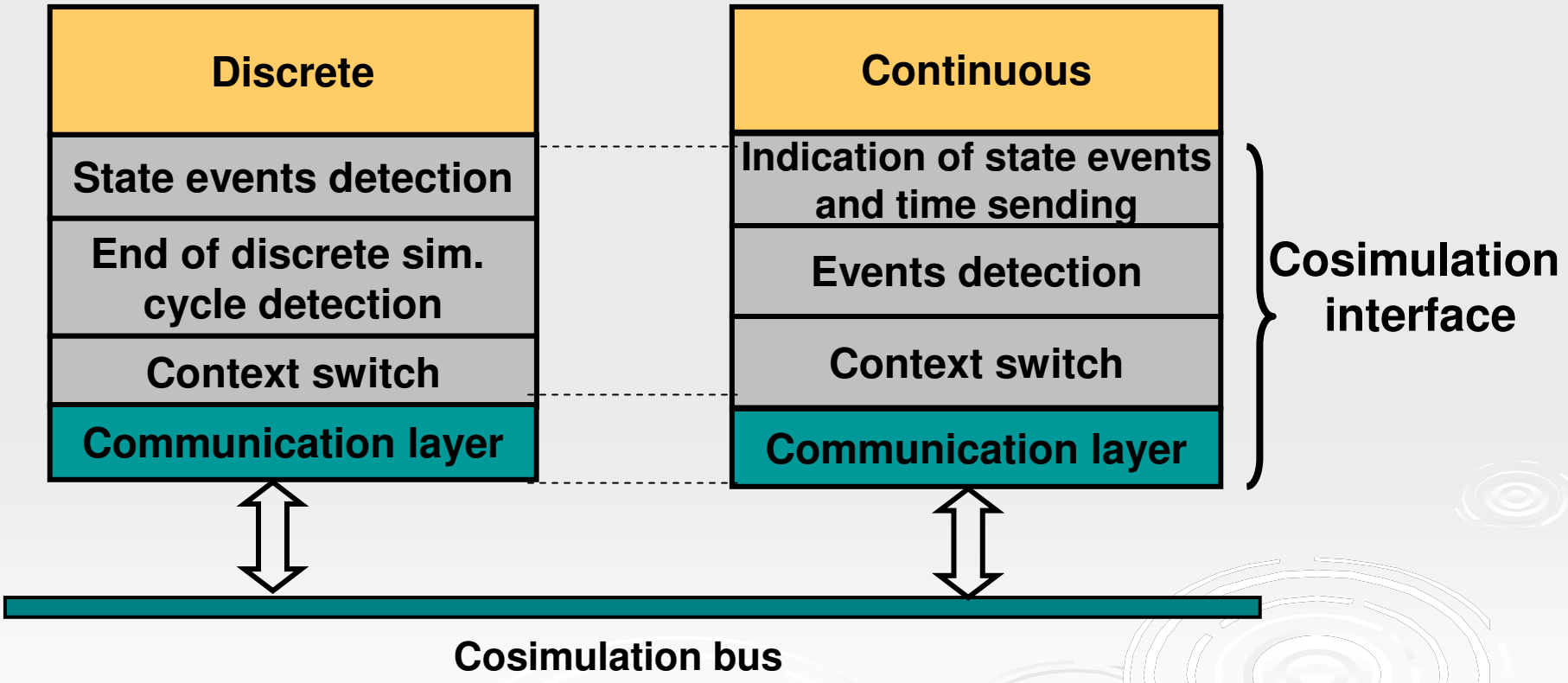
Challenges for Accurate Global Execution

- Detection of state events generated by the continuous simulator
- Detection of the next event of the discrete simulator (scheduled event)
- Detection of the end of the discrete simulation cycle and the time step sending

Generic Architecture for Continuous/Discrete Simulation



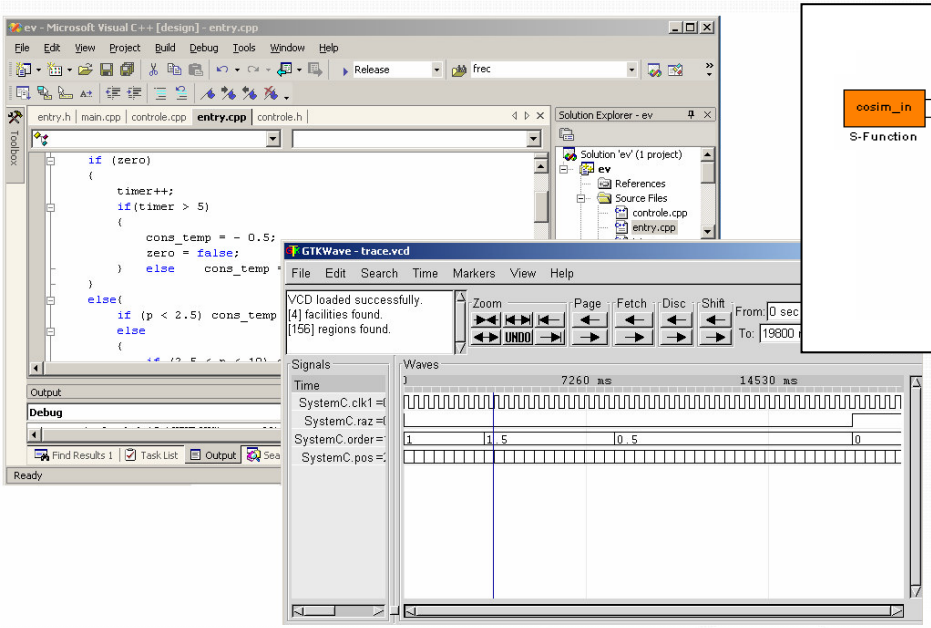
Generic Architecture for Continuous/Discrete Simulation



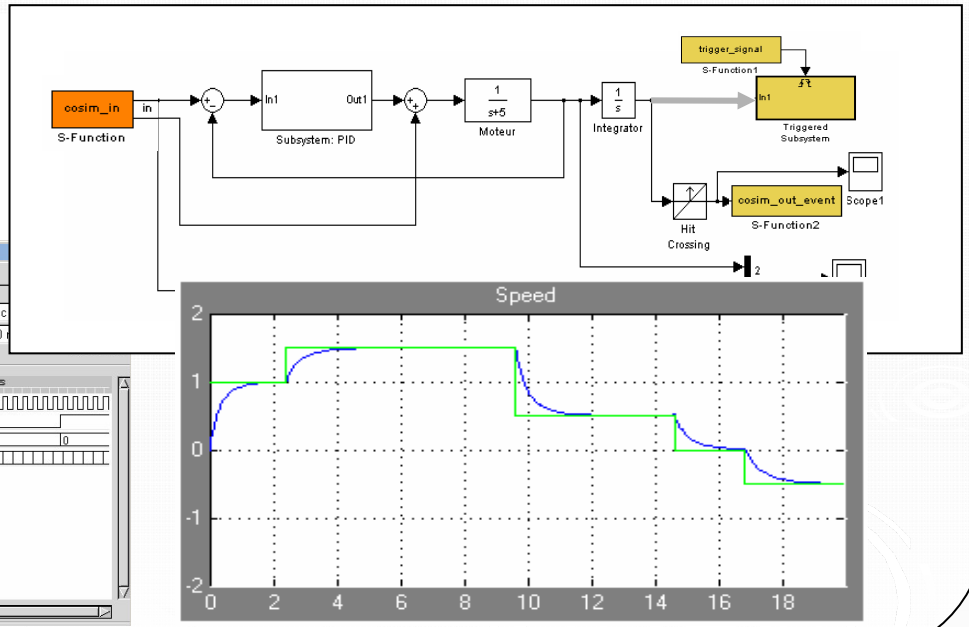
First results
- Continuous/Discrete simulation -

- SystemC/Simulink accurate simulation
  - Easy integration, generic library elements

Systemc



Simulink



Performances analysis

- Inter-Simulators Communication overhead
  - 20% of the total simulation time
- Overhead caused by the Simulink integration step adjustment
  - max. 5% of total simulation time
- SystemC Synchronization overhead
  - max. 0.2% of the total simulation time

Conclusions

- SoC drivers for multi-technology integration
- New CAD tools for design exploration are required
  - Global specification and validation are important challenges
- First prototype for electro-mechanical systems
  - Continuous/discrete integration
  - Simulink and SystemC integration