Surfing the Wave of Moore's Law ?

MPSoC'05

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Outline

- Definitions
- Yesterday
- Today
- Tomorrow

Definitions

ASIC (Application Specific Integrated Circuit):

IC dedicated to a specific application market designed for single customer based on standard cells

ASSP (Application Specific Standard Product):

IC dedicated to a specific application market designed for several customers based on standard cells

Structured ASIC:

Metal programmed gate array with embedded memories, analog blocks, and configurable IO

Yesterday

Riding Moore's Law for several decades:

- From LSI to multi million gates ICs
- From calculators to portable MM devices
- Mobile phones with compute power of yesterday's mainframes

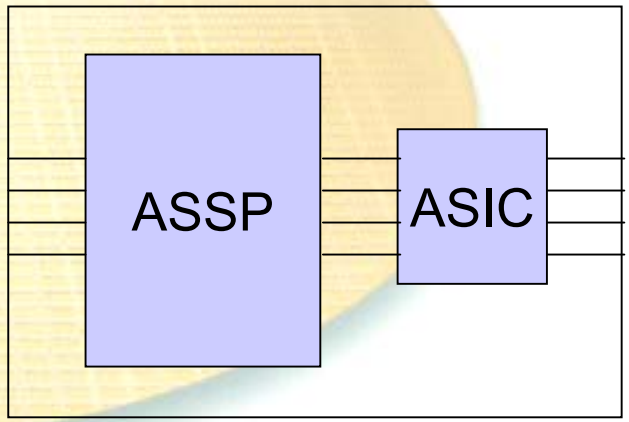
Several paradigm shifts to manage complexity

- Transistors => std cells => HDL synthesis
- IP reuse
- HW => SW

Yesterday

Two types of ICs

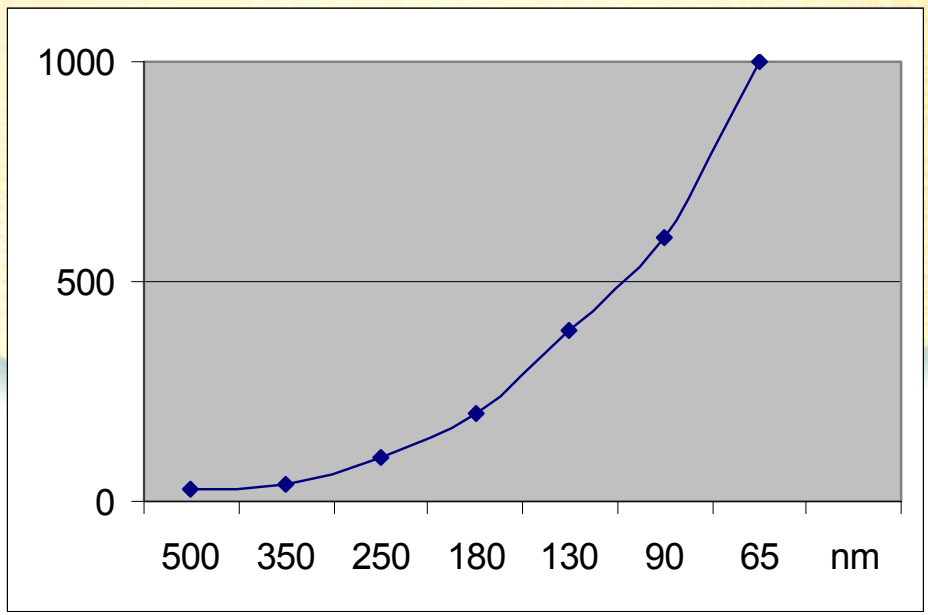
- ASSPs:
  - Developed for several customers
  - Platforms
  - Huge volumes
- ASICs:
  - Developed for single customer
  - Companion chip of ASSPs
  - Used to differentiate product from competition
  - High end => low volumes



Today

Mask costs have reached a critical point:

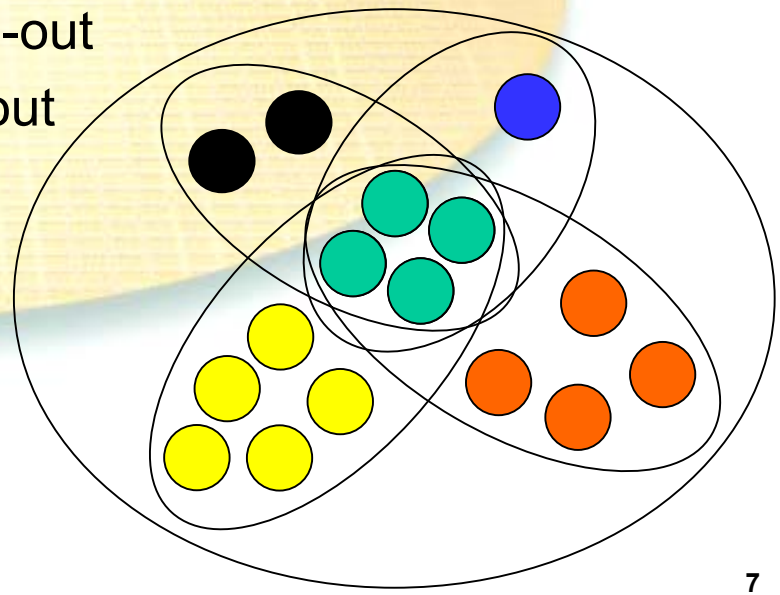
- ASICs:
  - No more ASICs < 130 nm
  - costs full mask are infeasible



Today

Mask costs have reached a critical point:

- ASSPs:
  - Mask costs dominate design process
    - Design for many use cases
      => huge complexity
    - Test silicon by means of silicon shuttles
    - Huge verification effort before tape-out
    - High level mngt approval for tape out
  - Huge financial risks:
    - Consortia of companies



Today

Alternatives to ASICs:

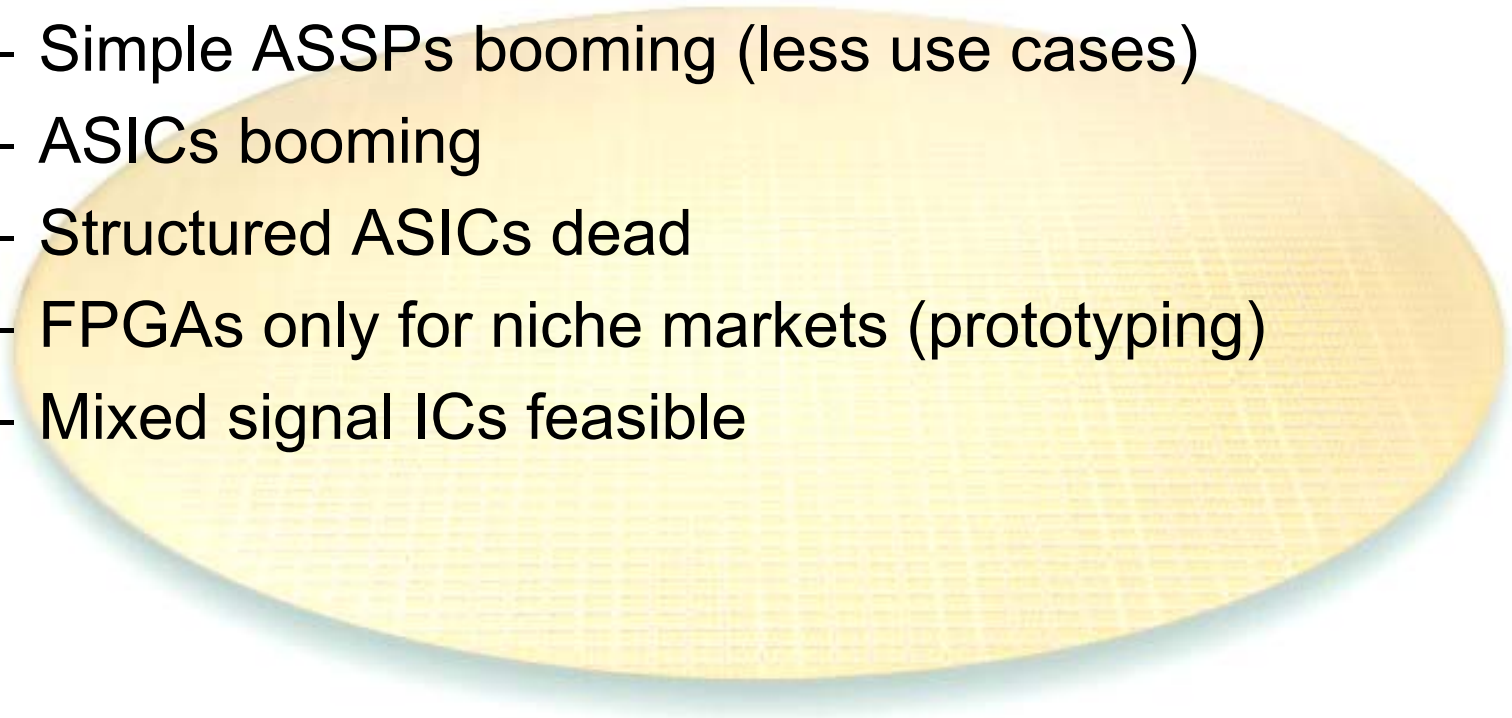
- FPGA paradise:
  - \+ Ultimate flexibility
  - \+ Easy verification (just synthesize and evaluate)
  - \- Complexity underestimated
  - \- Low performance (high speed interfaces)
  - \- Leakage power dissipation (< 65 nm technologies)
- Structured ASICs:
  - \+ Good Performance/power/area
  - \- Not really taking off
  - \- Definition of masters is issue

There are no alternatives to ASSPs!

Tomorrow

Two scenarios:

- Mask-less wafer stepper becomes reality:
  - Simple ASSPs booming (less use cases)
  - ASICs booming
  - Structured ASICs dead
  - FPGAs only for niche markets (prototyping)
  - Mixed signal ICs feasible



Tomorrow

Two scenarios:

- Mask-less wafer stepper stays dream:
  - ASICs dead
  - Structured ASICs booming
  - Future FPGAs depends on leakage power
  - Mixed signal ICs by means of SIPs
  - ASSPs will follow same path as foundries
    => couple of ASSPs developed by consortia

Thank you!