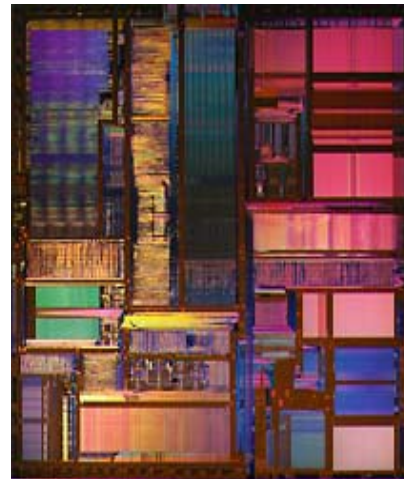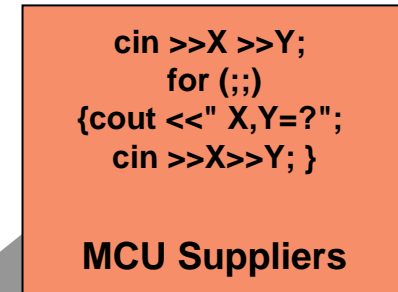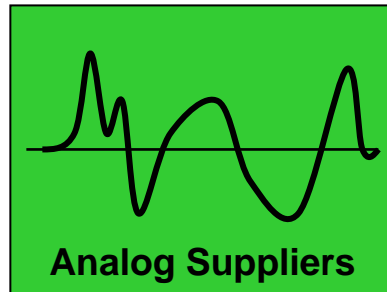# Introducing Mixed Signal into FPGA based MPSoC

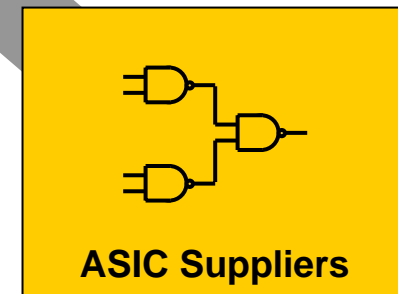**Yankin Tanurhan**

**Sr. Director Application and IP Solutions
Actel Corporation**

Actel

The Race to the Programmable System Chip

Analog Suppliers

```
cin >>X >>Y;
    for (;;)
{cout <<" X,Y=?";
  cin >>X>>Y; }
```

MCU Suppliers

LUT

FPGA Suppliers

Programmable System Chip

ASIC Suppliers

ONECHIP
is all you need

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Typical System

System Memory DRAM	Cache Memory	NV Storage
	SRAM	FLASH

MPU / MCU

FPGA / ASIC

Analog Interface

Power Mgmt

Clock Mgmt

Discrete Analog

ONECHIP
is all you need
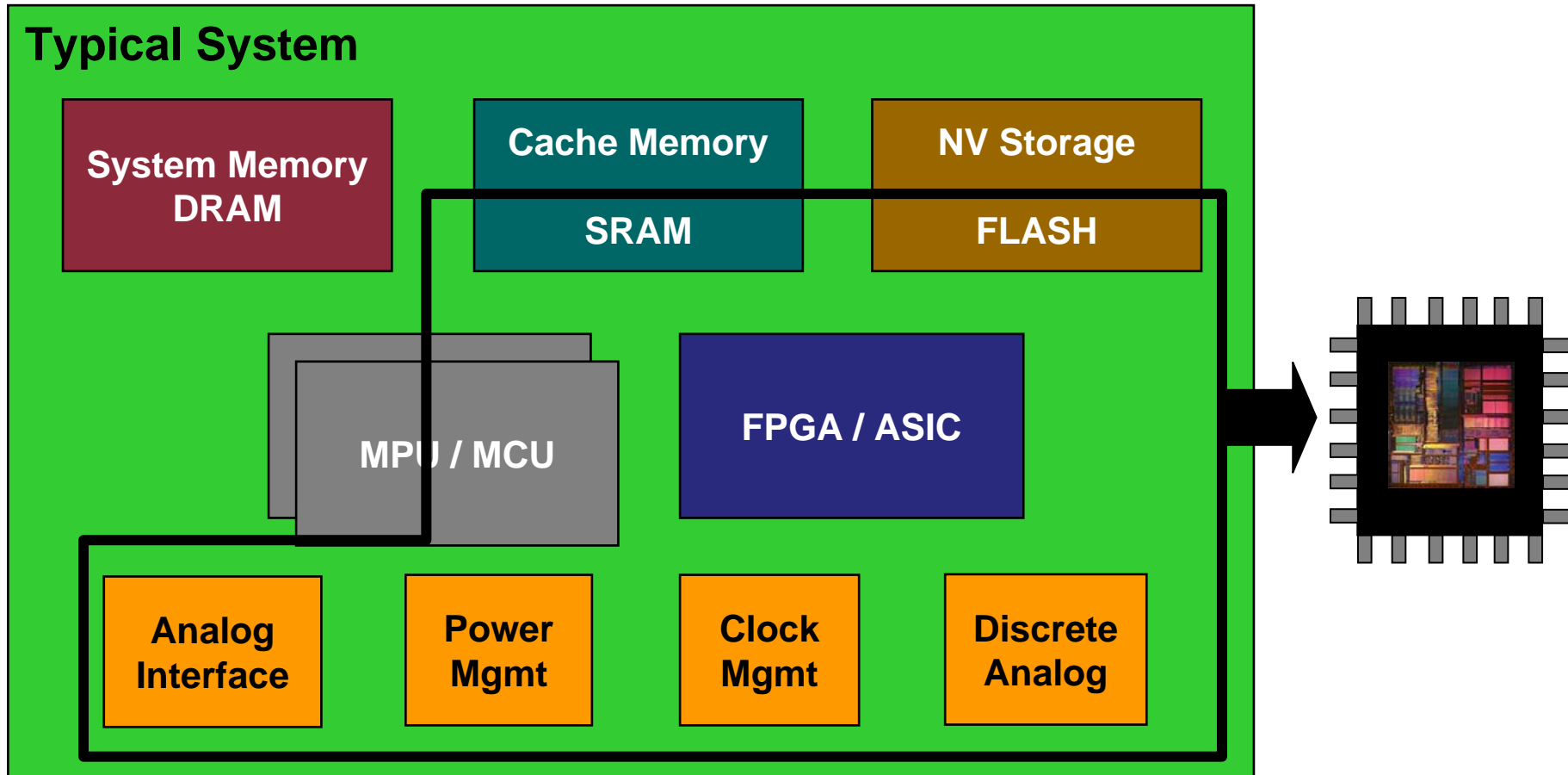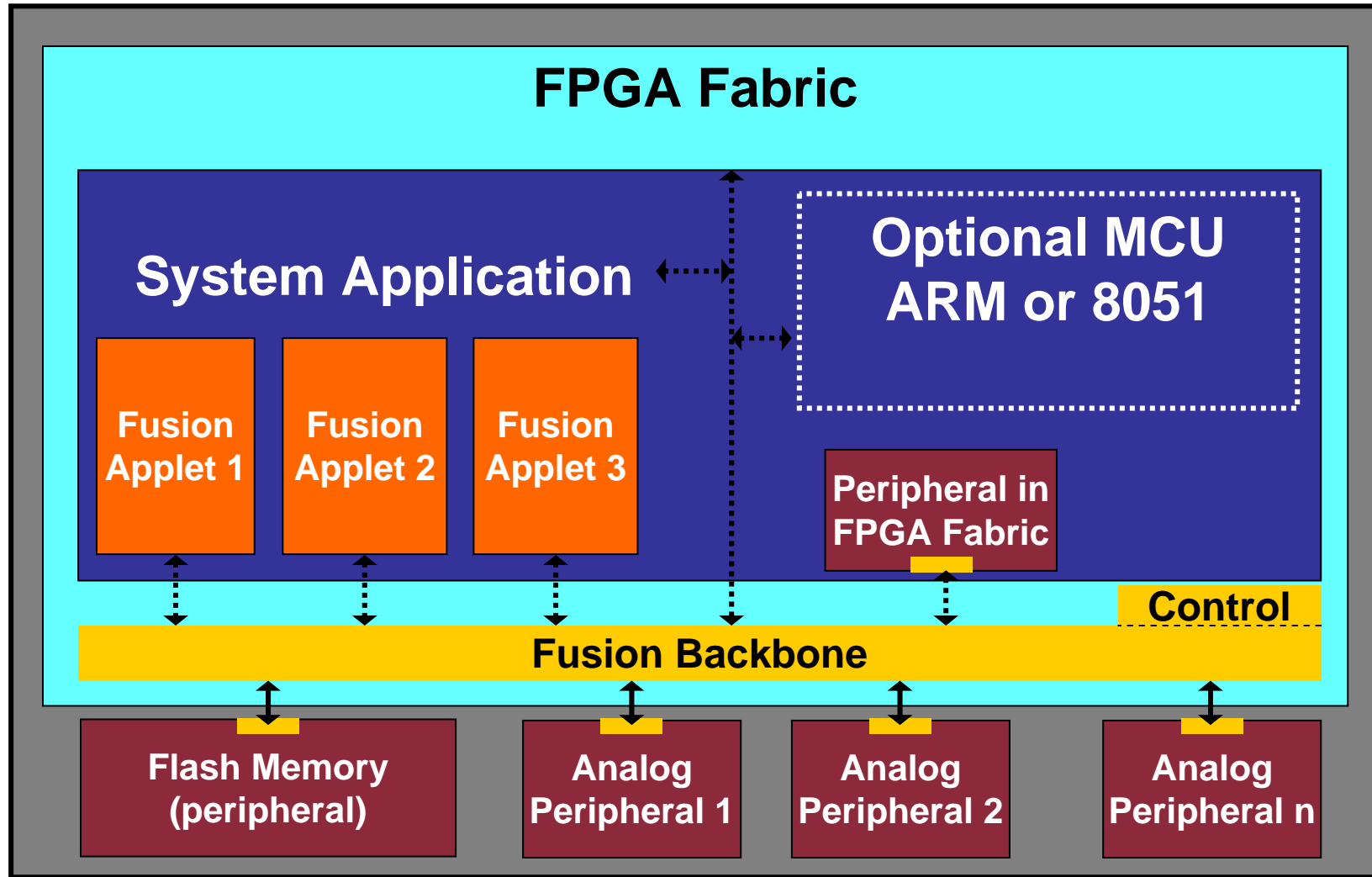
Level 0 – Fusion Peripherals

- **Configurable, hard-wired, analog & flash blocks**

- **Optional peripherals in soft (FPGA) gates**

- **Standardized interface embedded in all peripherals**

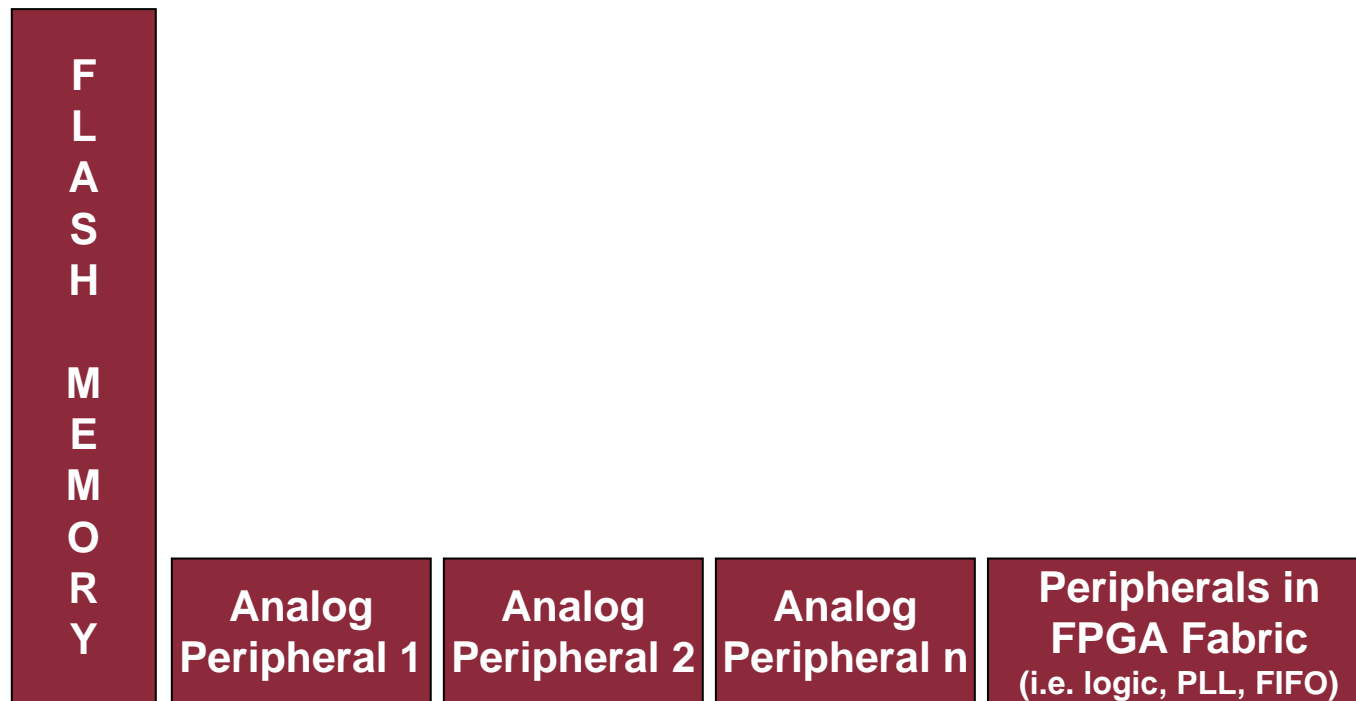| FLASH MEMORY				
	Analog Peripheral 1	Analog Peripheral 2	Analog Peripheral n	**Peripherals in FPGA Fabric** (i.e. logic, PLL, FIFO)

Level 1 – Fusion Backbone

- **Fusion Backbone is Flexible Bus and Control Logic**

- **Built-in control (soft IP) configures peripherals based on information stored in flash memory**

- **Bus controls communication between peripherals**

FLASH MEMORY	Fusion Backbone			
	Analog Peripheral 1	Analog Peripheral 2	Analog Peripheral n	Peripherals in FPGA Fabric (i.e. logic, PLL, FIFO)
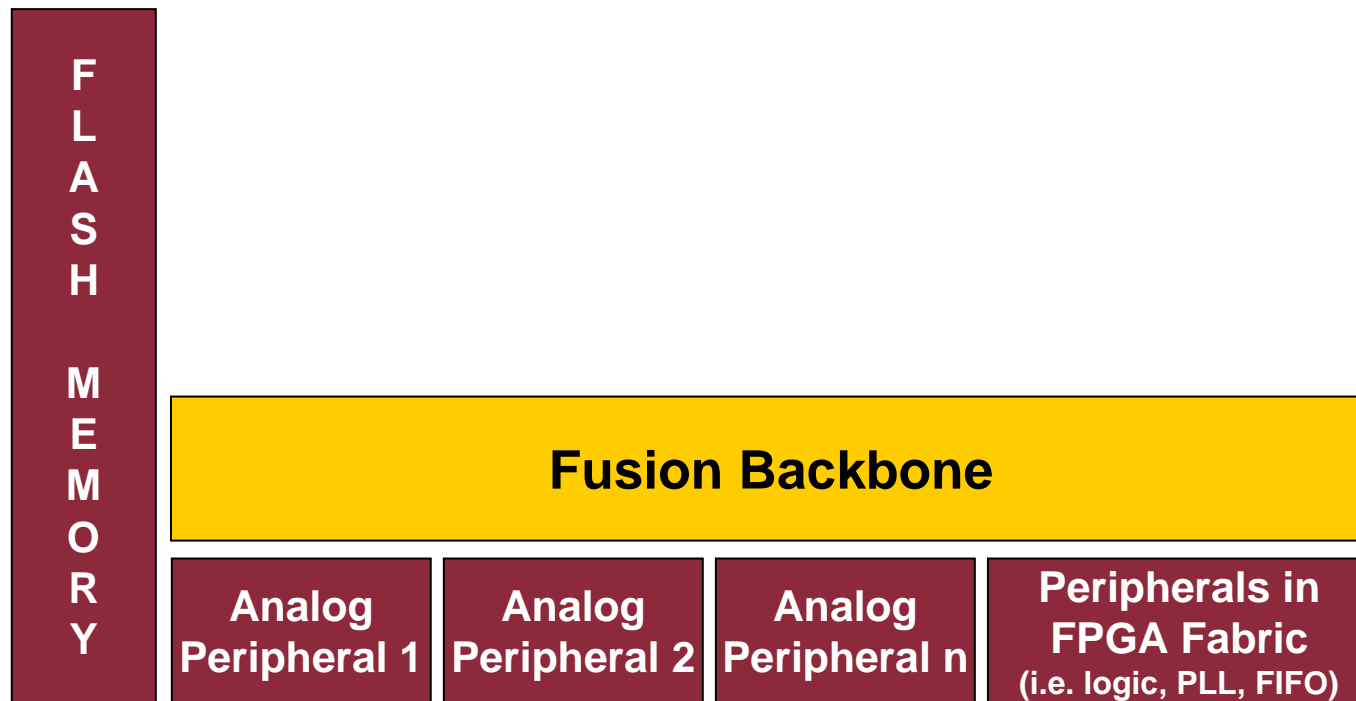
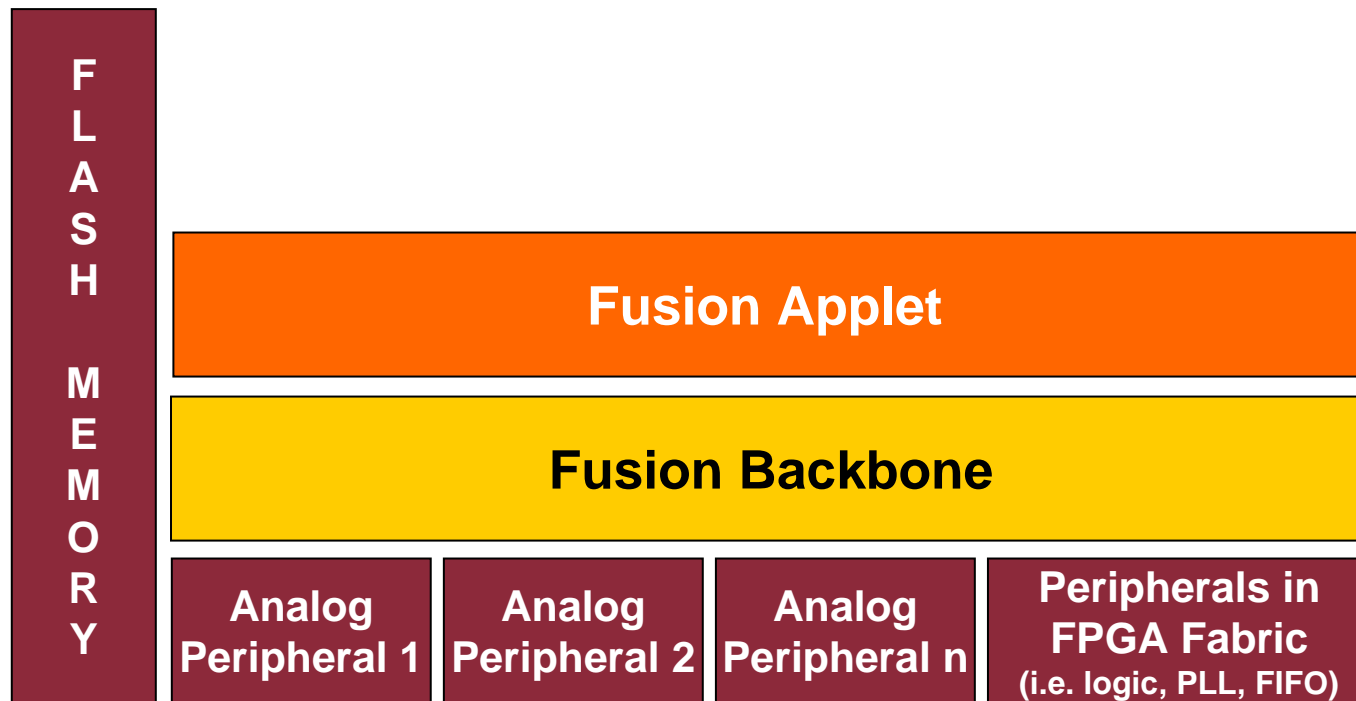# Level 2 – Fusion Applet

- **Application building blocks implementing specific functions**

- **Sourced by Actel, a customer, or a partner**

- **Soft IP implementation**

FLASH MEMORY	Fusion Applet
	Fusion Backbone
	Analog Peripheral 1	Analog Peripheral 2	Analog Peripheral n	Peripherals in FPGA Fabric (i.e. logic, PLL, FIFO)

Level 3 – System Applications

- **Larger user-application that combines applets**

- **Optional MCU enables a combination of software and HDL-based design methods**

Fusion Architecture Stack Benefits
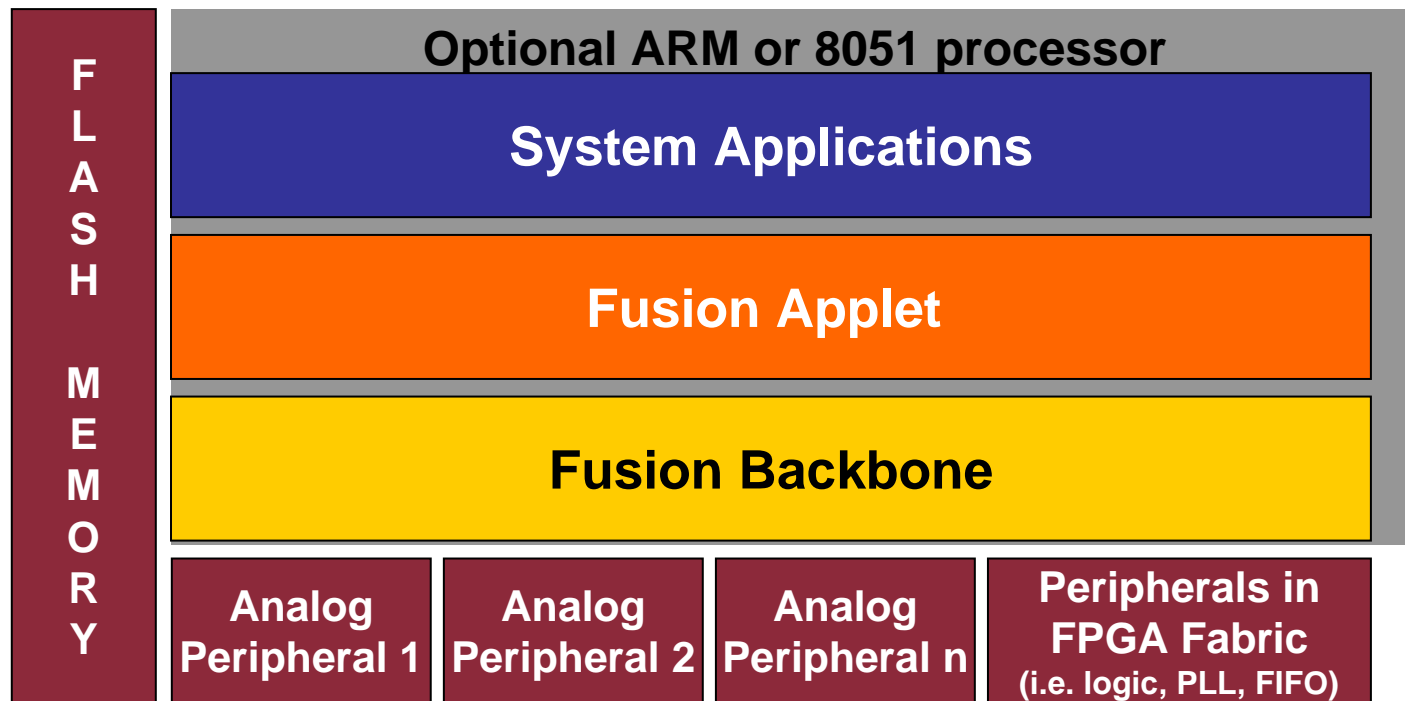
■ **Flexible design environment**

- **Layered model enables design at high or low levels of abstraction**

■ **Advantages**

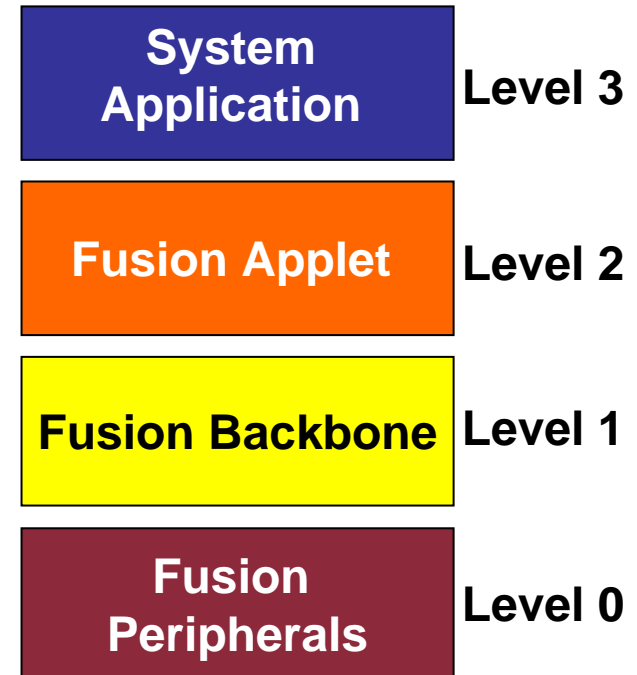- **Peripherals can be hard-wired resources or soft IP**

- **Backbone is scalable to any number of Peripherals or Applets**

- **Applets can be rapidly combined to create large applications**

- **Well defined interface for external IP and tool integration**

System Application	Level 3
Fusion Applet	Level 2
Fusion Backbone	Level 1
Fusion Peripherals	Level 0

ONECHIP
is all you need
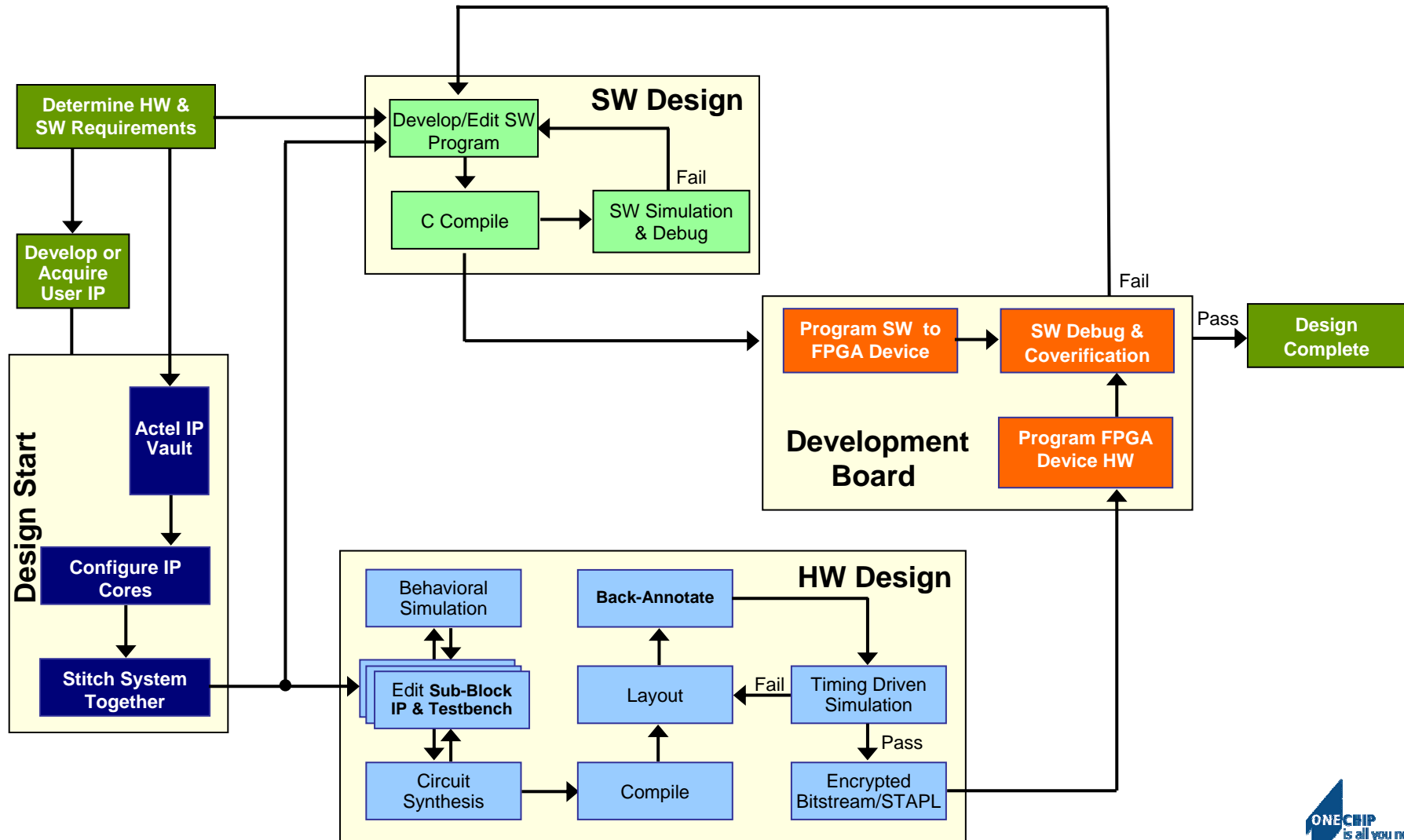
Integration increases complexity

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- **Tools needs increase with added integration**

  - **High-level design productivity**

  - **Hardware / software co-verification**

  - **Bus-based communication**

  - **Device / system modeling**

  - **Hardware and Software Debugging capability**

- **Innovative Fusion Tools resolve Complexity…**

Development Flow

Design Start

- Determine HW & SW Requirements
- Develop or Acquire User IP
- Actel IP Vault
- Configure IP Cores
- Stitch System Together

SW Design
- Develop/Edit SW Program
- C Compile
- SW Simulation & Debug — Fail

Development Board
- Program SW to FPGA Device
- SW Debug & Coverification — Pass → Design Complete
- Program FPGA Device HW
- Fail

HW Design
- Behavioral Simulation
- Back-Annotate
- Edit Sub-Block IP & Testbench
- Layout — Fail
- Timing Driven Simulation
- Circuit Synthesis
- Compile
- Encrypted Bitstream/STAPL — Pass

- **We are in a unique position to integrate multi-mode silicon – analog, flash, logic/FPGA, MCU**

- **Fusion stack provides a flexible and structured means of utilizing these features**

- **Fusion tools provide an easy-to-use graphical interface to simplify development**

- **Fusion opens exciting new capabilities to deliver MPSoC's**