Microelectronic System Design Research Group
University Kaiserslautern
www.eit.uni-kl.de/wehn

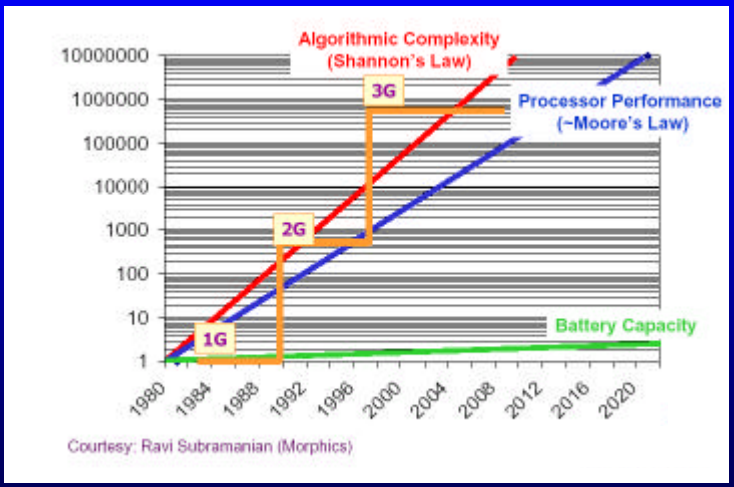
Breaking the Interleaving Bottleneck in Communication Applications for Efficient SoC Implementations

Norbert Wehn
wehn@eit.uni-kl.de

MPSoC'05, 11-15 July 2005
Relais de Margaux Hotel, France

Wireless Implementation Challenges

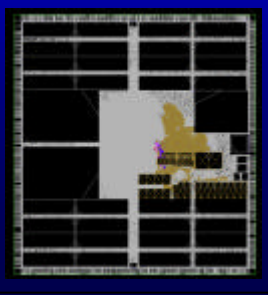
- DECT 10 MIPS, GSM 100 MIPS, UMTS x 1000 MIPS

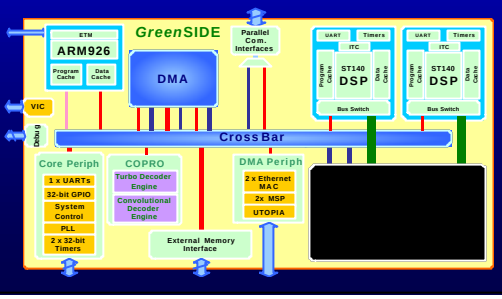


Can we close this gap ?

Example: Channel Coding

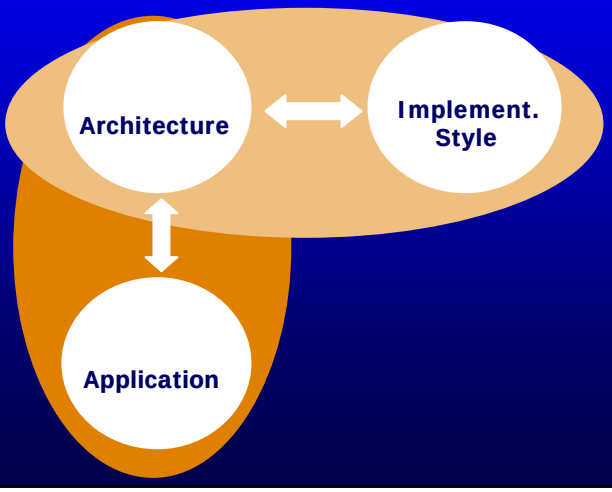
- Turbo-Codes (1993)
  - Revolution in channel coding e.g. UMTS, DVB, WLAN, CCSD
- LDPC Codes (1996)
  - Renaissance of Gallagers Work (1960)
  - Competitor to turbo-codes e.g. used in DVB-S2, WiMAX
- STM Greenside Chip: 2.5G/3G Wireless Infrastructure Chip (130nm technology)
  - Supports WCDMA, CDMA2000, EDGE
  - Decodes up to 256 voice channels & up to 8 384Kbps data channels simultaneously



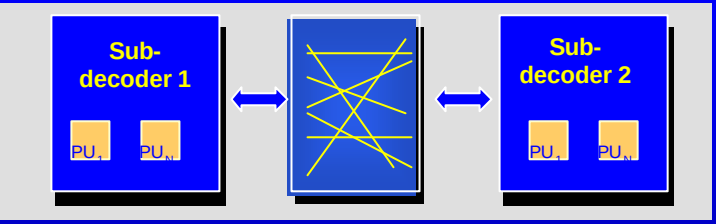


Design Space

- MPSoC'04: Trade-offs different implementation styles
  - ASIC, FPGA, ASIP, DSP, Multiprocessor...
  - Architectural efficiency & design time



Generic Decoding Structure



1. Subdecoder 1 processes one complete block
2. After finishing the calculation, data are sent to subdecoder 2
3. Subdecoder 2 starts block processing...
4. Iterate until stopping crtierion fullfilled

- Information exchange takes place „randomly“
  - Tanner graph (Parity check matrix) / Interleaver
  - Quality of „randomness“ influences communcations performance
- High Throughput/Low Latency achitectures
  - Interconnect centric architectures

Solving Interconnect Bottleneck

Crossbar functionality with output blocking conflict (MPSoC'04)

Conflict free by code design

- Solves the interconnect problem at the „system level“
- Tanner Graph/Interleaver is designed according to a fixed architectural template with regular interconnect topology e.g. barrelshifter
- Architecture imposes constraints on the code
  - Impact on communications performance

Run-time conflict resolution (MPSoC'04)

- Largest flexibilty, no impact on communications performance
- NoC approach

Algorithm Design Space

- Turbo-Decoder UMTS compliant, 166MHz, 180nm technology, Throughput 100 Mbit
  - NoC approach, large flexibilty

    14 parallel units, area = 16.84 mm^2 (14mm^2 PUs, 2.8mm^2 NoC)
  - Conflict free interleaver design, limited flexibility

    10 parallel units, area=11.23 mm^2 (10,3mm^2 PUs, 0.9mm^2 Barrelshifter)
- Implementing LDPC Decoding on Network-On-Chip, T. Theocharides, G. Link, N. Vijaykrishnan, M. J. Irwin, Int. Conference on VLSI Design 2005
  - 1024 Bit block size, 1.2Gb/s (?), R=0.75
  - NoC: 5x5 2D mesh, dimension-order routing, large flexibility
  - 160nm CMOS Technology, 1.8V, synthesis, 500 MHz, 110 mm^2, ~30 Watt
- A. Blanksby, C. Howland, IEEE Journal on Solid-States Circuits
  - 1024 Bit block size, 1 Gb/s, Rate=0.5
  - full hardwired interconnect network, no flexibility at all
  - 160nm CMOS Technology, 1.5 V, synthesis, 64 MHz, 52.5mm^2, ~700mW

DVB-S2 LDPC implementation

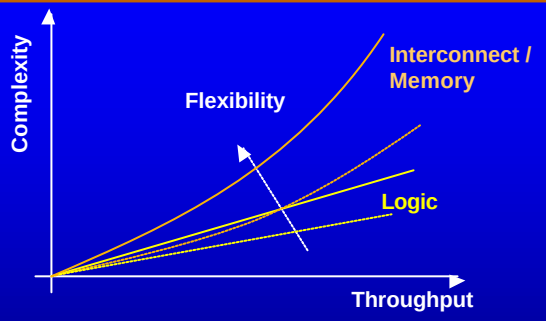
- Blocksize 64800 Bit, R=1/4..9/10, 0.7 dB to Shannon limit
- Synthesis results for the DVB-S2 LDPC code decoder

Area [mm^2] (0.13um, 270MHz)		Area [mm^2]
RAMs	Channel LLR	1.997
	Messages	9.117
	Addresses/Shuffling	0.075
Logic	Functional Nodes	10.8
	Control logic	0.2
Shuffling Network		0.55
Total Area [mm^2]		22.74
Throughput[Mbit/s] @30iter		255

Why is this implementation so efficient ?

- Code was defined with implementation complexity in mind
- IRA codes: subset of LDPC codes
- Limited flexibility (11 Tannergraphs)
- Permutation network
  - Shuffling network with some “tricky” memory allocation/assignments

Algorithmic Flexibility



LDPC Decoder: synthesizable IP block, 130nm, 10000 bits

- Full flexibility i.e. supports every LDPC code: 27 mm^2
- Limited flexibility (e.g. WiMax-WLAN): 5 mm^2

This graph is independent of implementation style

Analyze carefully the flexibility requirements

Application/architecture Codesign

Conclusion

The Gap can be closed

- Application/Architecture Codesign
- Match the architecture & application
- „Just enough flexibility“
  - Application
  - Implementation

Thank you for listening!

For further information please visit

http://www.eit.uni-kl.de/wehn