MPSoC '06

AGENDA

SUNDAY AUGUST 13: WELCOME

18.00 **Registration**

19.00 **Welcome reception**

MONDAY AUGUST 14: SOFTWARE DAY

8.30 **Registration continued**

SESSION 1: KEYNOTE

8.30 **Software and the Concurrency Revolution**
Herb Sutter, Microsoft, USA

9.30 **Break**

SESSION 2: MINI-KEYNOTES

10.00 **Semantics in Model-Based Design**
Janos Sztipanovits Vanderbilt University, USA

10.12 **Modular Communication-Centric MPSoC Architectures**
Pieter van der Wolf, Philips Research, The Netherlands

10.24 *Philippe Kajfasz, Thales, France*

10.36 *Rolf Ernst, TU Braunschweig, Germany*

10.48 **Programming models and Software Architecture for MPSoC**
Ahmed Jerraya, TIMA Laboratory, France

11.00 **Metaphors for Concurrent Computation**
Steven P. Levitan, University of Pittsburgh, USA

11.12 **Discussion with the lecturers of the session**

12.00 **Lunch**

SESSION 3: IN-DEPTH PRESENTATIONS

13.30 **System-level exploration tools for MPSoC designs**
Peter Flake, Imperas Inc., USA

14.00 **Bandwidth, Bandwidth, Bandwidth**
Paul Franzon, NCSU, USA

14.30 **Maximizing parallelism in NP**
Ran Giladi, EZchip technologies Ltd. & Ben-Gurion University, Israel

15.00 **Break**

15.30 **SODA: A Low-power Architecture For Software Radio**
Scott Mahlke, University of Michigan, USA

16.00 **Reconfigurable Multiprocessor System-on-Chip for Embedded Applications**
Thierry Collette, CEA LIST, France

16.30 **Networks-0n-Chip (NoC) for 3D Architectures**
Vijaykrishnan Narayanan, Pennsylvania State U., USA

17.00 **Discussion with the lecturers of the session**

17.30 **Participants' presentation**

18.30 **Diner sponsored by** 

TUESDAY AUGUST 15: HARDWARE DAY

SESSION 4: KEYNOTE

8.30 **The Reinvention of the Microprocessor for MPSOC**
Chris Rowen, Tensilica, USA

9.30 **Break**

SESSION 5: MINI-KEYNOTES

10.00 **Bus Architecture Optimization Method Based on System-Level Profiling**
Masaharu Imai, Osaka University, Suita, Japan

10.12 **Automatic Instruction-Set Specialisation**
Paolo Ienne, EPFL, Switzerland

10.24 **Securing Next-generation Mobile Platforms: The User-to-Device Authentication Issue**
Srivaths Ravi, NEC Laboratories America, USA

10.36 **Joining Efforts from Hardware and Software Communities for Embedded Systems Design**
Pierre G. Paulin, STMicroelectronics, Canada

10.48 **Optical NoC Evaluation in a System-Level MP-SoC Platform**
Gabriela Nicolescu , Ecole Polytechnique de Montréal, Canada

11.00 **ASIPs as a Cornerstone of Heterogeneous MPSoCs: What, Why, and How?**
Gert Goossens, Target Compiler Technologies, Belgium

11.12 **Discussion with the lecturers of the session**

12.00 **Lunch**

SESSION 6: IN-DEPTH PRESENTATIONS

13.30 **DaVinci™ technology for digital video applications**
Deepu Talla, Texas Instruments, USA

14.00 **Concurrent Exploration of Memory and Communication Architecture for MPSoCs**
Nikil Dutt,UC Irvine, USA

14.30 **Dependability of VLSI Systems**
Hiroto Yasuura, Kyushu University, Japan

15.00 **Break**

15.30 **Empirical Architecture: Balancing Computation and Communication**
Graham Hellestrand, VaST Systems Technology Corporation, USA

16.00 **The Future of Mobile Computing**
Ulrich Ramacher, Infineon Technologies AG, Germany

16.30 **Multiprocessors in Wireless Multimedia Terminals**
Mika Kuulusa, Nokia, Finland

17.00 **Discussion with the lecturers of the session**

17.30 **Speakers meeting**

18.30 **Diner sponsored by** ARM

WEDNESDAY AUGUST 16: VIDEO/COMMUNICATION

SESSION 7: KEYNOTE

8.30 **Programming modern FPGA platforms**
Ivo Bolsens, Xilinx, USA

9.30 **Break**

SESSION 8: MINI-KEYNOTES

10.00 Hardware/Software Co-Design of an FPGA-based Embedded Tracking System
Wayne Wolf, Princeton University, USA

10.12 An H.264/AVC Main Profile Video Codec Accelerator in a Multimedia SOC Platform
Youn-Long Lin, National Tsing Hua University, Taiwan

10.24 A Configurable Processor for Outer Modem Applications
Norbert Wehn, University of Kaiserslautern, Germany

10.36 Scalable processing through software threading
John Goodacre, ARM, UK

10.48 Next-Generation Microprocessor Performance Challenges
Olivier Franza, IntelMassachusetts, Inc., USA

11.00 Evolving MPSoC solutions
Jan Madsen, Technical University of Denmark, Denmark

11.24 Discussion with the lecturers of the session

12.00 Lunch

SESSION 9: IN-DEPTH PRESENTATIONS

13.30 The Sandbridge SB3011 Multiprocessor System on a Chip for Software Defined Radio Handsets
John Glossner, Sandbridge Technologies Inc., USA

14.00 Challenges of MPSOC Communication, Computation and Design Flow
Jari Nurmi, Tampere University of Technology, Finland

14.30 Standardized APIs Facilitate Software and Hardware Development of Embedded Multicore Designs
Markus Levy, Embedded Microprocessor Benchmark Consortium & The Multicore Association, USA

15.00 Break

15.30 Benchmarking System Applications on Virtex5 FPGA platforms
Kees Vissers, Xilinx Research, USA

16.00 Design challenges for wireless smart cameras
Marc Heijligers, Philips Research, The Netherlands

16.30 A 90nm Low-Power GSM/EDGE Multimedia-Enhanced Baseband Processor with 380MHz ARM9 and Mixed-Signal Extensions
Steffen Buch, Infineon Technologies AG, Germany

17.00 Discussion with the lecturers of the session

18.00 Social Event sponsored by

THURSDAY AUGUST 17: INTERCONNECT/NETWORKING

SESSION 10: IN-DEPTH PRESENTATIONS

8.30 Profiling based architecture optimization for heterogeneous MPSoC
Rainer Leupers, RWTH Aachen University, Germany

9.00 The Use Of Virtual Platforms In MP-SoC Design
Eshel Haritan, CoWare Inc., USA

9.30 Break

SESSION 11: MINI-KEYNOTES

10.00 Quality of Service for an Uncertain World
Kees Goossens, Philips Research, The Netherlands

10.12 Algorithms and Architecture for Next Generation GPUs
Donald S. Fussell, The University of Texas at Austin, USA

10.24 Developing a fully Scalable MPEG-4 AVC/ H.264 Video Codec using a proven MPSoC architecture and heterogeneous design methodology
Ian Walsh, CEO, MnD Semiconductors, France

10.36 NoC is the answer! (What was the question?)
Drew Wingard, Sonics Inc. USA

10.48 *Hannu Tenhunen, Royal Institute of Technology (KTH), Sweden*

11.00 QoS: is or is not the main differentation point for NoC?
Marcello Coppola, STMicroelectronics, France

11.12 Discussion with the lecturers of the session

12.00 Lunch

SESSION 12: IN-DEPTH PRESENTATIONS

13.30 Statistical Design Issues and Tradeoffs in On-Chip Interconnects
Wayne Burleson, University of Massachusetts, USA

14.00 Will the NoC swallow the SoC?
Ran Ginosar, Israel Institute of Technology, Israel

14.30 QoS Profiling Using NoC Adaptive Design Information System
Alain Fanet, Arteris, France

15.00 Break

15.30 FAUST: A NoC-based Platform for Telecom
Jean-René Lèquepeys, LETI/CEA, France

16.00 Multi-core platforms are a reality... but where is the software support?
Rudy Lauwereins, IMEC, Belgium

16.30 The Diopsis Multi-Processor Tile of SHAPES
Pier Stanislao Paolucci, ATMEL & INFN, Italy

17.00 Discussion with the lecturers of the session

18.30 Diner

FRIDAY AUGUST 18: UNDERSTANDING THE VALUE CHAIN FOR MPSOC

SESSION 13: KEYNOTE

8.30 A New Business Model to Face the Challenges in the Ubiquitous Era
Masao Nakaya, Renesas, Japan

9.30 Break

SESSION 14: MINI-KEYNOTES

10.00 Processors in FPGAs - Quo Vadis ?
FPGA representative: Yankin Tanurhan, Actel Corp., USA

10.20 From Tape-out to the Fab
EDA representative: Raul Camposano, Synopsys, USA

10.40 The Critical Role of Algorithmic Engines in Consumer SoCs
Analyst: Jacques Benkoski, US Venture Partners, USA

11.00 Discussion with the lecturers of the session

12.00 Lunch