Understanding the Value Chain for MPSoC

The Critical Role of Algorithmic Engines in Consumer SoCs

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MPSoC Presentation

August 2006

Consumer SoCs Differentiation

Recent Example:
Nokia releases three phones on April 25th, 2006

- N93 The ultimate spontaneous video recorder
- N73 The camera replacement with music
- N72 A moderate camera with FM radio

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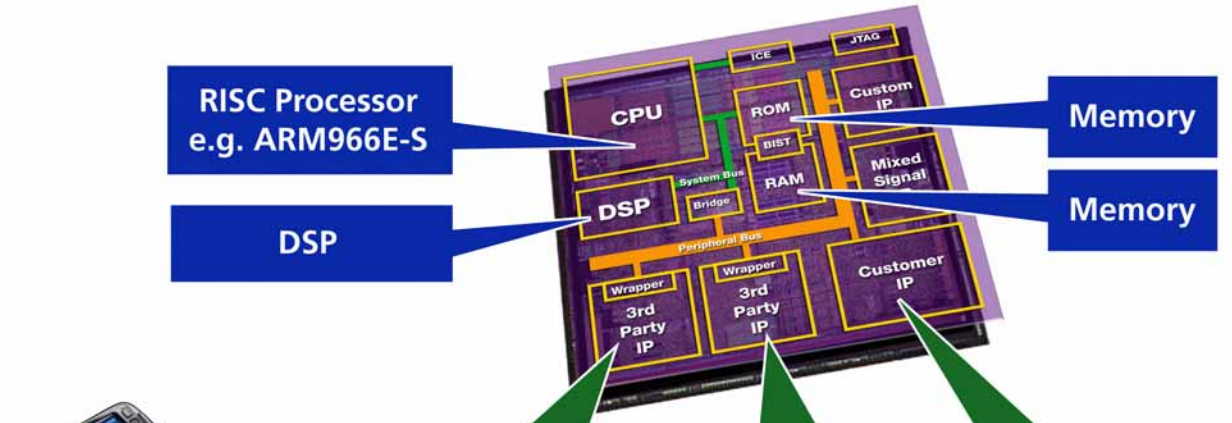
Algorithmic Engines are the Main Differentiators



N93	Wireless baseband Accelerators	3.2MP Camera	90 minute Camcorder

N73	Wireless baseband Accelerators	3.2MP Camera	Music player

N72	Wireless baseband Accelerators	2MP Camera	FM Radio

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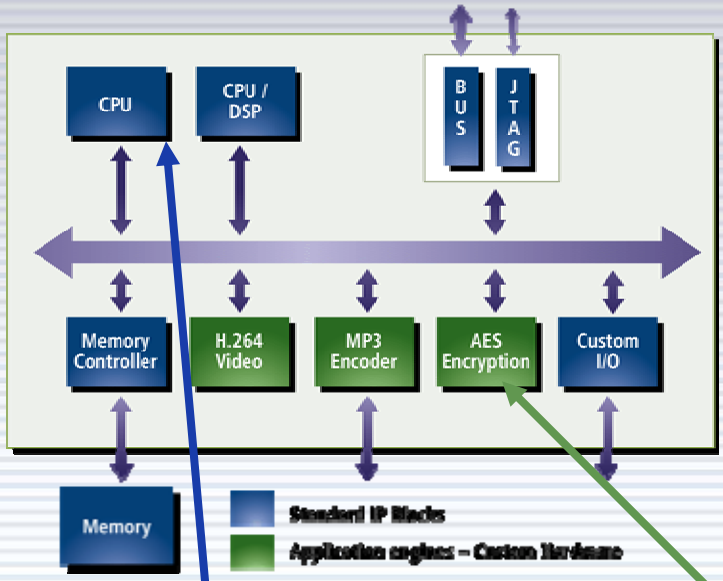
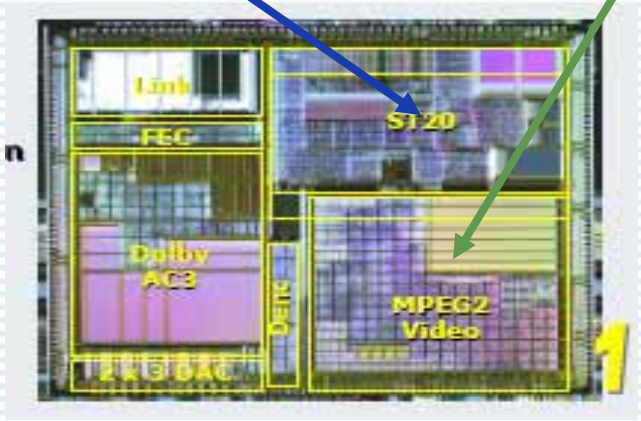
Platform-based MPSoCs



Re-usable Blocks

Complex Algorithmic Engine



- Re-usable "blocks" for a product family
  - µP, bus, bridges & I/O
  - Other off-the-shelf IP
- Interchangeable algorithmic engines based on a product's needs

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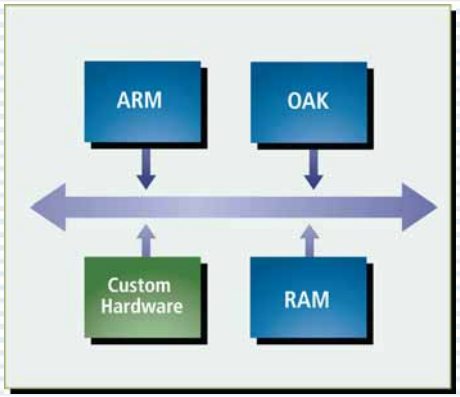
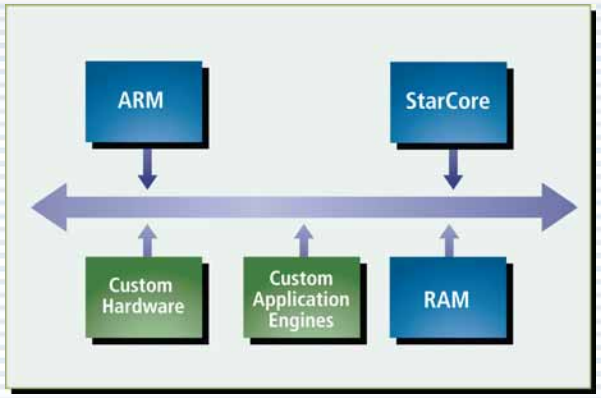
Evolution of Complex Algorithmic Engines

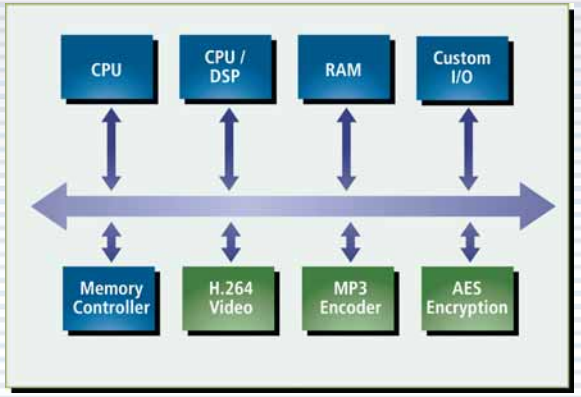
- No longer just “the” MCU/DSP
- A set of application processors dedicated to specific task(s)
- Clean SOC architecture with processors, application processing logic and memories



1995
Non synthesizable processors
Custom Memory
Little algorithmic hardware



2001
Synthesizable processors
(ARM, MIPS, Tensilica)
Compiled Memory (Virage)
Simple custom algorithmic hardware (JPEG)



2006
Synthesizable ARM, MIPS (Tensilica)
Compiled Memory
Complex configurable algorithmic hardware (H.264)

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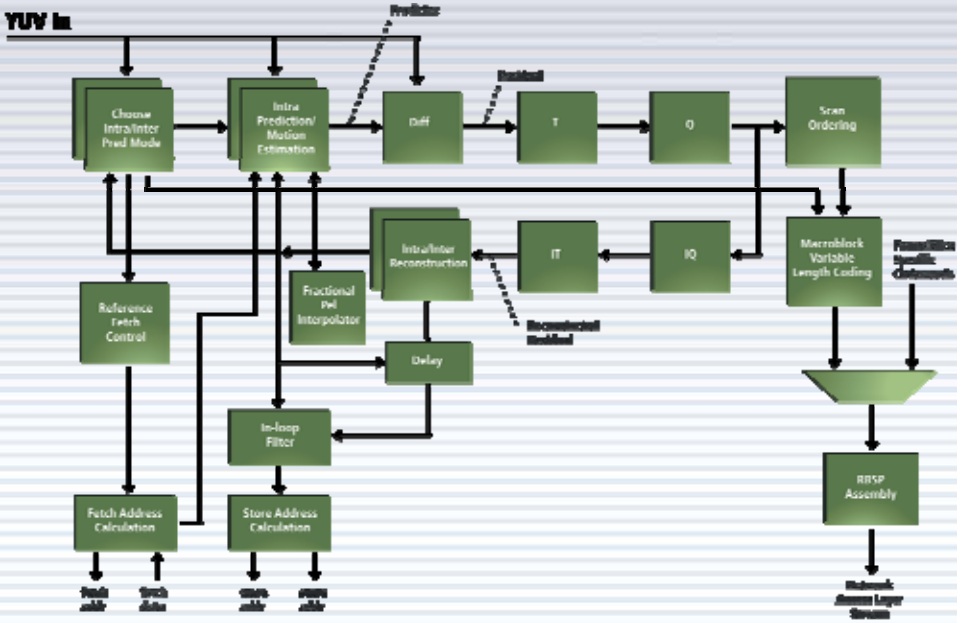
Complex Algorithmic Engines are Multiprocessors

- An efficient architecture is a combination of
  - Dedicated HW blocks
  - Programmable processor(s)
  - Local/global communication and data accesses
- To meet performance/cost goals it is also application-specific



H.264 Encoder Block Diagram

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Key Design Issues

- Rapidly create multiple implementations with different performance – cost - power requirements with minimal efforts and:
  - Concurrency
    - » To cope with Massive Computation
  - Efficient Data Transfer Architecture
    - » To cope with Massive Data Transfer
  - Application Specific computation and communication architecture
    - » To cope with Cost and Power Constraints
  - Higher Level Programming Model and automatic design/mapping
    - » To cope with Huge Design Time
  - Verification of concurrent, mixed HW/SW systems

Adapted from: Ferid Gharsalli, et.al. An Efficient Architecture for the Implementation of Message Passing Programming Model on Massive Multiprocessor SoC

Most Common Complex Algorithmic Engines

SEGMENT	EXAMPLE ALGORITHM
VIDEO	H.264 MPEG 2
AUDIO	MP3 WMA AC3
IMAGING	JPEG
WIRELESS	802.11a 802.11b 802.11g

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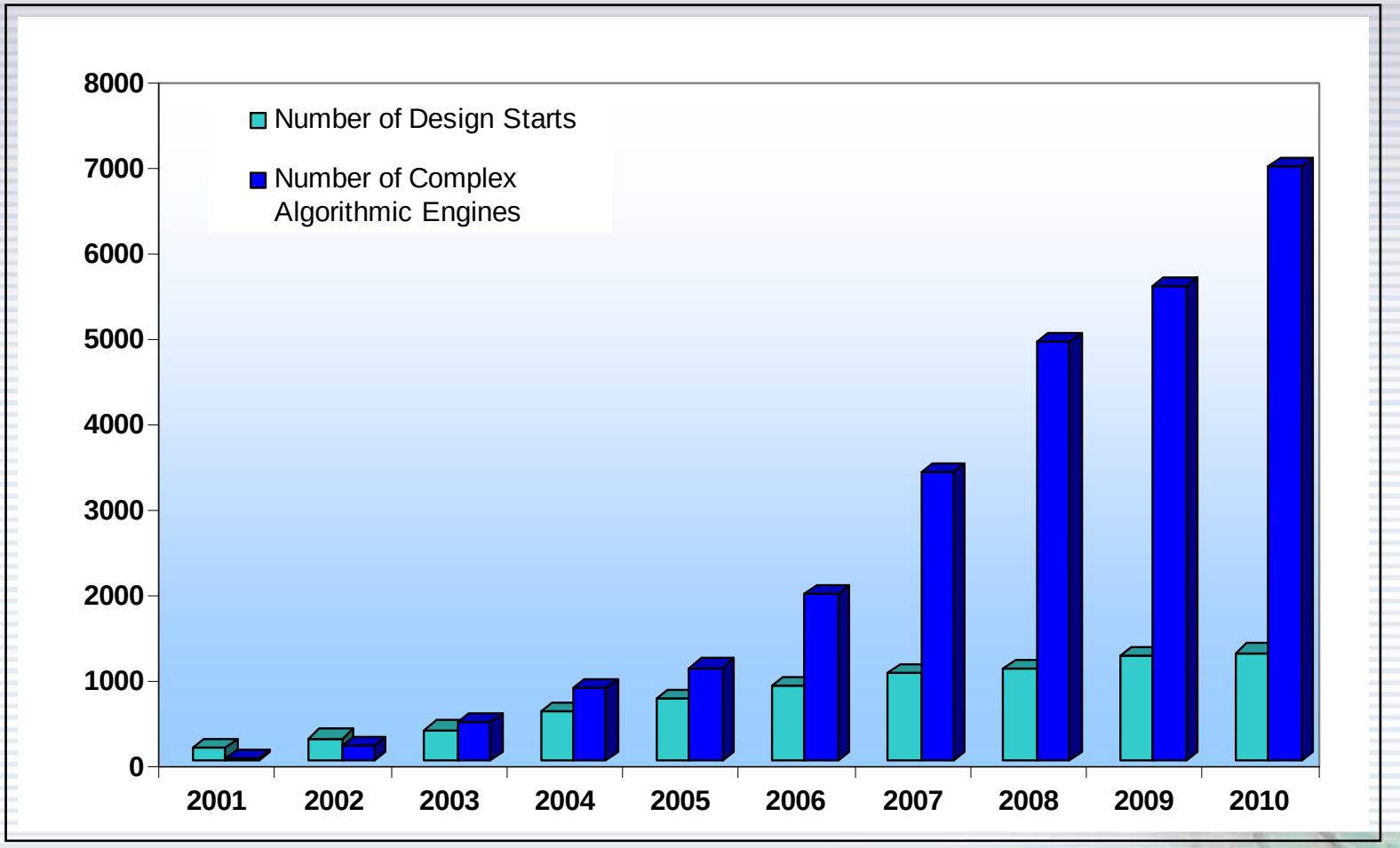
Complex Algorithmic Engines Trend



Source: InStat, IDC, Zoran and Synfora (DSC/Camcorders and 2009-2010 estimates)

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Conclusions

- Complex algorithmic engines differentiate consumer MPSoCs
- The number of algorithmic engines to be designed grows much faster than the number of design starts
- Need chip architectures and design methods for
  - Systems with interchangeable algorithmic engines
  - Automatically implementing complex algorithmic engines with different area/power/performance requirements from a single high level specification

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