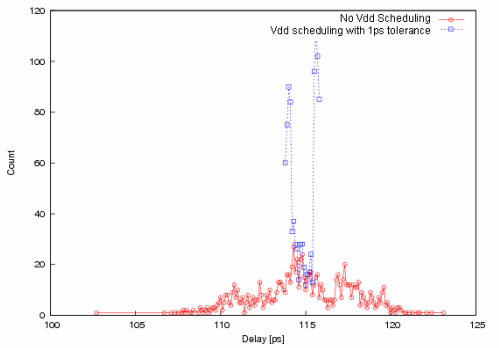
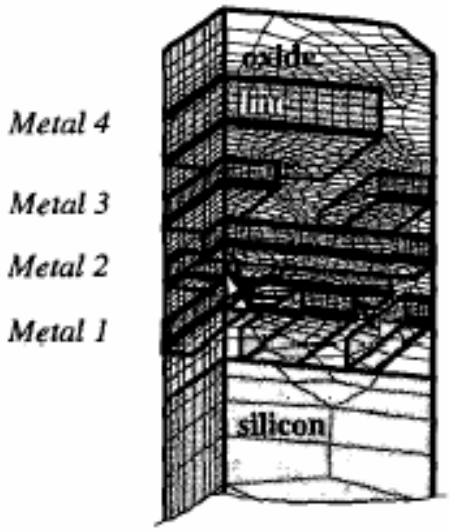
Statistical Design Issues and Tradeoffs in On-Chip Interconnects

$$PDF(I) = f_y(I) = \left(\frac{1}{h'(L)}\right)\left(\frac{1}{\sigma\sqrt{2\pi}}\right)\exp\left(\frac{-(g(I)-\mu)^2}{2\sigma^2}\right)$$





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UMASS Interconnect Circuit Design Group

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  - Recent Grads:
    - Atul Maheshwari (now at Intel)
    - Matt Heath (now at Intel)
    - Aiyappan Natarajan (now at AMD)
    - Vijay Shankar (now at Qualcomm)
    - Anki Nalamalpu (now at Intel)
- Collaborators:
  - Sandip Kundu (UMASS/Intel/IBM)
  - Russ Tessier, Israel Koren (UMASS)
  - Olivier Franza, Mandy Pant, (Intel MMDC)
  - SRC liasons (Intel CRL, Freescale, AMD)

- Selected Alums
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  - Y. Jeong (now Prof at Kwangwoon Univ)
  - Andrew Laffely (now Prof. at U.S. Air Force Academy)
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Abstract

- Interconnects play an increasing role in all aspects of VLSI design, ranging from critical timing paths, to significant aspects of the area/power/energy budget, reliability and security issues, and an increasing portion of the overall design and verification effort.
- With technology advances has come increasing uncertainty in the form of process, temperature, voltage and workload variations.

- Statistical approaches have become necessary in most aspects of design in order to predict costs, performance and reliability measures.

- This talk reviews recent advancements in this area focusing on tradeoffs in on-chip interconnects.
- New unified methods of analysis are proposed as well as architectural and circuit-level methods for mitigating the impact of statistical variation.

- This work is funded by the SRC and Intel.

Outline

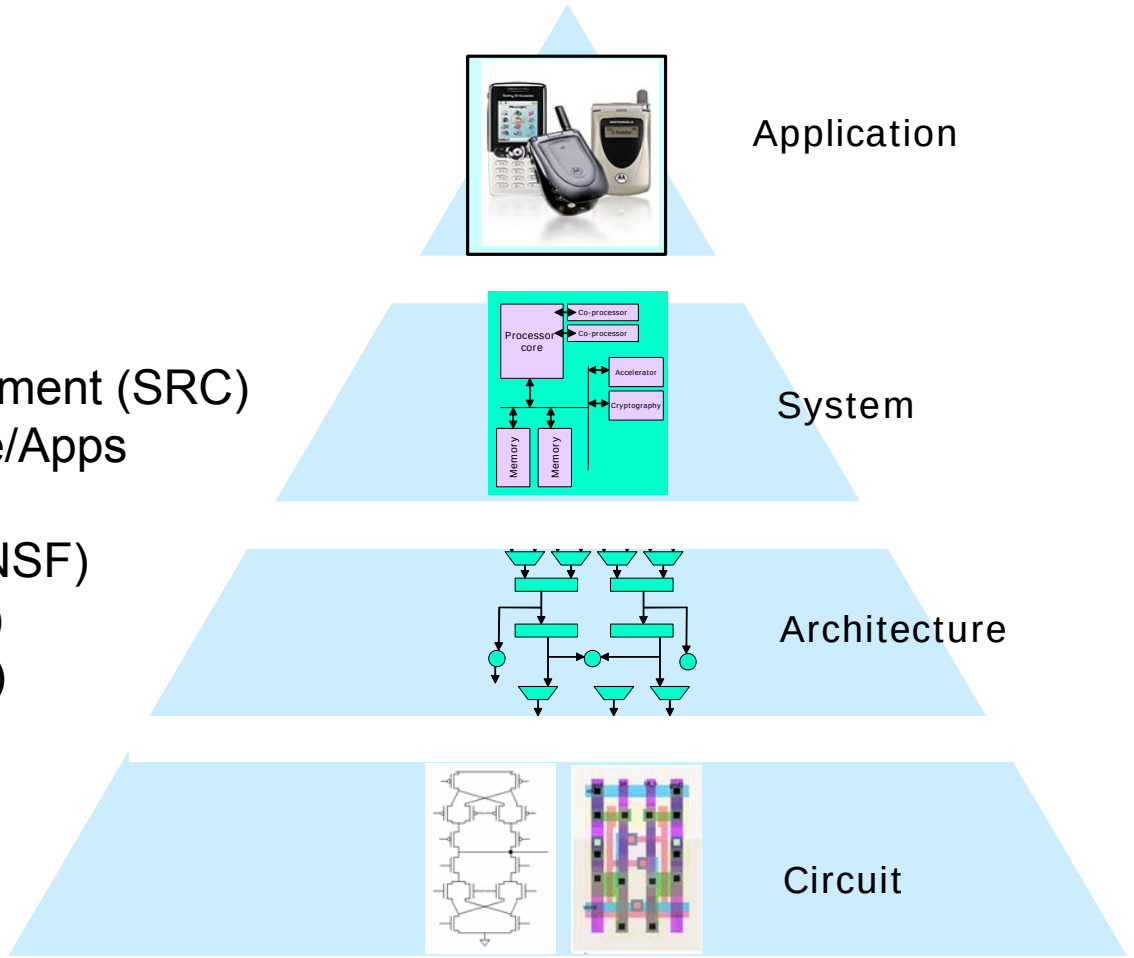
- My Perspective: VLSI Circuits and Architectures
- Motivations: Interconnects
- Why Statistics? Sources of Uncertainty, Metrics, Time Scales, Estimation
- Optimization Scenarios: Bounds, Constraints, Tradeoffs, Pareto-optimality
- Some Recent Work (mine and others)
- Dynamic Tradeoffs?
- Open Problems

Objectives

- Set the context for **on-chip interconnect** design
- Wax philosophical about trends in **design methodology** ☺
- Discuss **impacts of various uncertainties** on design metrics
- Argue the case for **massive SPICE simulation** in addition to analytical approaches
- Survey some **recent research** in statistical approaches
- Present some **challenges and open problems** in the area of statistical interconnect design

My Perspective

- VLSI Signal Processing, BS/MS MIT 1983, PhD Colorado 1989, UMASS 1990-
- Worked as a VLSI Designer (Fairchild, VTI) and teach VLSI Design
- Research in VLSI Circuits
  - Low-power (NSF, SRC)
  - Interconnects (SRC, Intel)
  - Wave-pipelining (NSF)
  - SRAM (Intel, CRL)
  - Soft-errors (Intel, MMDC)
  - Clocking (Intel)
  - Thermal Sensing/Management (SRC)
- Research in VLSI Architecture/Apps
  - Adaptive SOC (NSF)
  - VLSI Signal Processing (NSF)
  - Video, 3D Graphics (NSF)
  - Embedded Security (NSF)



Deep sub-micron effects: The Dark side of Moore's Law

- Delay
  - Short channels, velocity saturation, variations, supply noise, interconnects, clock rates, gates per cycle, pipelining, voltage scaling, threshold scaling
- Energy/Power
  - Dynamic: Clock rates, activity factors, capacitance, thermal effects
  - Leakage: Voltage/threshold scaling
- Reliability
  - Lower C, lower V, lower Qcrit, more bits, more process variation, more coupling, more supply noise

What do we mean by statistical?

- Sources of randomness (voltage, temperature, process, radiation, workload)
- Statistical models? What's really random?
  mean, variance, correlation
- Impact on Metrics: constraints, margins, yield, speed binning, power binning
- Test-time: Yield enhancement techniques: e.g. spares
- Run-time: Error correction/detection
- Nanotechnologies?

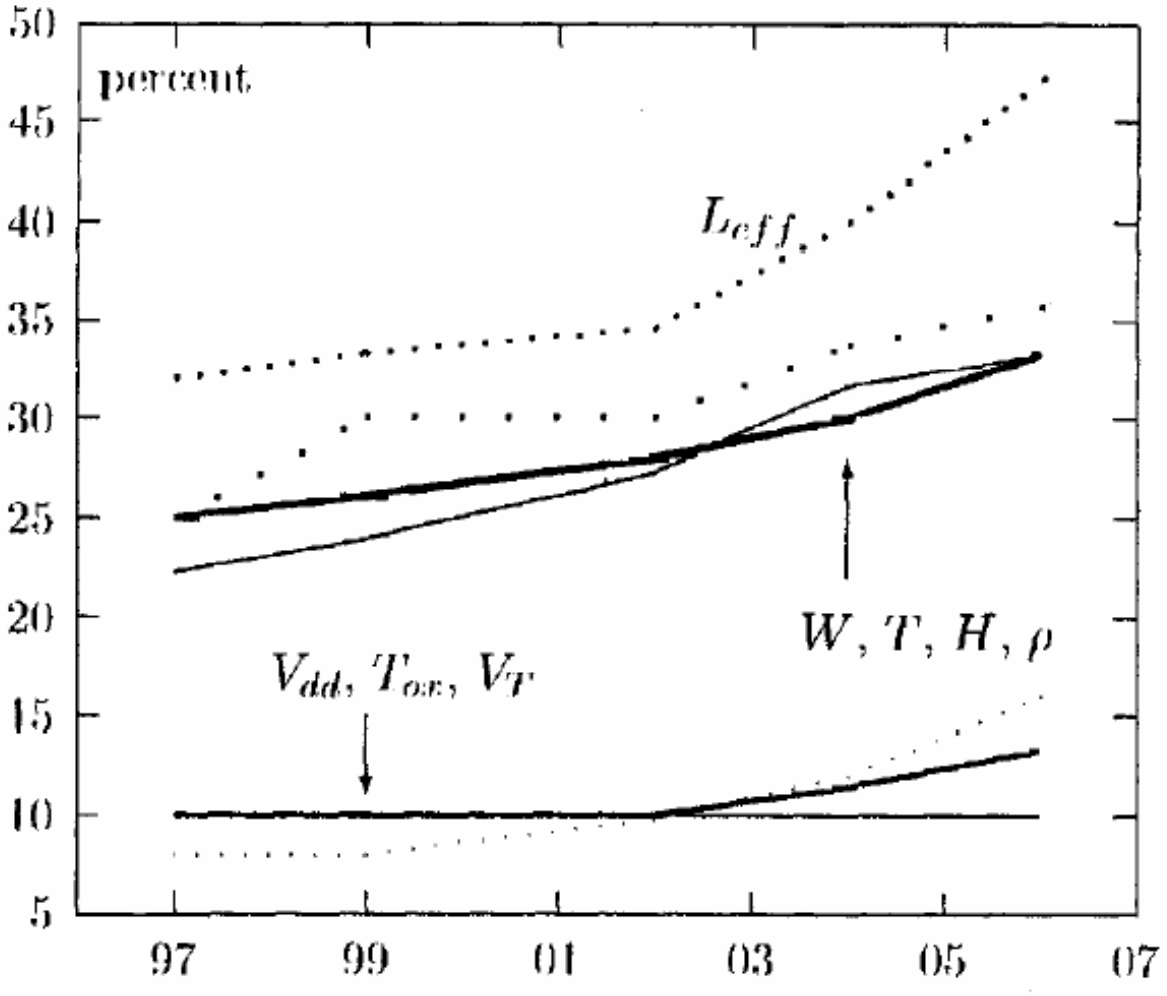
Statistics

- Worst-case vs. average case vs. variance vs. full distributions (Normal?)
  - Delay –
    - Worst-case for clock rate
    - Average case for benchmarks
  - Energy –
    - Worst-case for power distribution and thermal
    - Average-case for battery life
  - Error
    - FIT, MTBF, System Down-time, Silent Data Corruption

Time Scales

- Peak (single cycle)
  - Set-up or hold time violation
  - Noise spike causing logic error
- Very Short (1's to 10's of cycles)
  - Power distribution network time constant
  - Clock distribution latency
- Short time scale (10's to 100's of cycles)
  - Thermal time constants
  - PLL lock time
- Long time scale (minutes/hours/days/years)
  - Battery life
  - Electromigration
  - System/application reliability (radiation-based)

Trends in Process and Voltage Variations



Nassif, ISQED, 2000

Sources of uncertainty and their impact on metrics

Source/Metric	Delay	Power	Reliability
Supply Voltage	Device speed either too slow or too fast	Dynamic power, Leakage, Static	Hot Carrier, SRAM Vmin
Temperature	Device speed, Interconnect Resistance	Leakage	Oxide breakdown, metal self-heating, PMOS Bias Temp
Process - Materials and Doping - Lithographic - Oxide thickness - Metal polish, etch	Device Leff, Weff, Ron, C parasitics, threshold voltage, wire R, oxide thickness	Dynamic power, Leakage, Static power	Writability failure, wearout, metal migration, …
Particle Hit - Type: Alpha, Neutron - Charge, Location, Time	Charge injection either speeds up or slows down critical transitions	*not significant*	Bit-flip, delay fault
Control/Data	Rise/fall variation, coupling,	Activity factor, state dependent leakage	Logic masking, Architectural masking

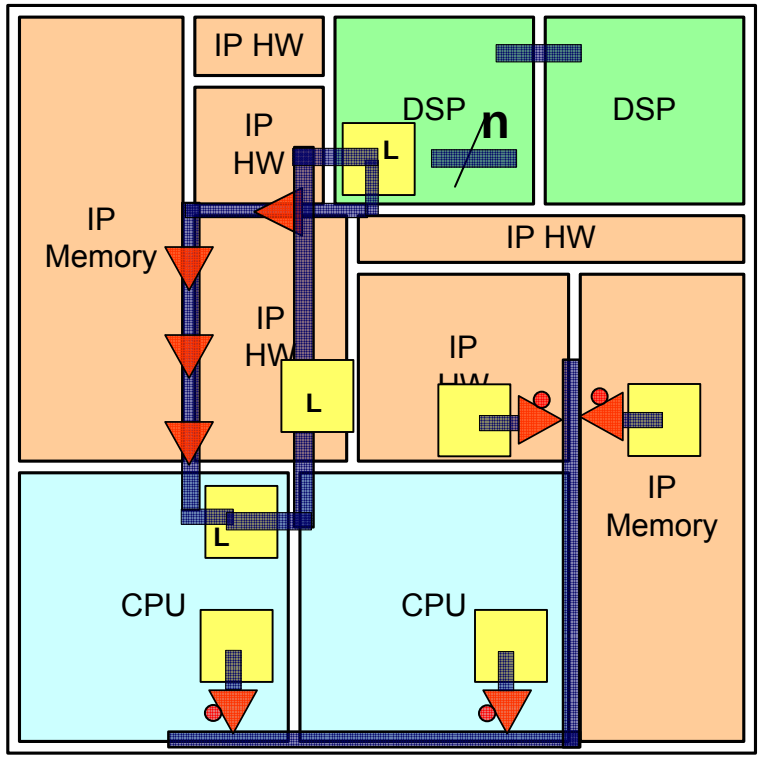
Why are interconnects of increasing importance?

- Technology trends: Moore's Law, More layers, more complex circuits
- Architectural trends: Parallelism, memory systems, flexibility
- CAD/Methodology trends: re-use, synthesis, shrinks, timing closure

Interconnect is the crux of divide-and-conquer, the fundamental method for managing complexity

MPSoC Interconnects

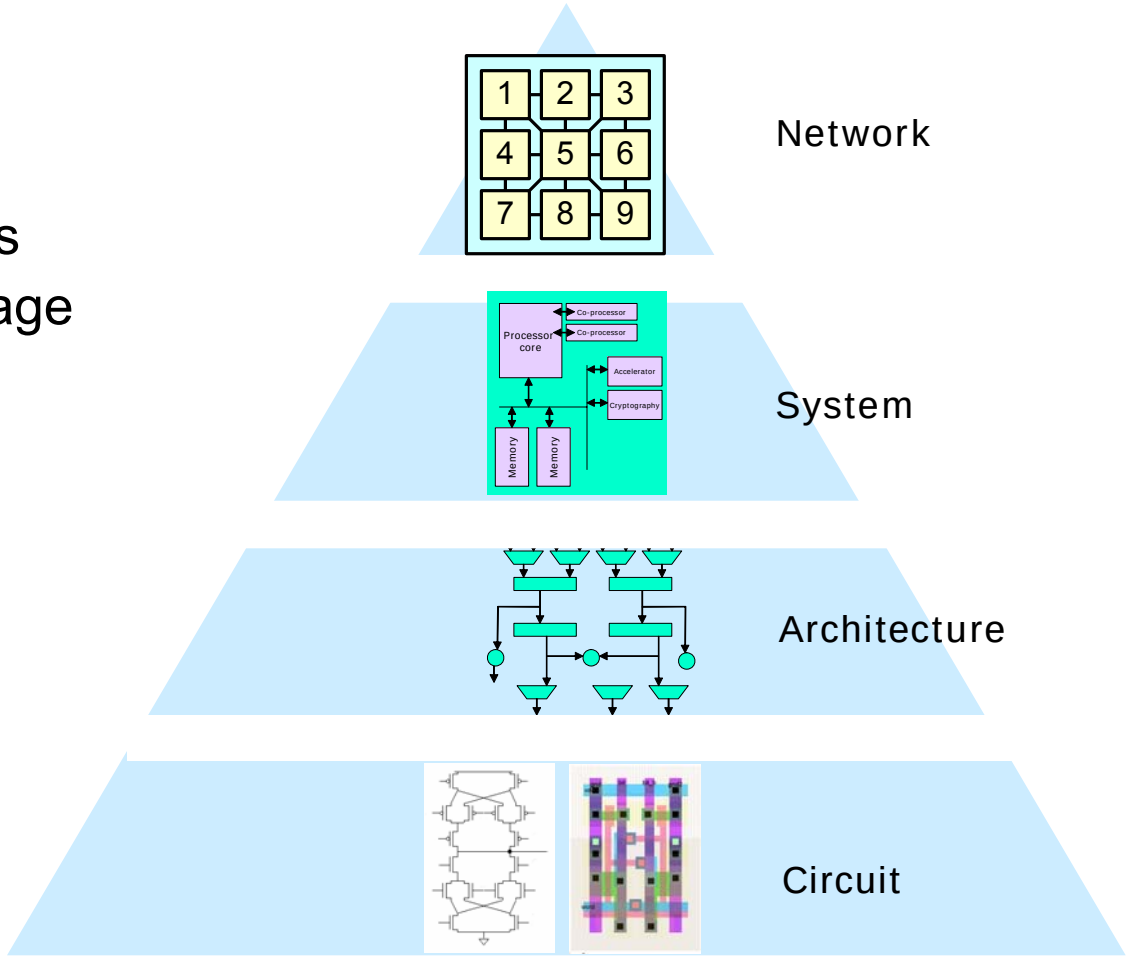
- Intra-core vs. inter-core,
- Bus-width (1,8,...32,64,...)
- Adjacent core vs. long-haul
- Repeated vs. unrepeated
- Single-cycle vs. pipelined
- Bus vs. point-to-point
- Synch vs. asynch
- Metrics:
  - Latency
  - Bandwidth
  - Noise
  - Area
  - Power/Energy



Source : A. Jerraya, W. Wolf, **Multiprocessor Systems-on-Chips**, Elsevier 2005

On-Chip Interconnect: Levels of Abstraction

- Network level
  - CDMA
  - TDMA
- System level
  - Communication Links
  - Adaptive supply voltage links
- Architecture level
  - AMBA™
  - CoreConnect™
  - Sonics
- Circuit level
  - Low Swing
  - Coding
  - Single / Differential



Interconnect Geometry Scaling

Layer	Pitch (nm)	Thick (nm)	AspectRatio
Isolation	220	320	-
Polysilicon	220	90	-
Contacted gate pitch	220	-	-
Metal 1	210	170	1.6
Metal 2	210	190	1.8
Metal 3	220	200	1.8
Metal 4	280	250	1.8
Metal 5	330	300	1.8
Metal 6	480	430	1.8
Metal 7	720	650	1.8
Metal 8	1080	975	1.8

65nm Intel© Technology

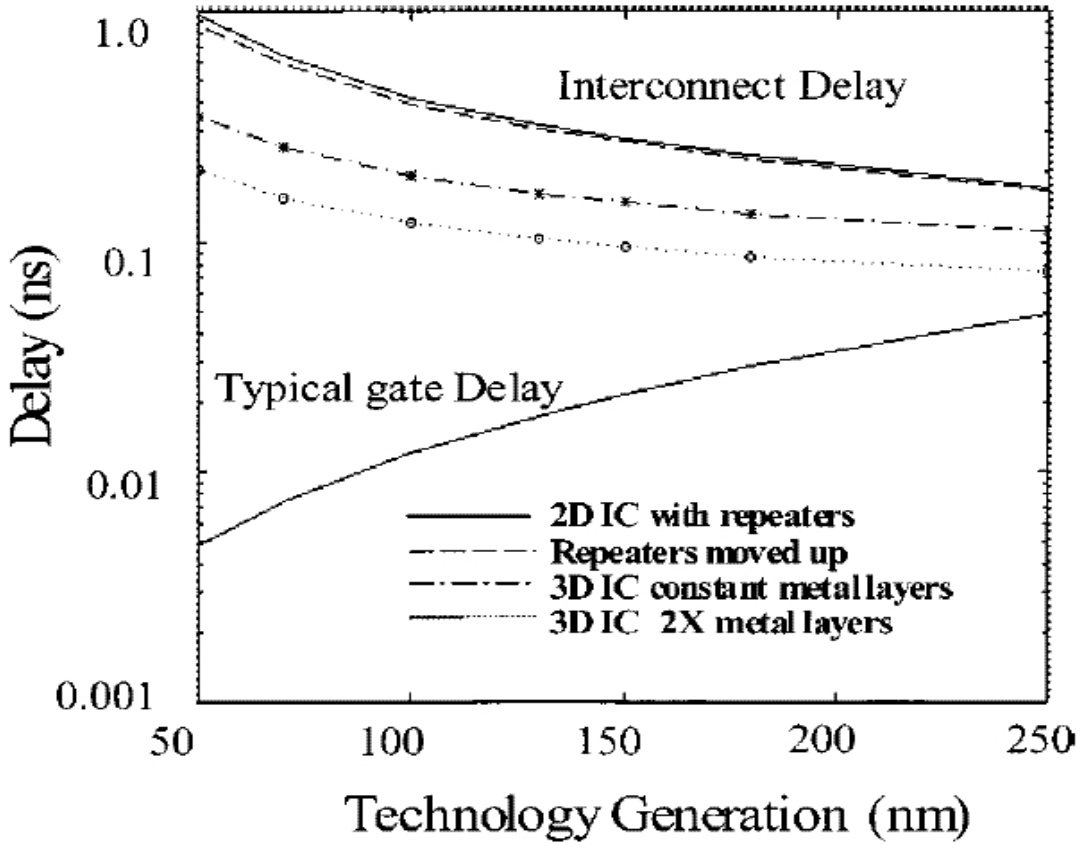
LAYER	PITCH	THICK	AR
Isolation	240	400	-
Poly-Si	260	140	-
Metal 1	220	150	1.4
Metal 2,3	320	256	1.6
Metal 4	400	320	1.6
Metal 5	480	384	1.6
Metal 6	720	576	1.6
Metal 7	1080	972	1.8

90nm Intel© Technology

- Weak scaling of vertical dimension compared to horizontal dimension
- Extremely high height/width aspect ratios
- Reduces degradation of interconnect resistance

Source : **90nm Intel© Technology**, Thompson, IEDM, 2002, **65nm Intel© Technology** Bai, IEDM 2004.

Interconnect RC Trend

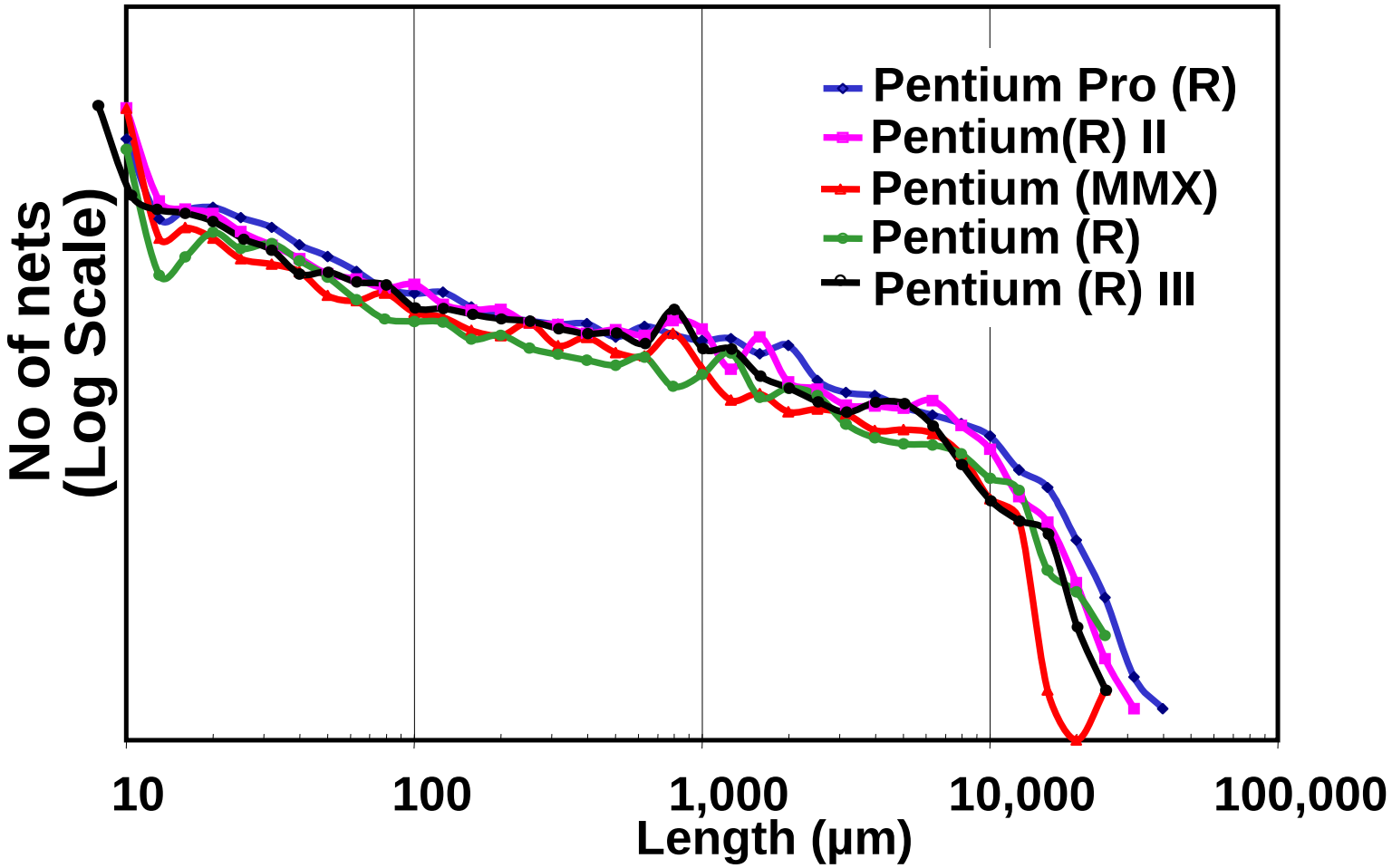


% increase each generation	R	C	RC
Poly	45%	-2%	42%
M1	53%	5%	61%
M2	46%	12%	62%
M3	39%	8%	51%
M4	18%	24%	46%

- RC/μm increases 40-60% per generation
- Copper, low-K dielectric: modest benefit

Borkhar, Intel, 2004

Interconnect Distribution Trend



RC/µm scaling trend is only one side of the story…

Average wire lengths don't scale well

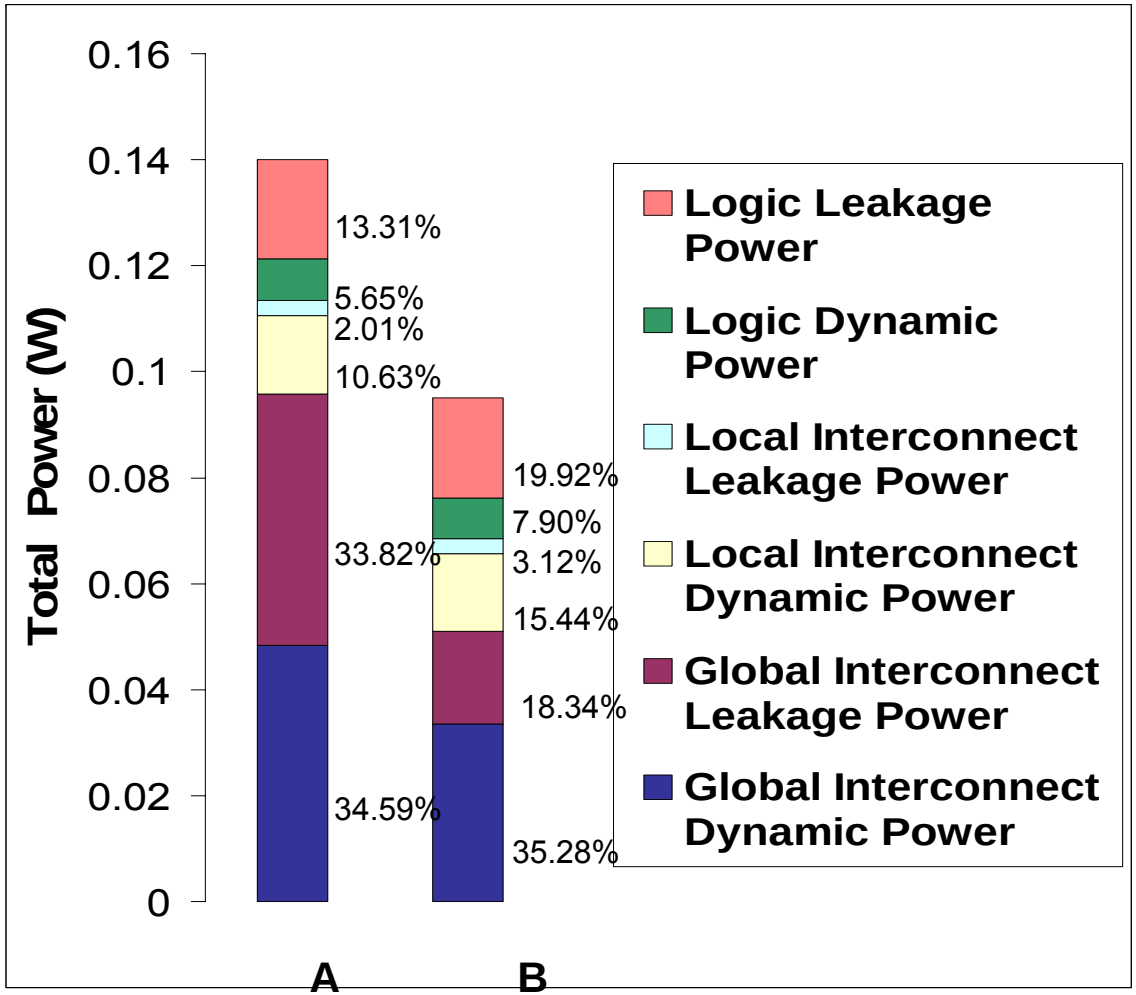
What about more recent processors P4, Itanium, Cell?

Interconnect Power Consumption

- Using Vdd programmability
- High Vdd to devices on critical path
- Low Vdd to devices on non-critical paths
- Vdd Off for inactive paths

A – Baseline Fabric

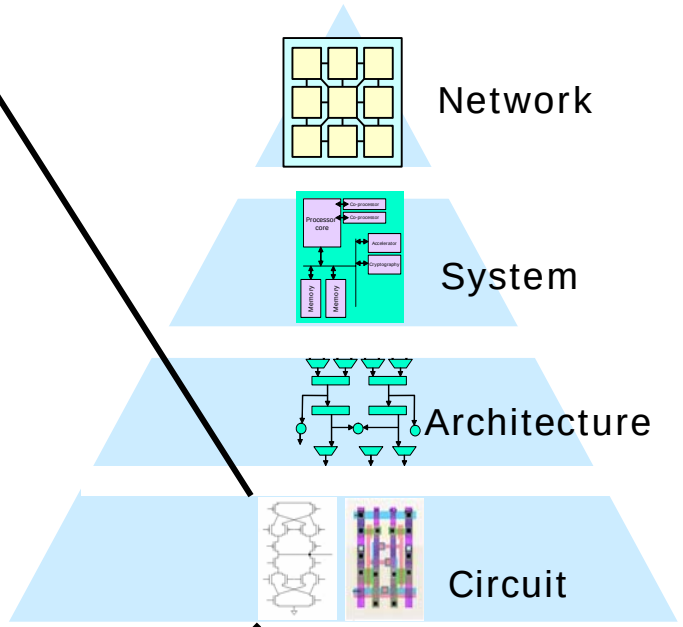
B – Fabric with Vdd Configurable Interconnect



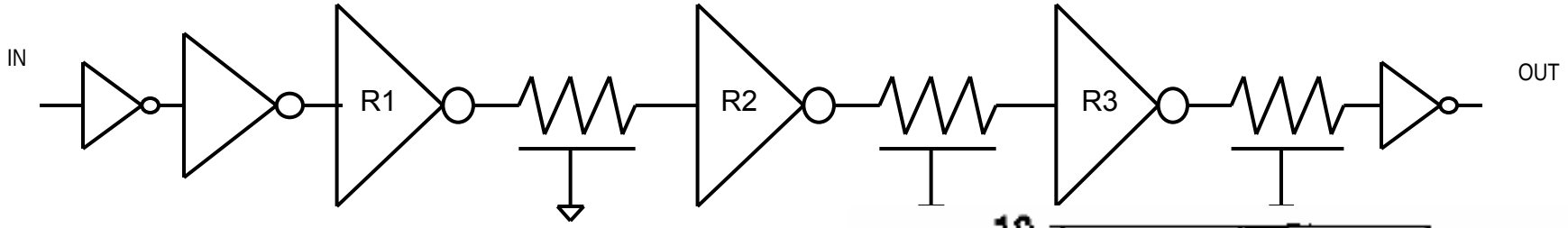
This work builds on a similar idea for FPGAs described in:
Fei Li, Yan Lin and Lei He. *Vdd Programmability to Reduce FPGA Interconnect Power*, IEEE/ACM International Conference on Computer-Aided Design, Nov. 2004

Circuit and Signaling Solutions

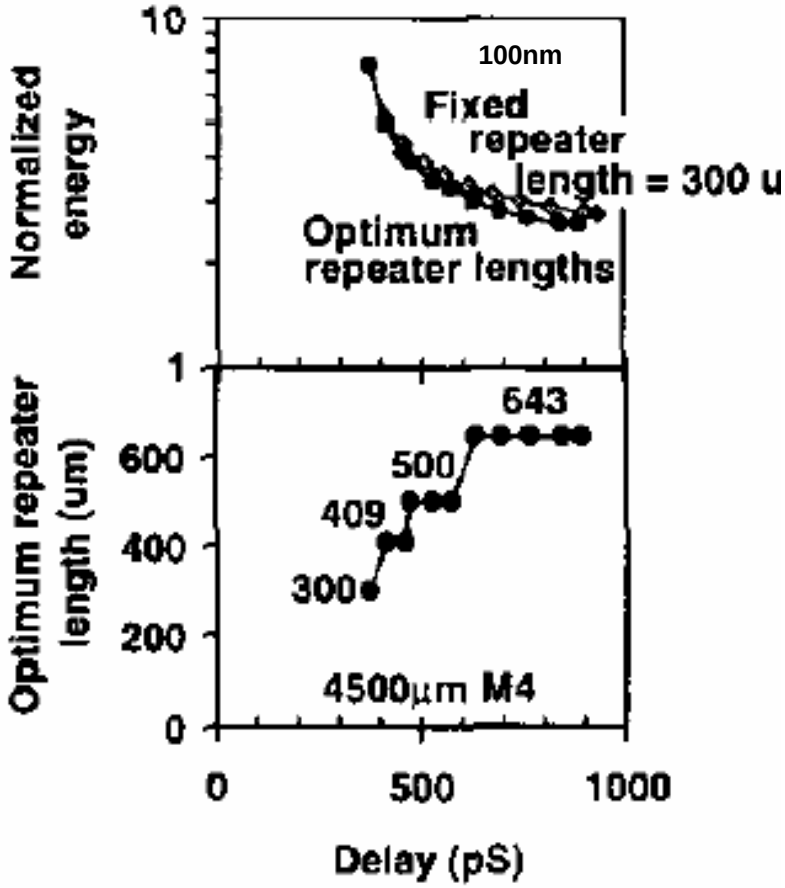
- Conventional Circuit techniques
  - Repeater insertion
  - Booster insertion
- Low Swing techniques
  - Pseudo differential interconnect
  - Differential Current sensing
- Bus encoding techniques
  - Transition aware encoding
  - Low Power encoding for crosstalk reduction
- Signaling techniques
  - Multi-level signaling
  - Near speed of light signaling



Interconnect Circuits - Repeater



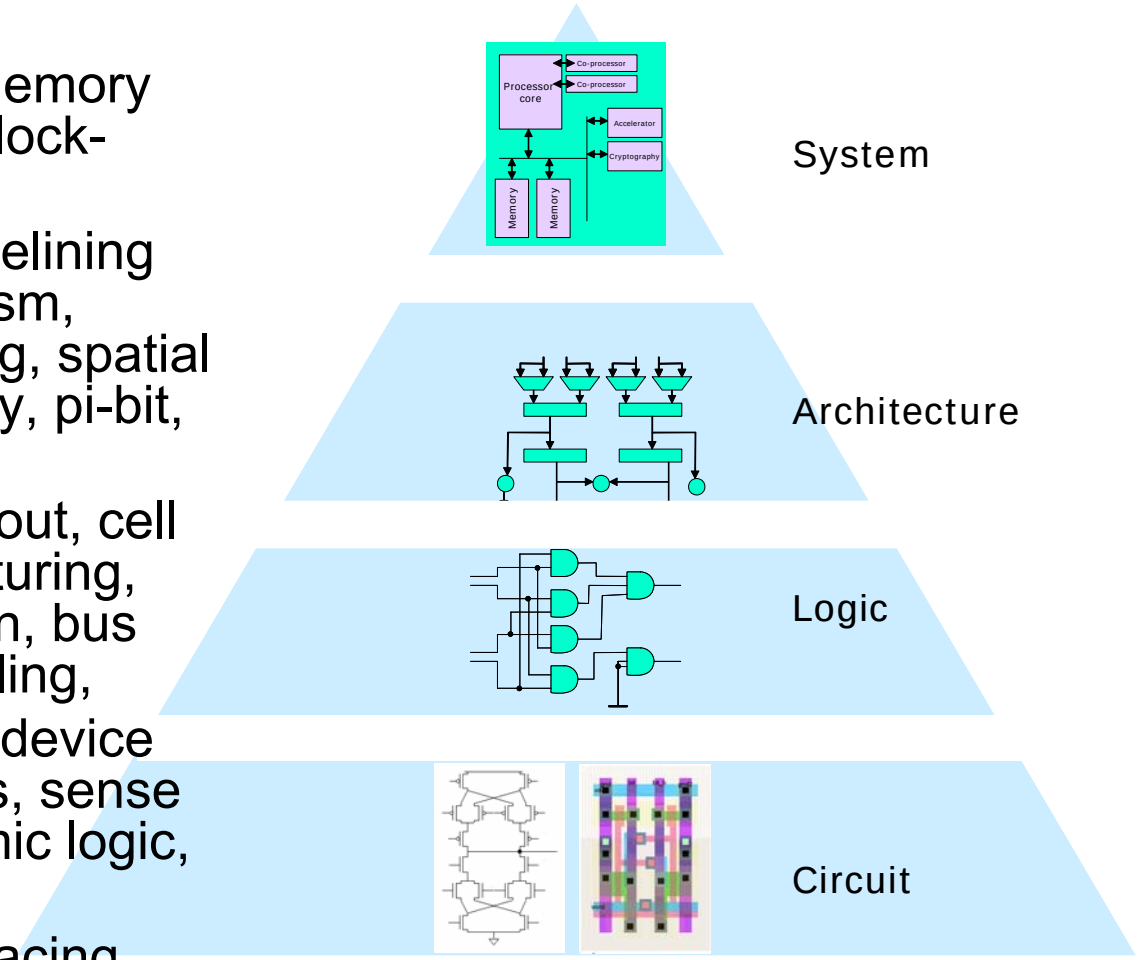
- Optimum repeater insertion reduces interconnect delay.
- Optimized energy-delay tradeoffs used to satisfy design criteria.



Khellah, VLSI Symposium, 2003

Performance/Energy/Reliability tradeoffs in interconnects

- **System level** : GALS, memory systems, I/O, multi-core,lock-stepping, re-boot
- **Architectural level :** pipelining instruction-level parallelism, redundant multi-threading, spatial and temporal redundancy, pi-bit, checkpointing/rollback,
- **Logic level** : fan-in, fan-out, cell library, algebraic restructuring, parity checking/prediction, bus coding, differential signaling,
- **Circuit level** : Vdd, Vth, device sizing, redundant latches, sense amps, capacitors, dynamic logic, shielding
- **Layout level:** Sizing, spacing, orientation, floorplanning,



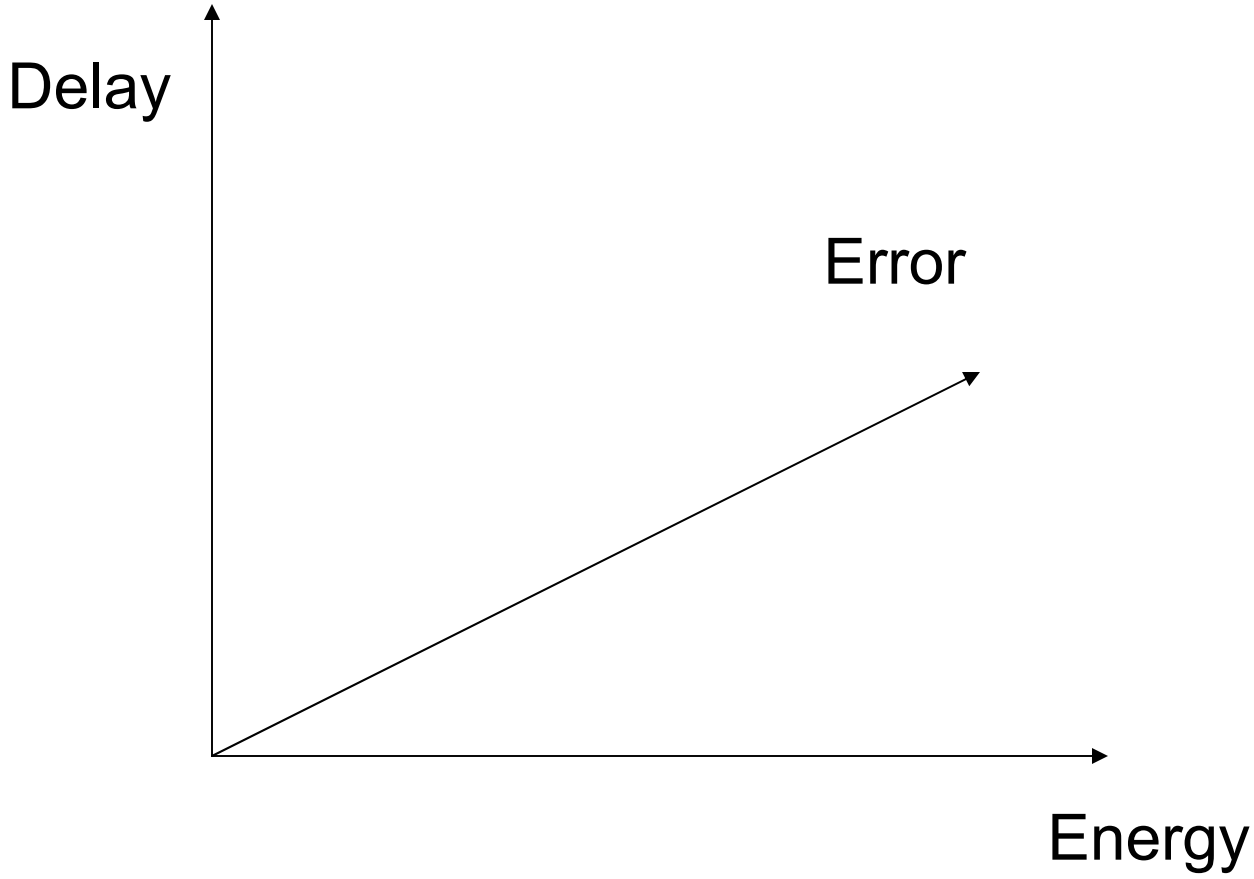
Scales/Correlation

Source	Spatial	Temporal	
Supply Voltage -**1st droop** - **2nd droop** - **3rd droop**	Chip cm Region mm-cm Module mm	usec nsec 100's of psec	
Temperature	mm	usec	
Process - Doping - Lithographic - Materials - Oxide thickness - Metal polish, etch	Single Device		
Particle Hit - Type: Alpha, Neutron - Charge, Location, Time	Single device, Up to 3-4 devices	psec	
Control/Data	Single device	Single cycle	

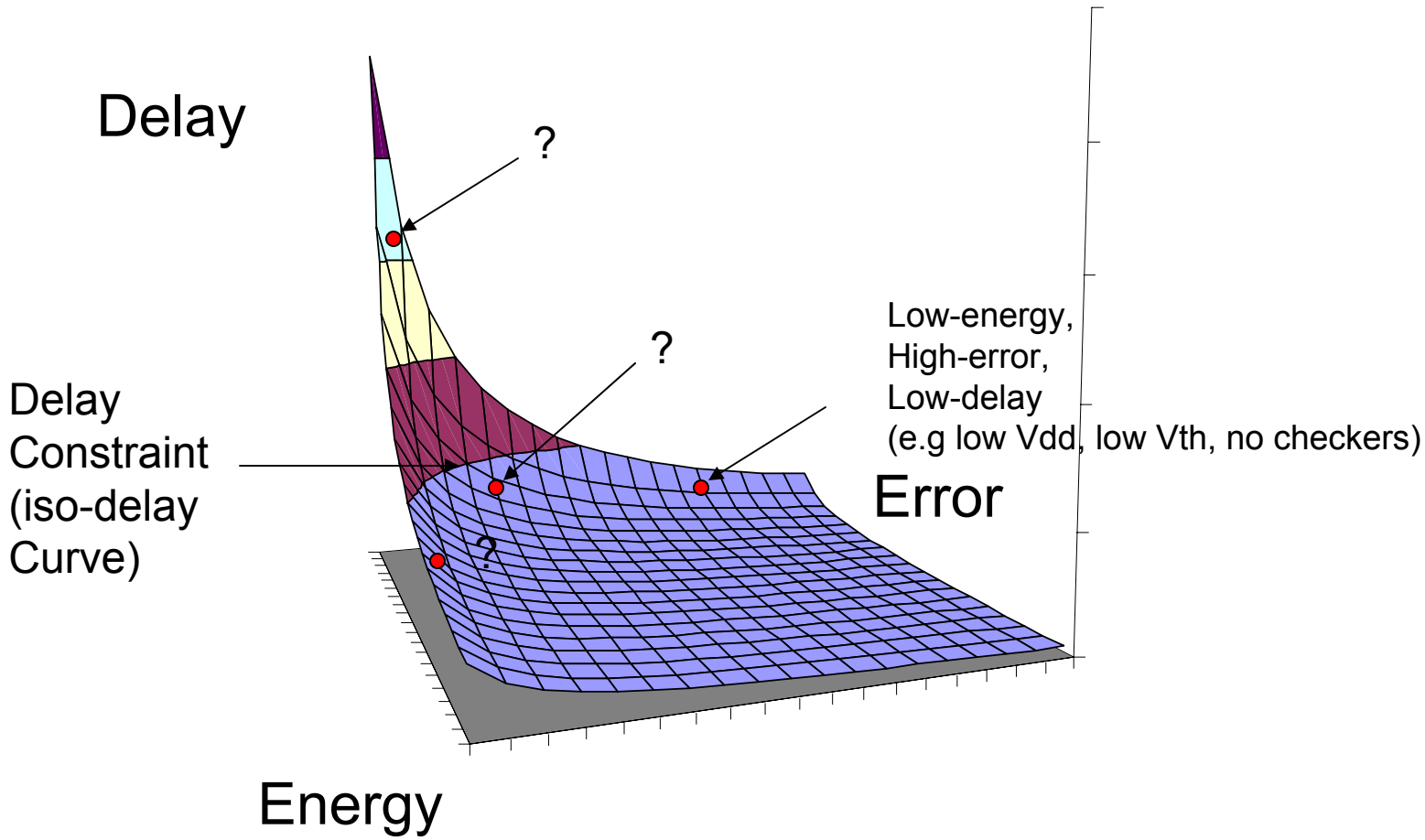
Metrics

- Initially, let's define them all as things to minimize, ie. **Delay, Energy, Error**
- **Delay** is a path or set of paths
- **Energy** is a weighted sum over the entire design over some time period or workload
- **Error** is a weighted sum over the entire design, typically represented as a probability of failure

The Delay, Energy, Error space



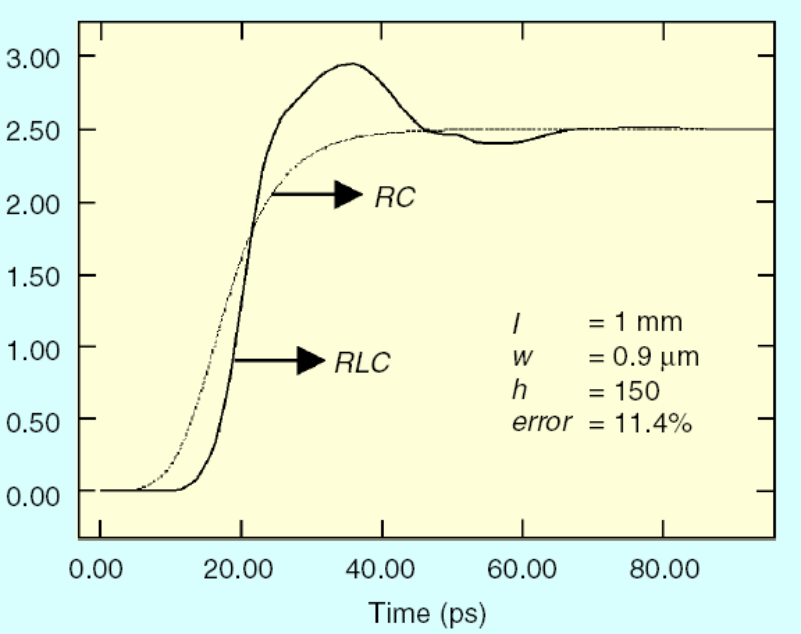
The Delay, Energy, Error space

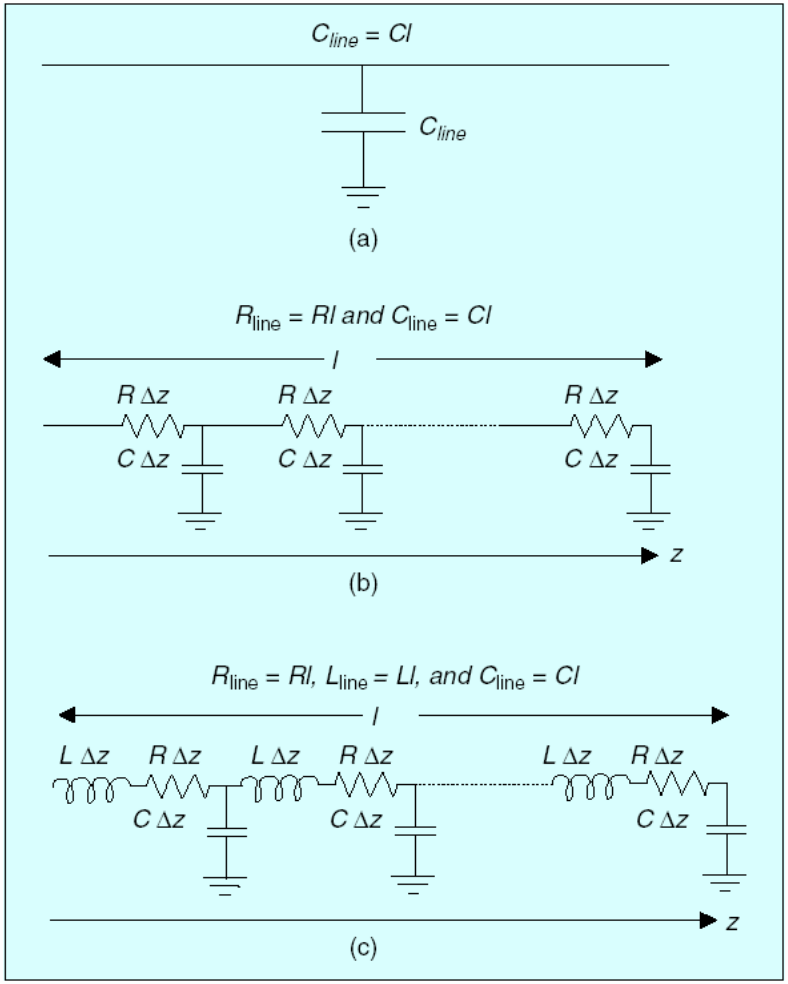


Delay Modeling and Estimation

- Longest path in graph
  - Weights depend on physical layout (ie wire-load models)
- What's hard:
  - Early estimation of layout
  - Process variation (devices, wires)
  - Noise (coupling, supply, substrate)
  - Logic (worst-case pattern, false-paths, coupling patterns)
- State-of-the-art
  - Parasitic extraction (C, C+, RC+, RLC+)
  - Static Timing Analysis considering logic sensitization
  - SPICE of critical paths including worst-case coupling
  - Statistical analyses of variation (mostly just for clocks)

Interconnect Modeling





a. Capacitive model

b. RC model

c. RLC model

Massoud, Ckts and Devices Mag, 2001

Statistical timing design

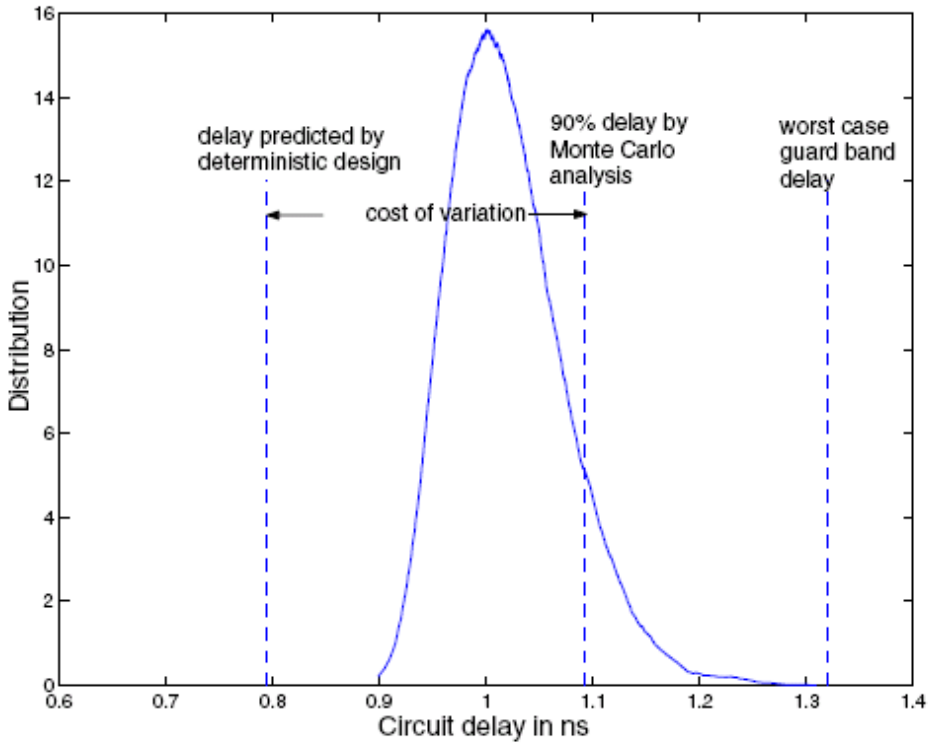


Figure 1. Monte Carlo Analysis on a deterministically sized 32-bit adder

A New Method for Design of Robust Digital Circuits

Dinesh Patil, Sunghee Yun, Seung-Jean Kim, Alvin Cheung, Mark Horowitz and Stephen Boyd

Department of Electrical Engineering, Stanford University, ***ISQED 2005.***

Energy Modeling and Estimation

- Broken down into Dynamic, Static, Leakage
- Dynamic: well understood, includes glitch and short circuit power
- Static: pseudo-NMOS, sense-amps, bleeders, biasing circuits,PLL
- Leakage: sub-threshold, gate, DIBL, etc. increasing concern
- What's hard:
  - Data patterns
  - Leakage variations due to process and temperature
  - Modeling leakage improvement techniques (e.g. power gating, stacking, adaptive body biasing, etc.)
- State-of-art
  - Low-level: Powermill or SPICE accurately models device, but not variations or logic issues. Not statistical. Monte Carlo approaches help.
  - High-level: RTL estimation models logic and system-level (ie power-down) issues well but not device or timing issues. Not statistical.

Intra- vs. Inter-die process variation

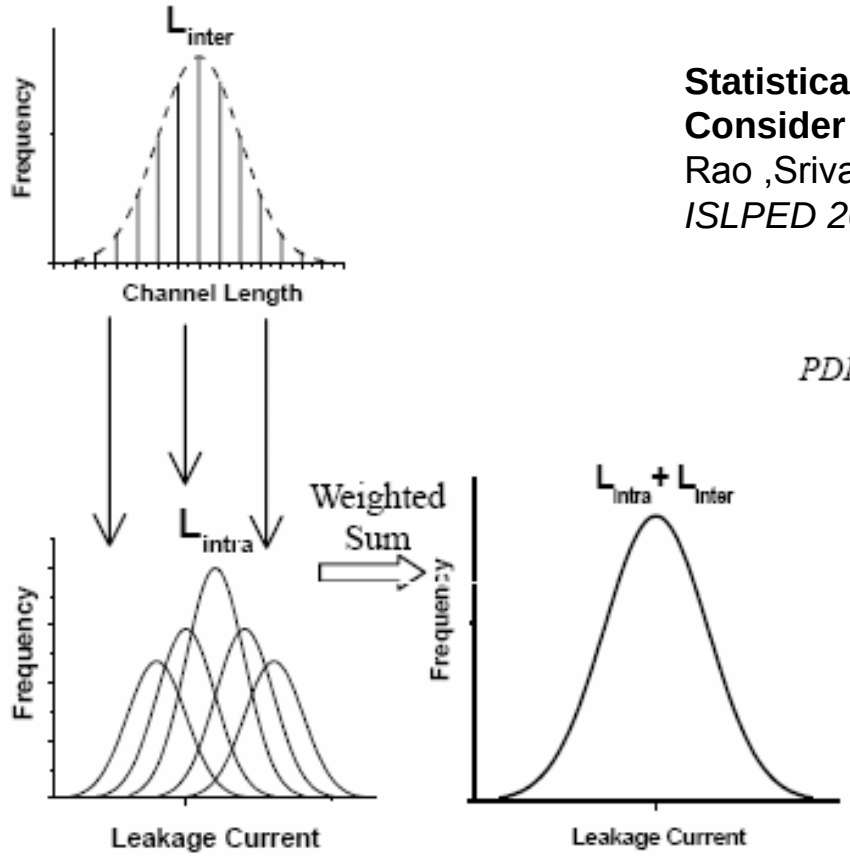
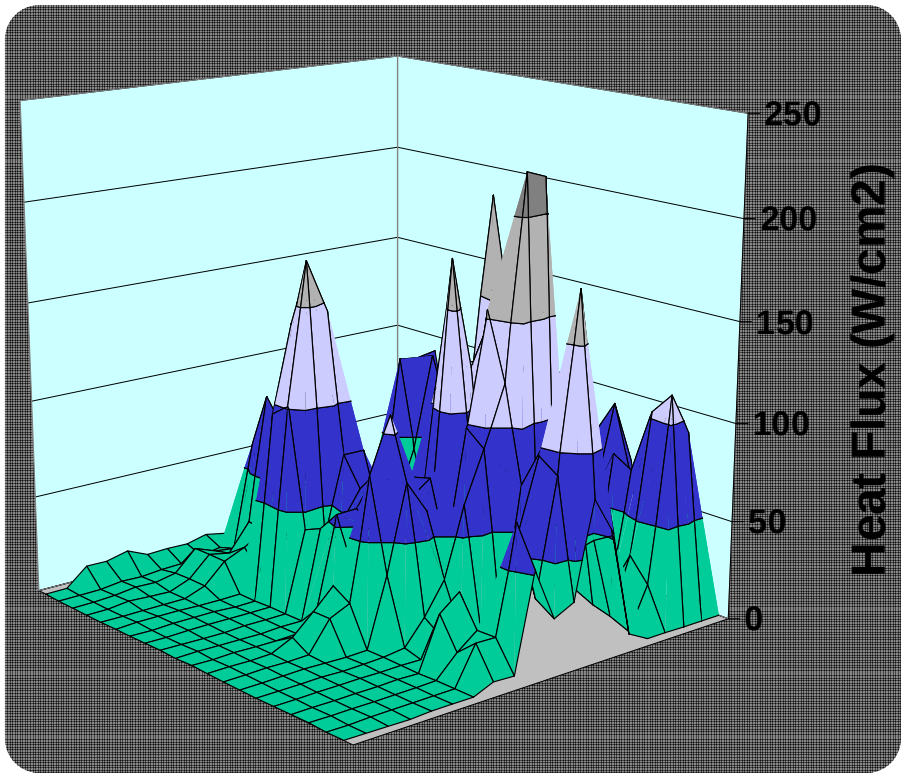


Figure 4. PDFs for (a) Channel length considering only L_{inter} (b) Leakage current corresponding to each point in (a) considering L_{intra} (c) Leakage current considering both L_{inter} and L_{intra}

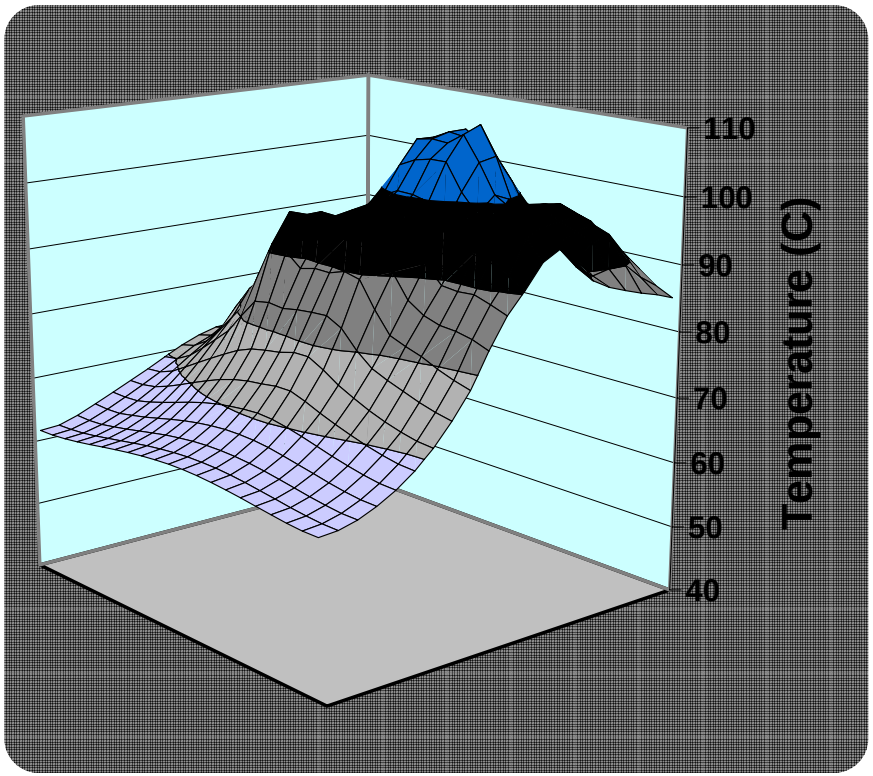
Statistical Estimation of Leakage Current Consider Inter- and Intra-Die Process Variation
Rao ,Srivastava, Blaauw, Sylvester, (Michigan),
ISLPED 2003.

$$PDF(I) = f_y(I) = \left(\frac{1}{h'(L)}\right)\left(\frac{1}{\sigma\sqrt{2\pi}}\right)\exp\left(\frac{-(g(I)-\mu)^2}{2\sigma^2}\right)$$

Heat Flux & Temperature Variation



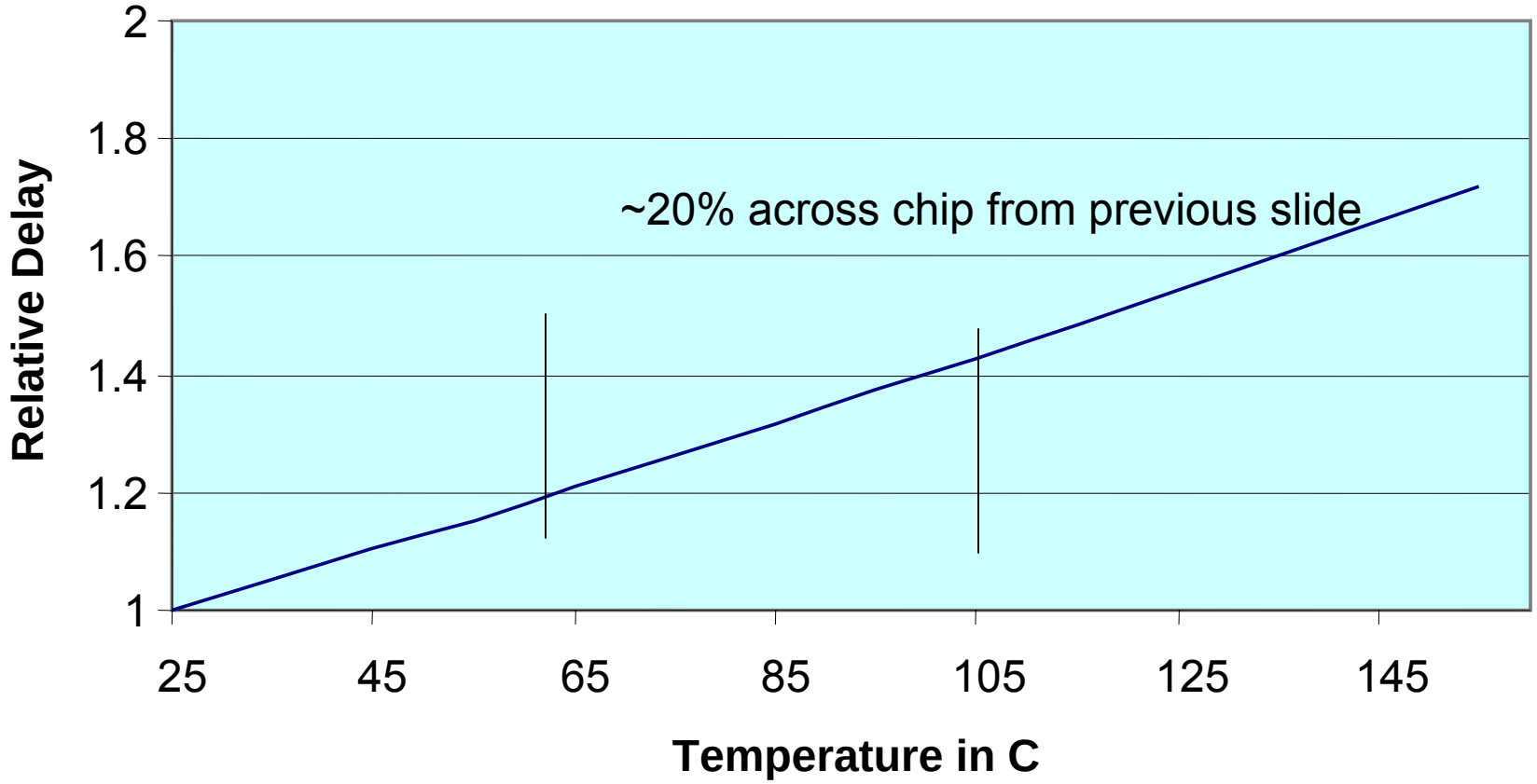
Heat Flux (W/cm²)
Results in V_{cc} variation



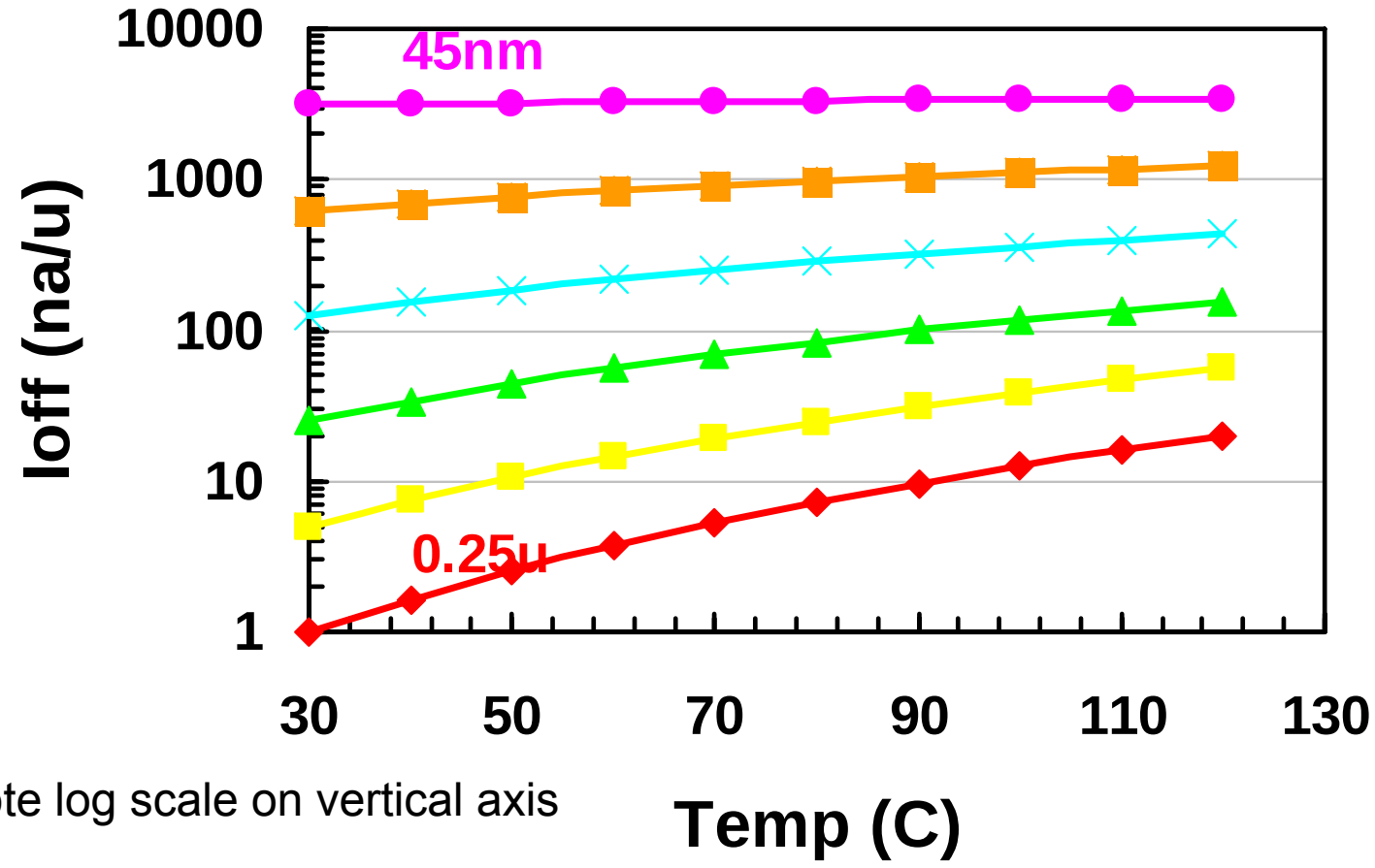
Temperature Variation (°C)
Hot spots

Source: Pat Gelsinger, Intel

Delay Impact of Temperature



Leakage current against temperature



Note log scale on vertical axis

Source: Pat Gelsinger, Intel

How to estimate statistical metrics for interconnects? Analysis or Simulation?

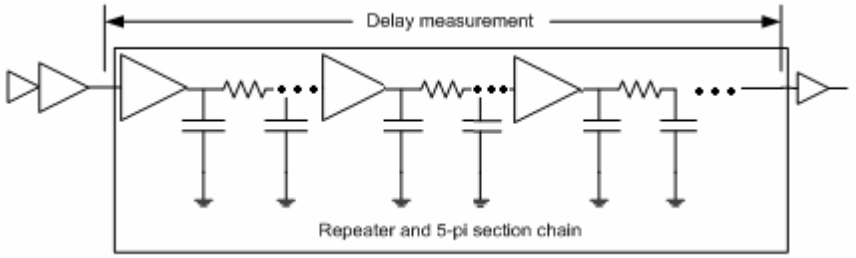
- Most statistical analysis problems have become intractable or highly dependent on lower level approximations of circuit, device and interconnect behavior. (Examples include various commercial timing analyzers, power estimators, yield analysis tools and soft-error analyzers).
- In contrast, for interconnects, SPICE simulations are now robust enough to be run as the inner loop of Monte Carlo, optimization and other design exploration programs. As long as appropriate model files are available, SPICE provides an excellent vehicle for statistical interconnect design.
- We use a commercial SPICE (Synopsys HSPICE) running on a farm of 10-20 Linux PCs. PERL is used to create SPICE circuit and excitation files, spawn jobs on the farm or remotely, gather and analyze data, spawn new jobs, and format results.
- Simple interconnect circuits take up to 30 seconds to simulate in SPICE. Monte Carlo simulation for process, voltage, and temperature variation analysis on simple interconnect spice circuits including simulation for design space exploration takes up to 9 hours

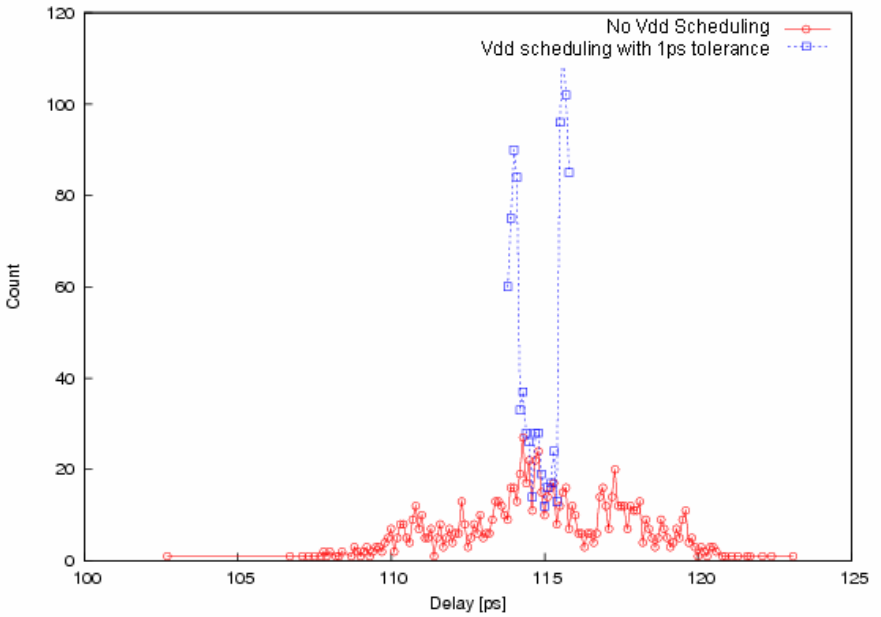
An Example:

Process Variation-Aware Repeater Insertion

I. Benito (MS Thesis) , V. Venkatraman, W. Burleson

- Objective: Minimize delay variation in repeated interconnects caused by intra-die L_{eff} variation in 70nm CMOS using a supply voltage assignment technique.
- L_{eff} variation assumed as 28nm±16.7% (3σ tolerance)
- A Monte Carlo, normal distribution of L_{eff}'s was obtained using HSPICE driven by a Perl script, and a delay distribution was obtained with these L_{eff}'s. The supply voltages were assigned to reduce the delay distribution.
- Delay distribution was reduced 90% with a power overhead of 0.74%.





I. Benito, V. Venkatraman, W. Burleson, "Process Variation-Aware Vdd Assignment Technique for Repeated Interconnects", *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), 2006*.

Optimization Scenarios

- Bounds
- Constraints
- Pareto-optimality
- Compound measures
- Sensitivity to a computation parameter (ie wordlength, vector length, filter length)
- Sensitivity to a design parameter (ie pipeline depth, cache size, bus width)

Pareto optimality

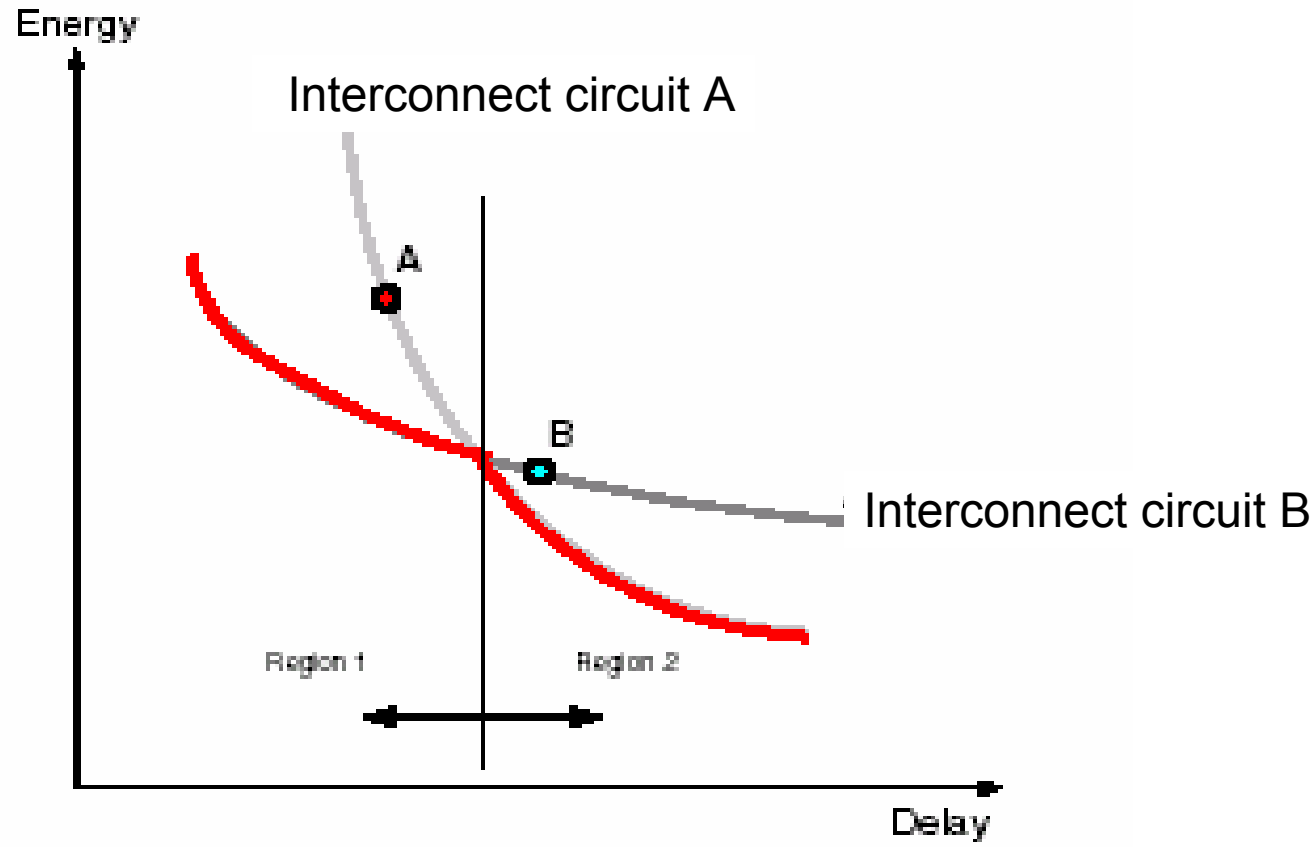


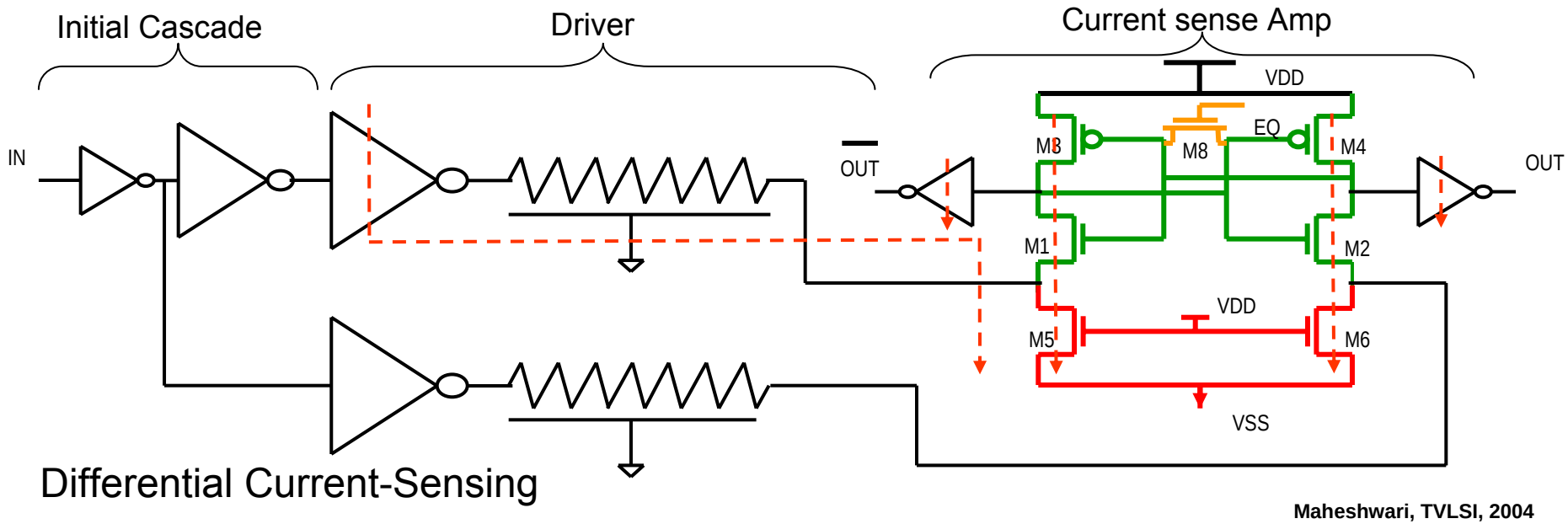
Fig. 3. Energy-Delay dependency

Compound metrics

- What makes sense?
  - Something you can bound: ie AT^2
  - Something physical: ie Power.Delay= Energy
  - Something you can advertise to a customer: MTBF, Availability, Battery Life,
  - Some design characteristic that implies performance like clock rate,
  - Something statistical/empirical that implies performance: ie IPC on SPEC
  - A hybrid: Instructions Before Failure (IBF), Instructions Before Failure per Watt (IBFPW)

Maximize: IPC/FIT/Energy/Time

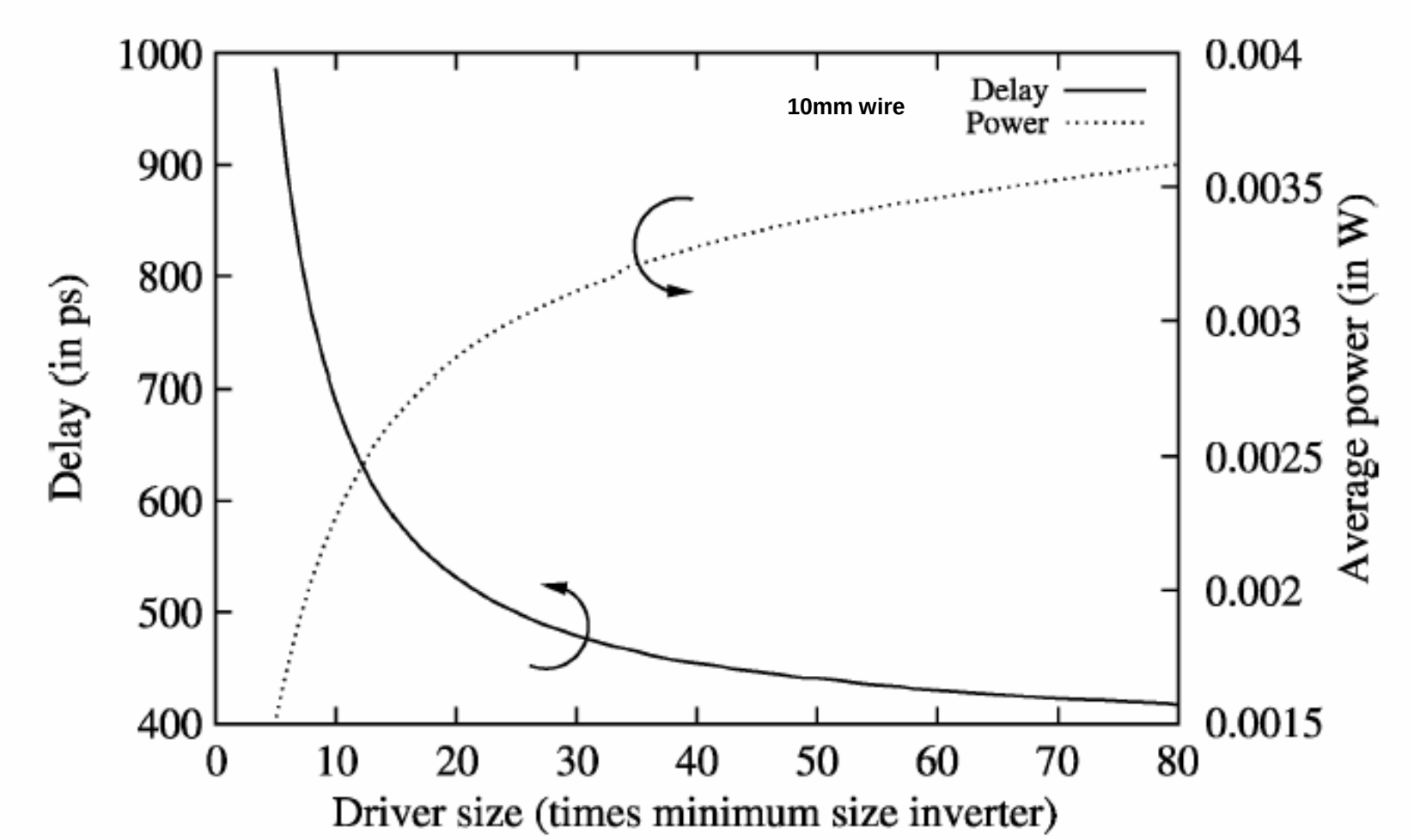
Interconnect Circuits – Low Swing



Maheshwari, TVLSI, 2004

- Current mode, Differential
- Avoids charging and discharging wire capacitance
- No repeaters along the wire: Avoids placement constraints
- Suffers from static power dissipation (paths shown by dashed lines)

Delay-Power tradeoffs

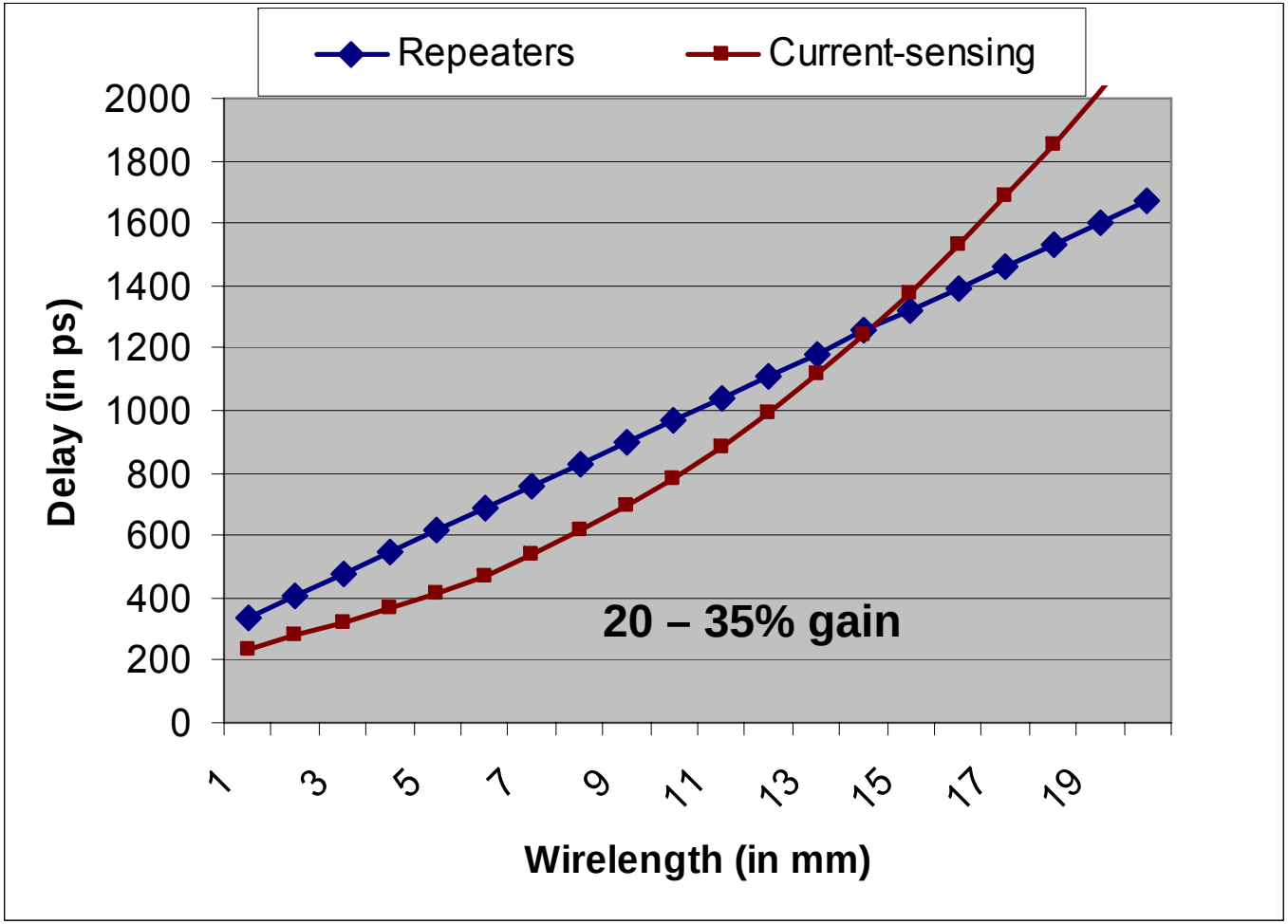


Differential Current-Sensing

Burleson, 2006

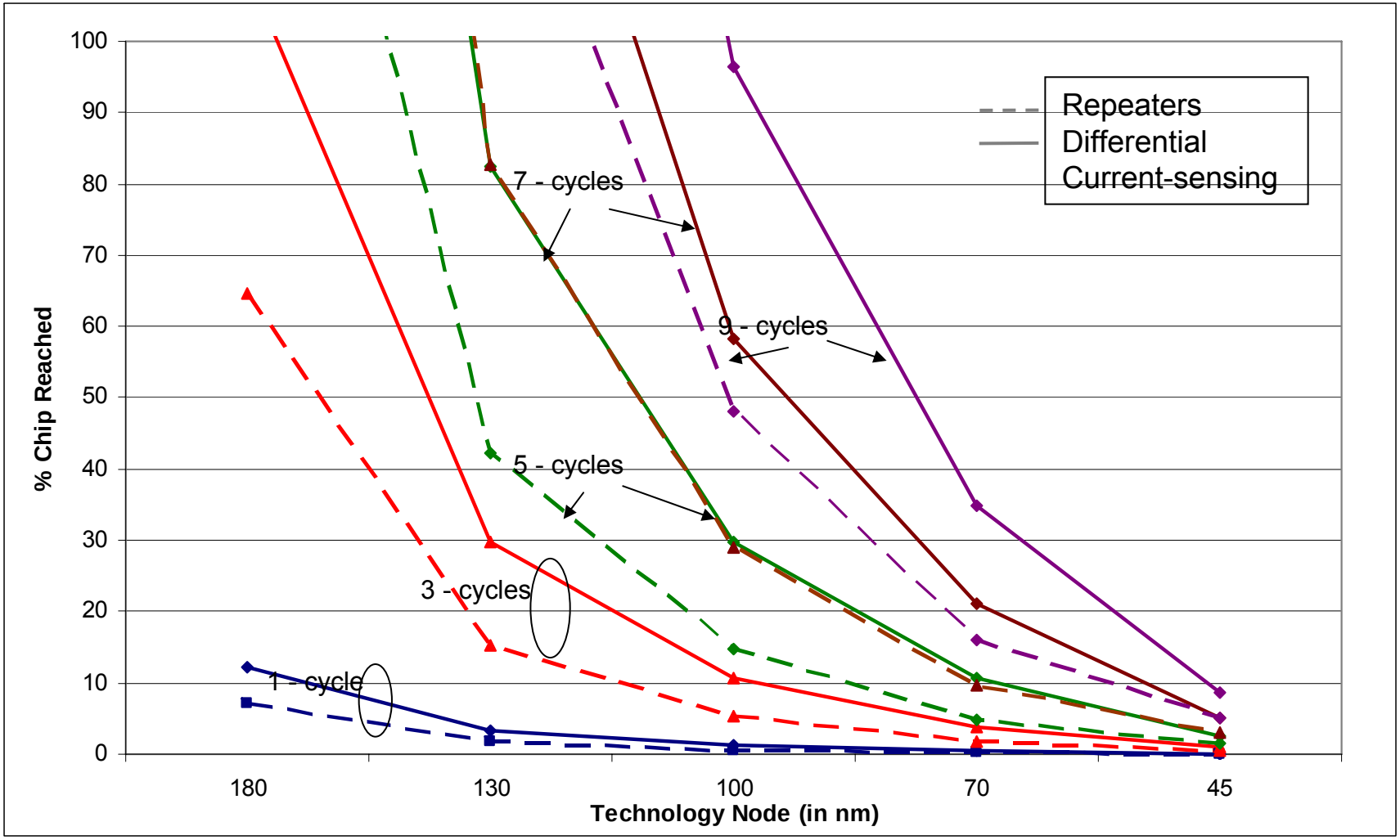
Maheshwari, TVLSI, 2004

Delay vs. wirelength



Intel 90nm (wires with 2x min. width)

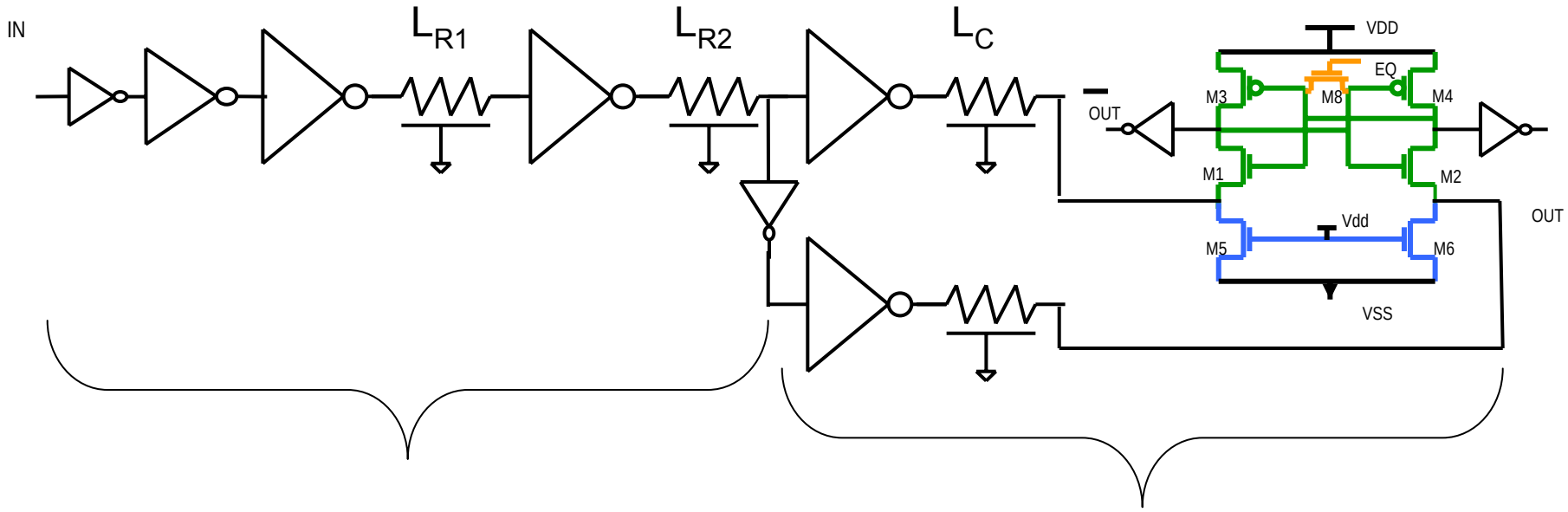
% chip coverage in n cycles



Percentage of Chip Coverage

Burleson, 2006

Hybrid Repeaters & Current-sensing



Uniform Repeater Insertion

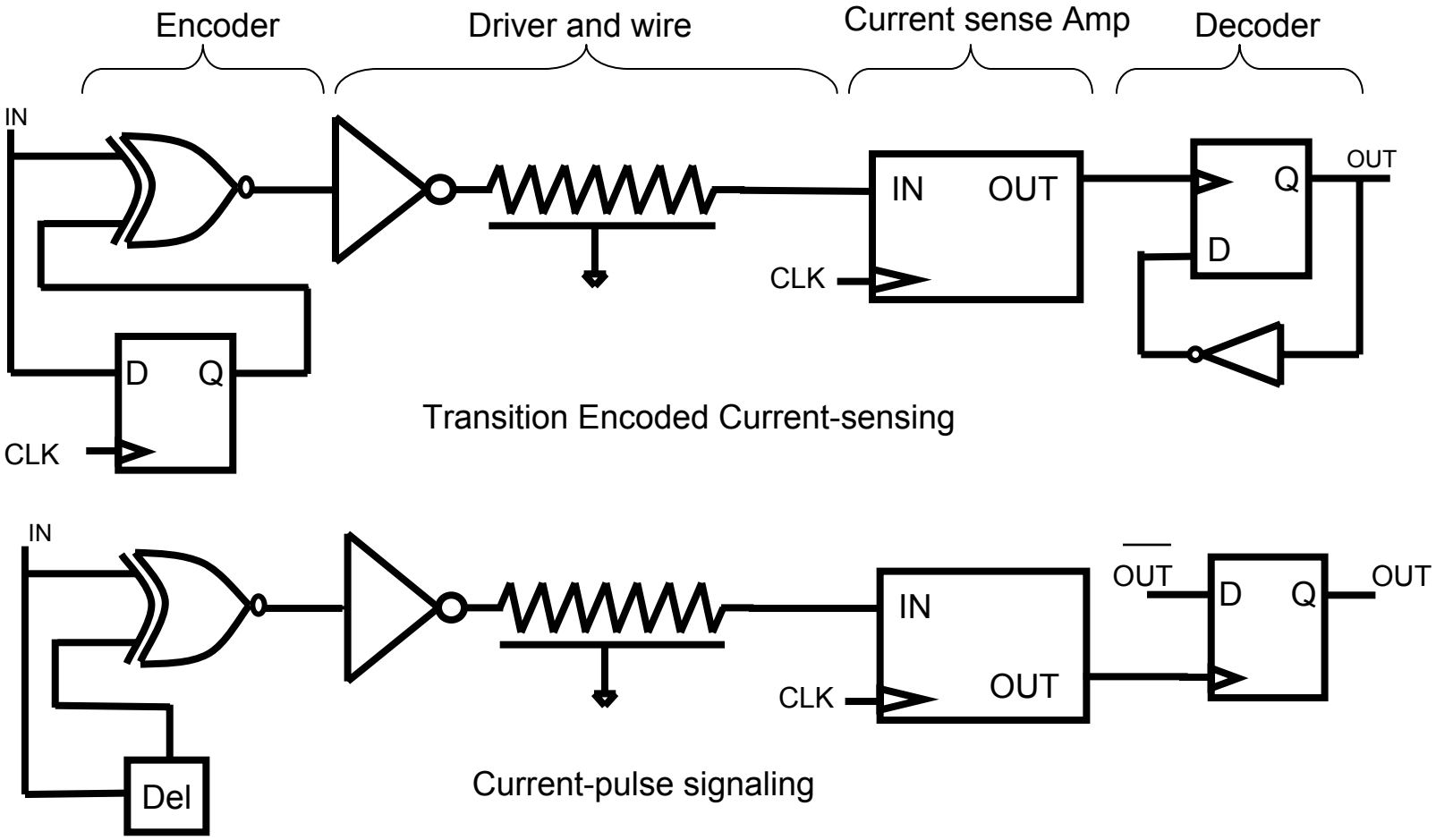
Current-sensing e.g. DCS

$$\sum_{i=1}^{n} L_{Ri} + L_C = L$$

$$\frac{\sum_{i=1}^{n} L_{Ri}}{L} = ?$$

How much wire driven by repeaters ?

Eliminating bus static power dissipation

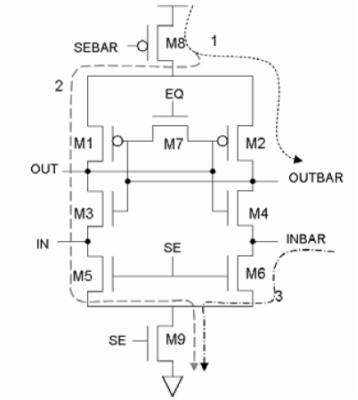


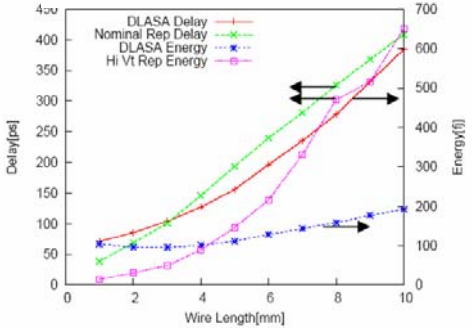
- Send current only when there is a transition
- Hold the bus at GND otherwise
- Encoder and decoder overhead

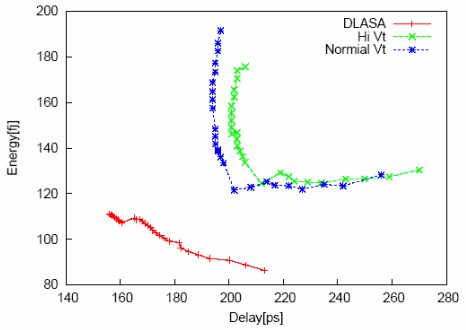
Energy-Aware Differential Current Sensing for Interconnects

S. Xu, V. Venkatraman, W. Burleson

- Problem:
  - Traditional Differential Current Sensing Circuit are good at speed, dynamic power and layout simplicity but leakage power is the bottleneck
    - Leakage become dominant(More than 50%) in the total energy consumption
  - Proposed an improved DCS circuit to optimize leakage energy while keep the merits in delay
  - Compared with repeater circuit
    - Results show advantage in speed and competitive in energy
- Uncertainty
  - Threshold Voltage (Vth) influence leakage current
  - Threshold voltage is largely related to process variation
    - Doping in the channel
    - Effective Channel length
    - Gate Oxide thickness
- Methodology: Varying the wire length and driver size and process variation in HSPICE using perl script. Retrieve result with perl.
- Results:
  - 58.1% less leakage than high threshold voltage repeater in 5mm interconnect
  - Up to 20% faster than repeater







References:

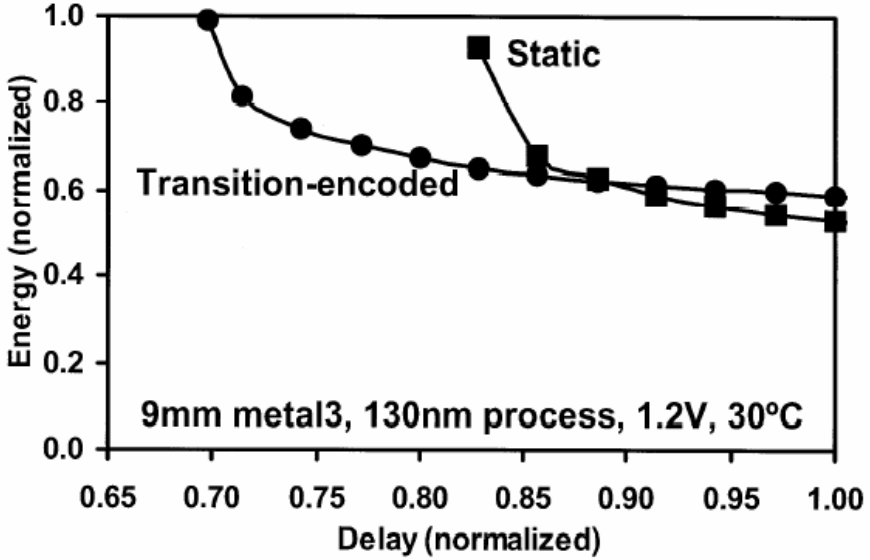
A. Maheshwari, W. Burleson IEEE Transactions on VLSI Systems 2004

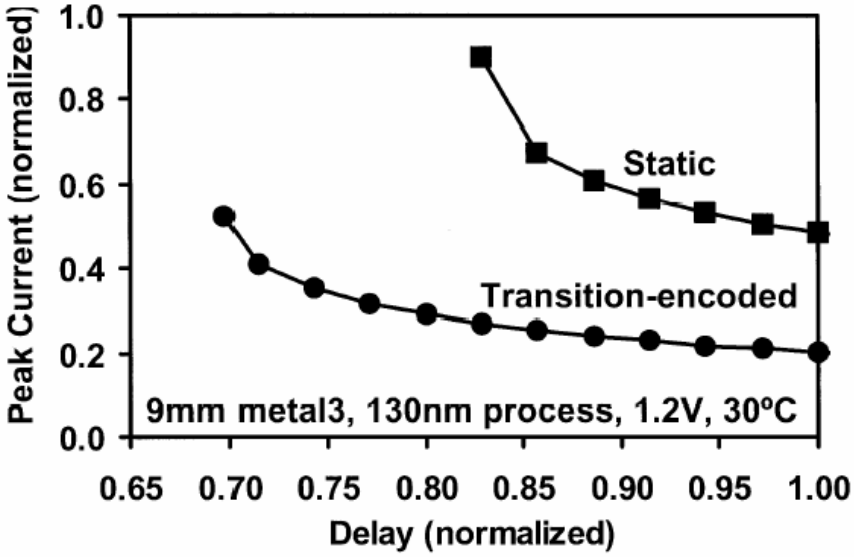
S. Xu, V. Venkatraman, W. Burleson MWSCAS 2006

Interconnect Solutions - Bus Encoding

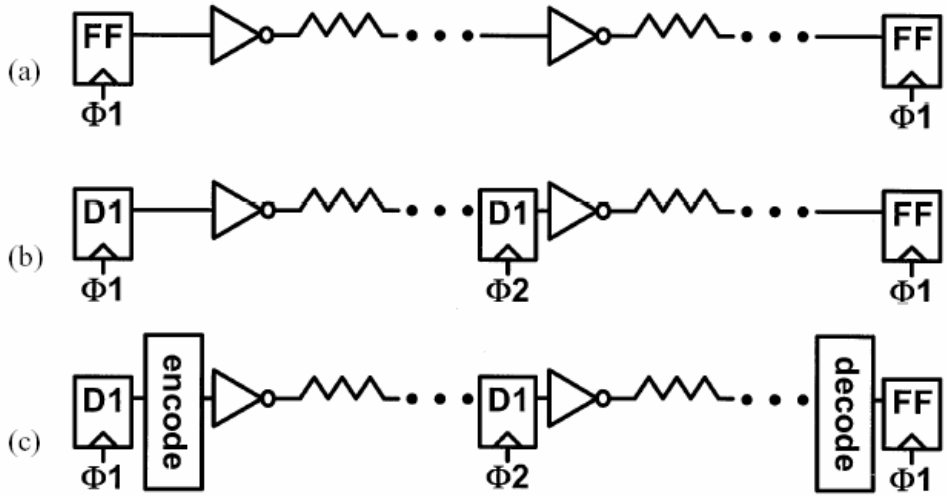
- Reduce dynamic power due to switching activity on a bus
  - Transition encoding, spatial encoding, invert encoding, pattern encoding
- Various encodings target different aspect of interconnect
  - Delay, power, energy, crosstalk, area
- Cost of encoding/decoding
  - Power, area, latency, additional wires

Interconnect Solutions – Bus encoding





- Uses a dynamic bus configuration
- Encoder translates input transition activity into an output logic state
- Decoder uses encoded signal to reconstruct the original input using its stored state information to distinguish between the two input transitions.



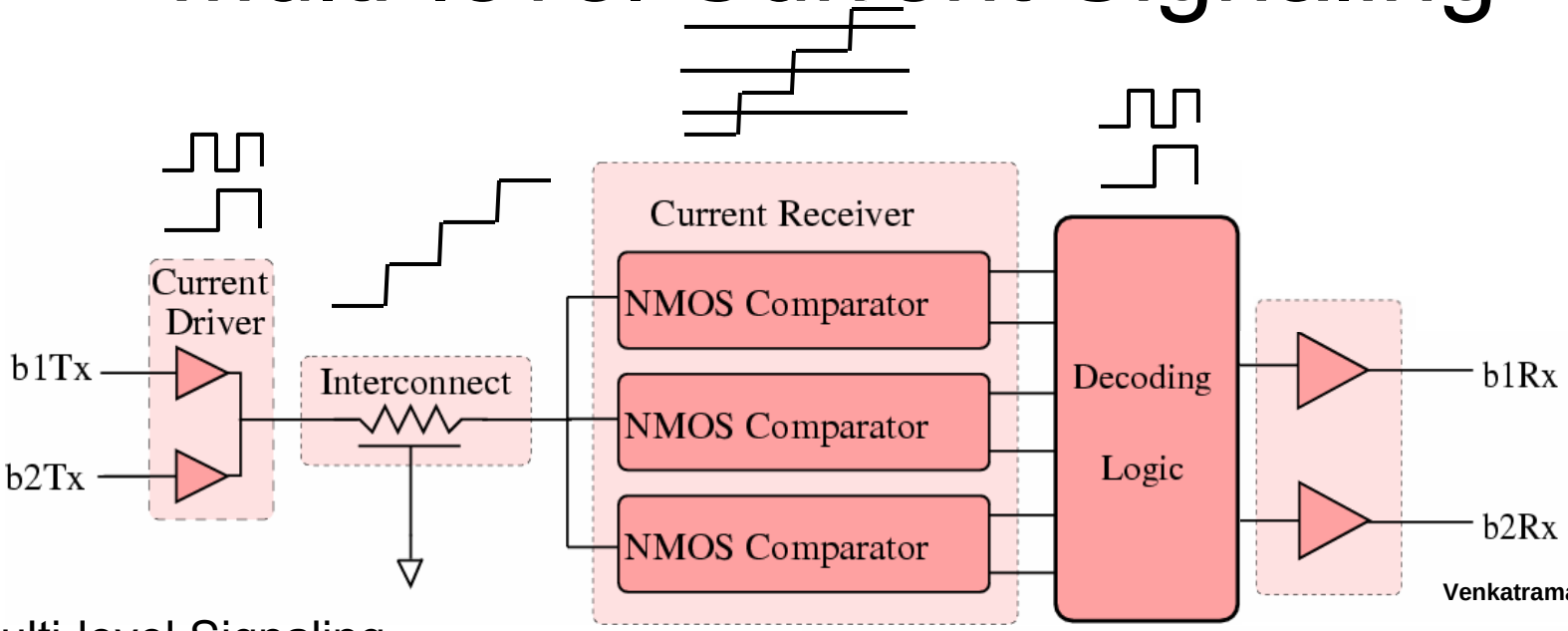
Transition Encoded Dynamic Bus Anders, JSSC, 2003

Interconnect Solutions - Bus Encoding

- Bus invert encoding
  - Checks each cycle if there is a possibility of greater than 50% transitions on the bus
  - Decides whether sending the true or compliment form of the signals
  - Reduces the switching activity
  - Requires one additional wire to inform receiver whether the bus is true or complement
  - Numerous extensions and improvements for different statistical assumptions and metrics

Stan/Burleson, TLVSI, 1997

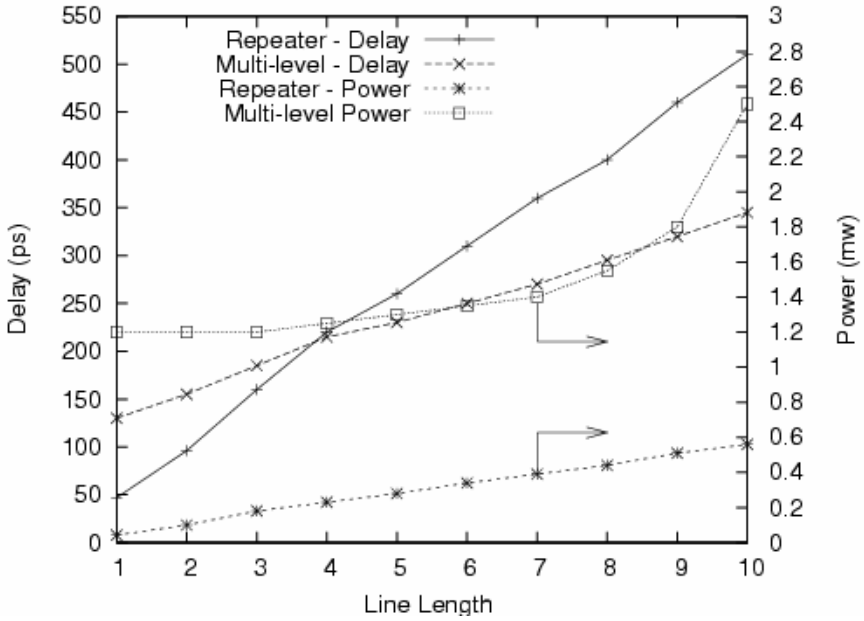
Multi-level Current Signaling



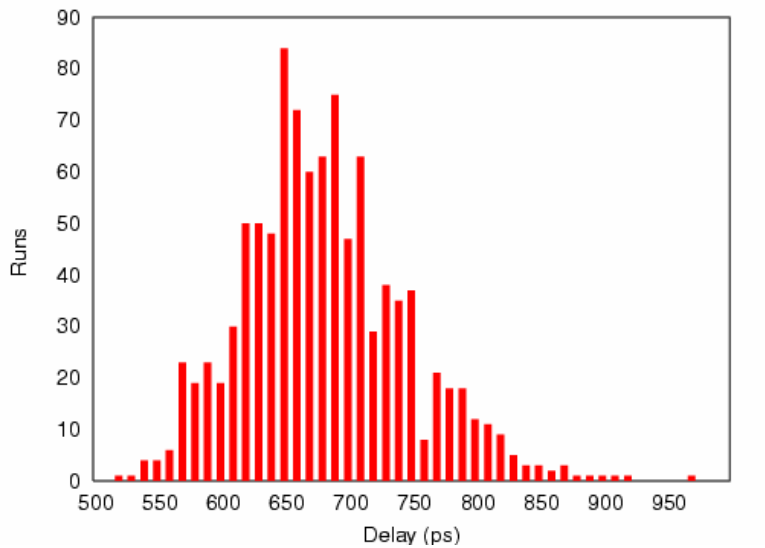
Venkatraman, ISQED, 2005

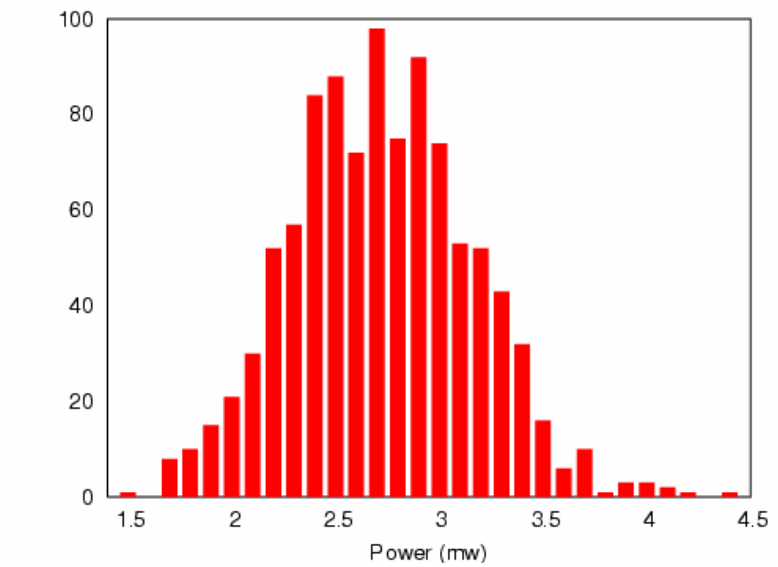
Multi-level Signaling

- Encode two or more data bits and transmit on interconnect.
- The two or more data bits are encoded into four or more current levels. Current provides more head-room than voltage!
- Sense the current levels and decode the original signals



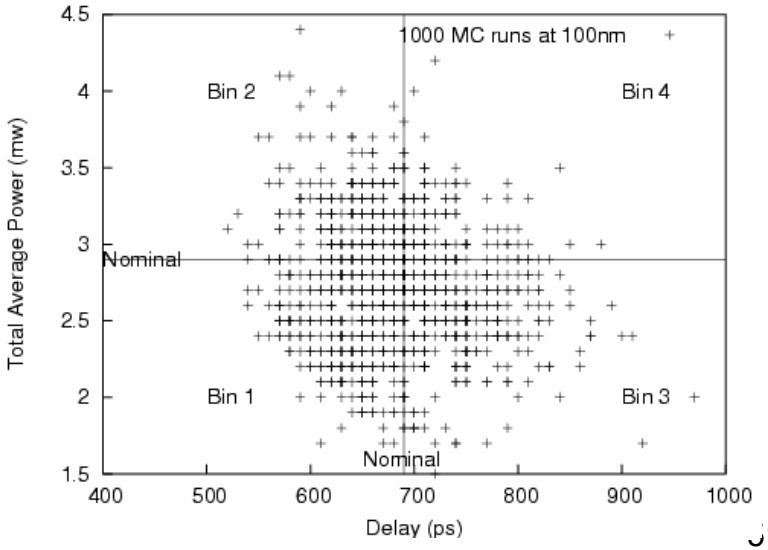
Impact of Uncertainty on Delay and Power



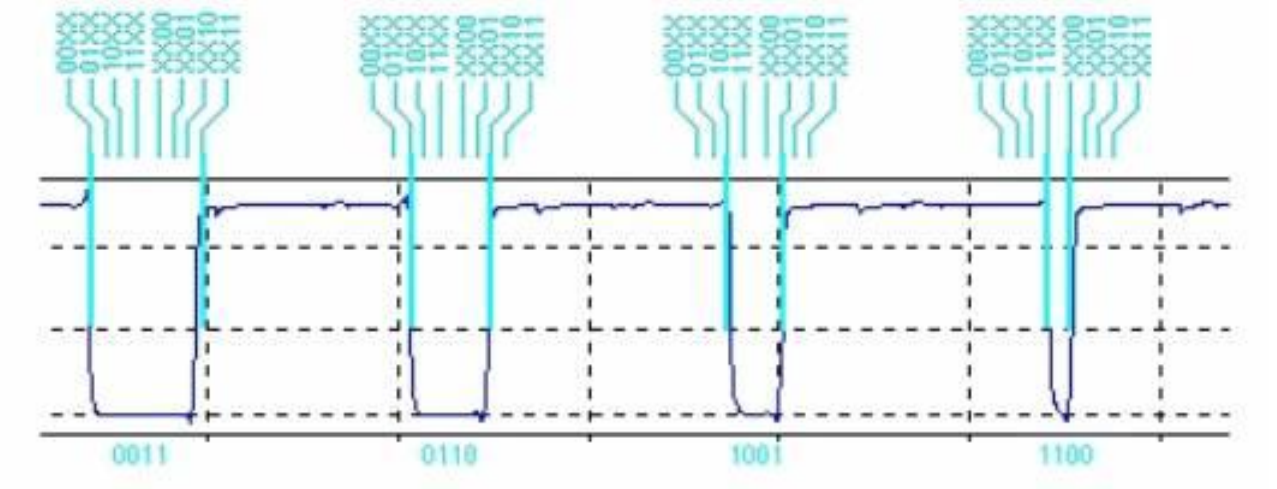


- 100nm technology
- 1000 Monte Carlo Runs
- Power variability of 43.64%
- Delay variability of 28.95%

- 100nm Technology
- Bin 1(High Performance) Yield – 36.1%
- Bin 2(Low Delay) Yield – 27.3%
- Bin 3(Low Power) Yield – 25.1%
- Bin 4(Low Performance) Yield – 11.5%

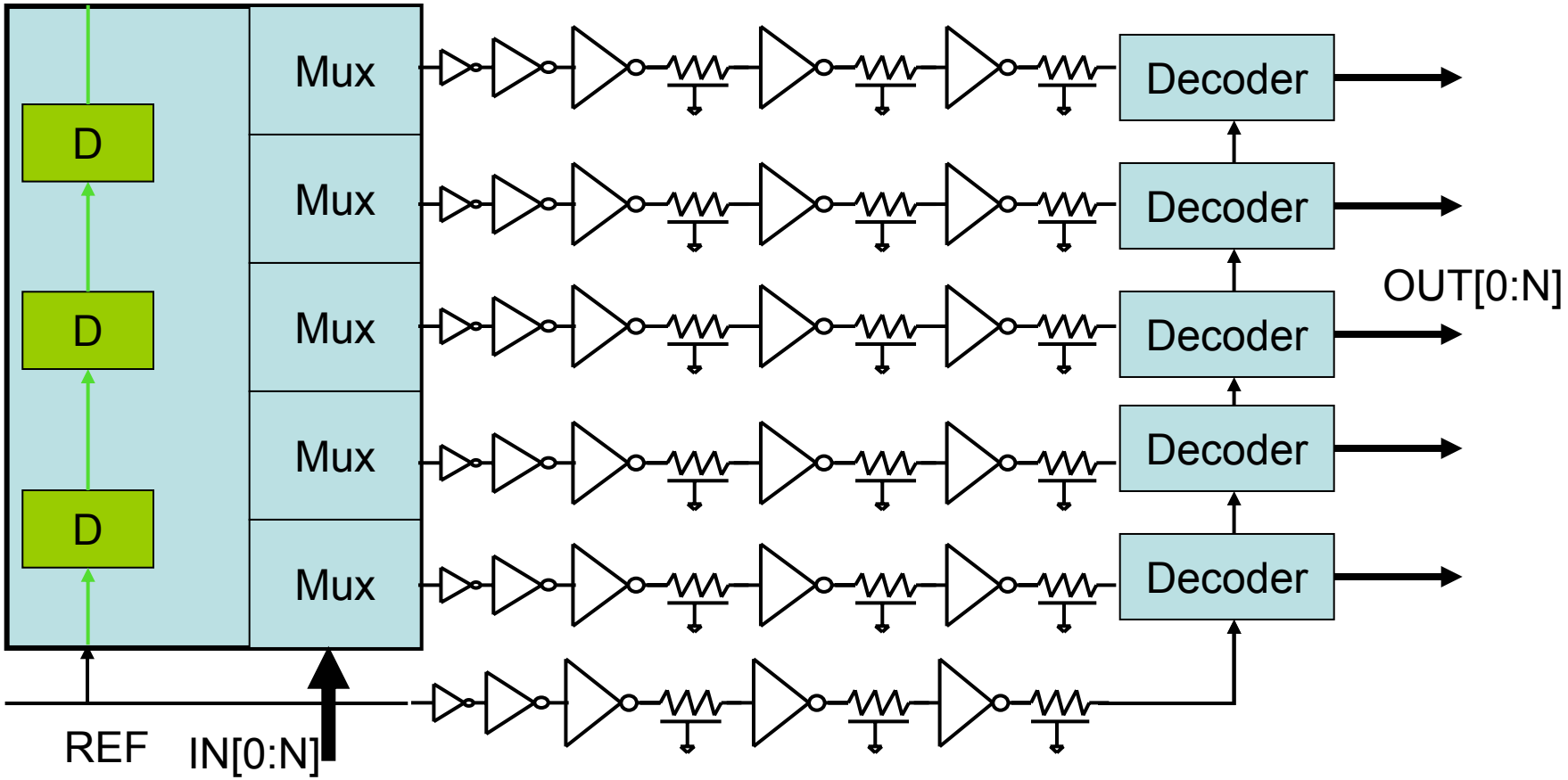


Phase Coding



- Actually phase modulation
- Transmitting multiple bits in one transition
  - Significant power and area savings
  - Increased bandwidth
- Phase coding – Phase determines the data
- How to deal with timing uncertainty?

Open Loop Phase Coding



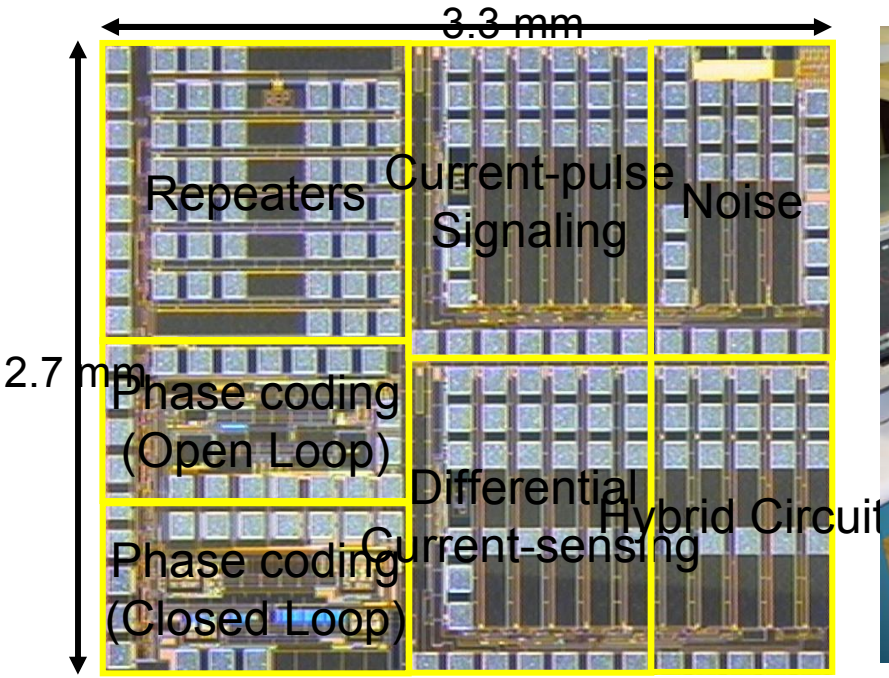
- Delay elements can be shared across wires
- Supply noise, Process variation etc. can result in errors

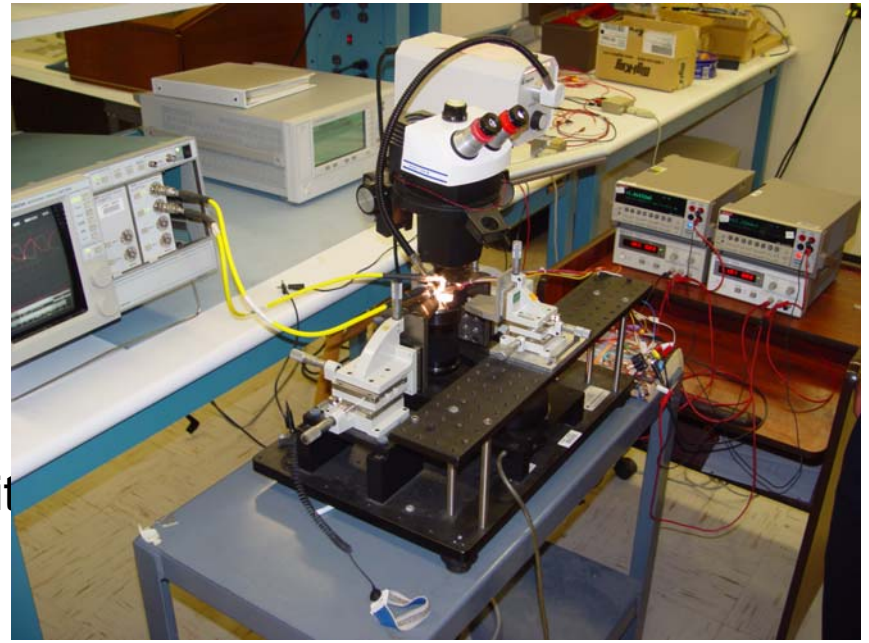
Measured Results: Closed Loop

- 16-bit 5mm long bus, 0.27u wide, 0.27u spacing, shielded, 1GHz
- Repeater insertion, Transition encoding used
- Encode in ½ cycle and use ½ cycle for decode

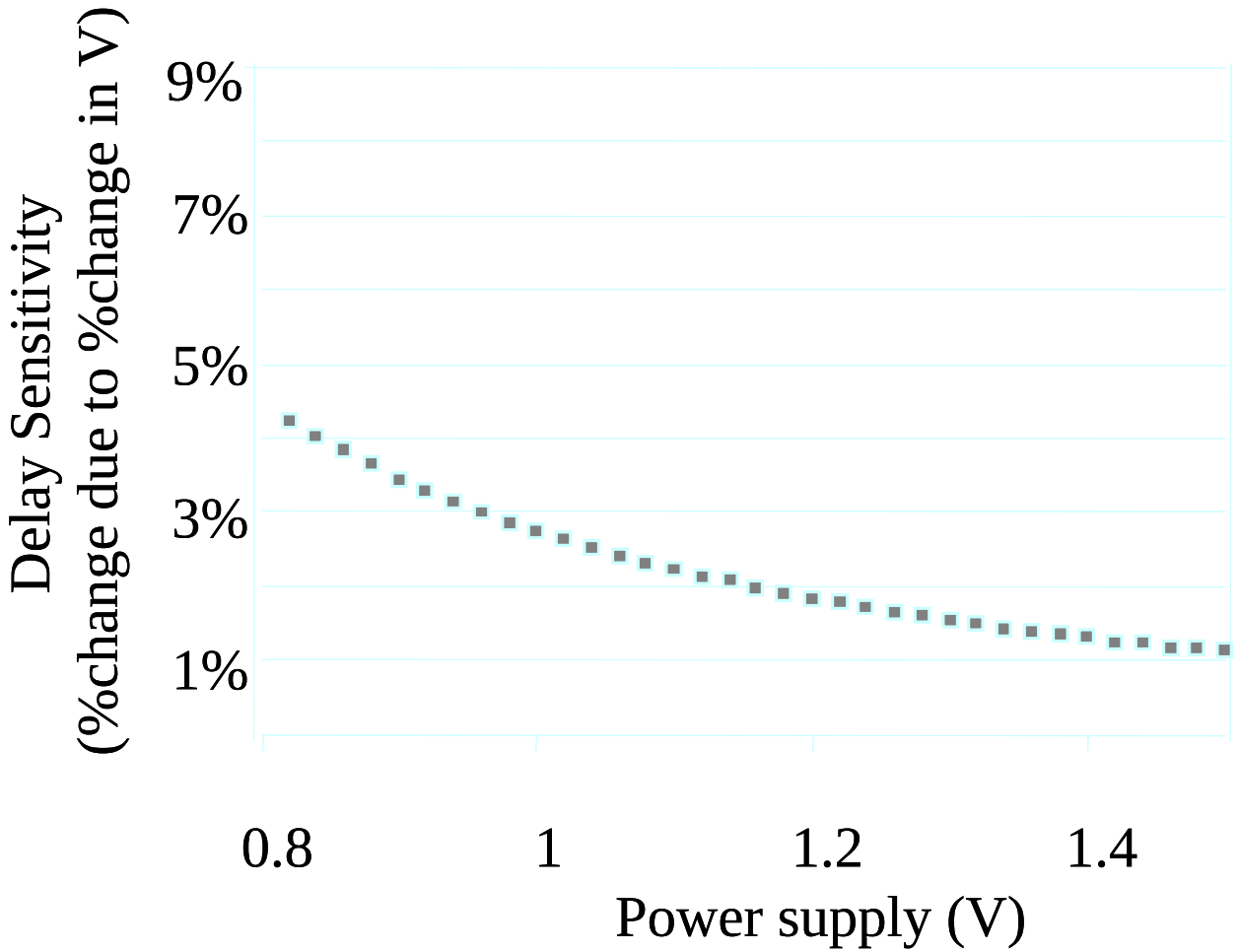
Encoding Levels (bits/wire)	Encoder Overhead (mW)	Decoder Overhead (mW)	Phase coding power (mW)	Repeater bus (mW)
2	0.33	1.00	5.61	8.56
3	0.47	1.33	5.01	8.56
4	0.62	1.52	4.28	8.56

Interconnect test chips



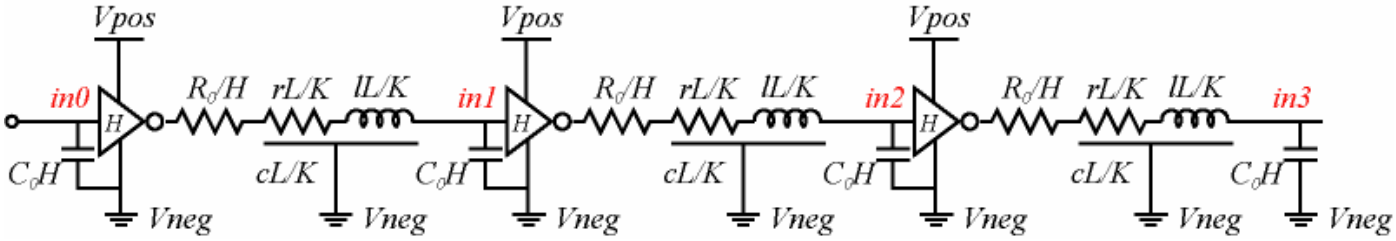


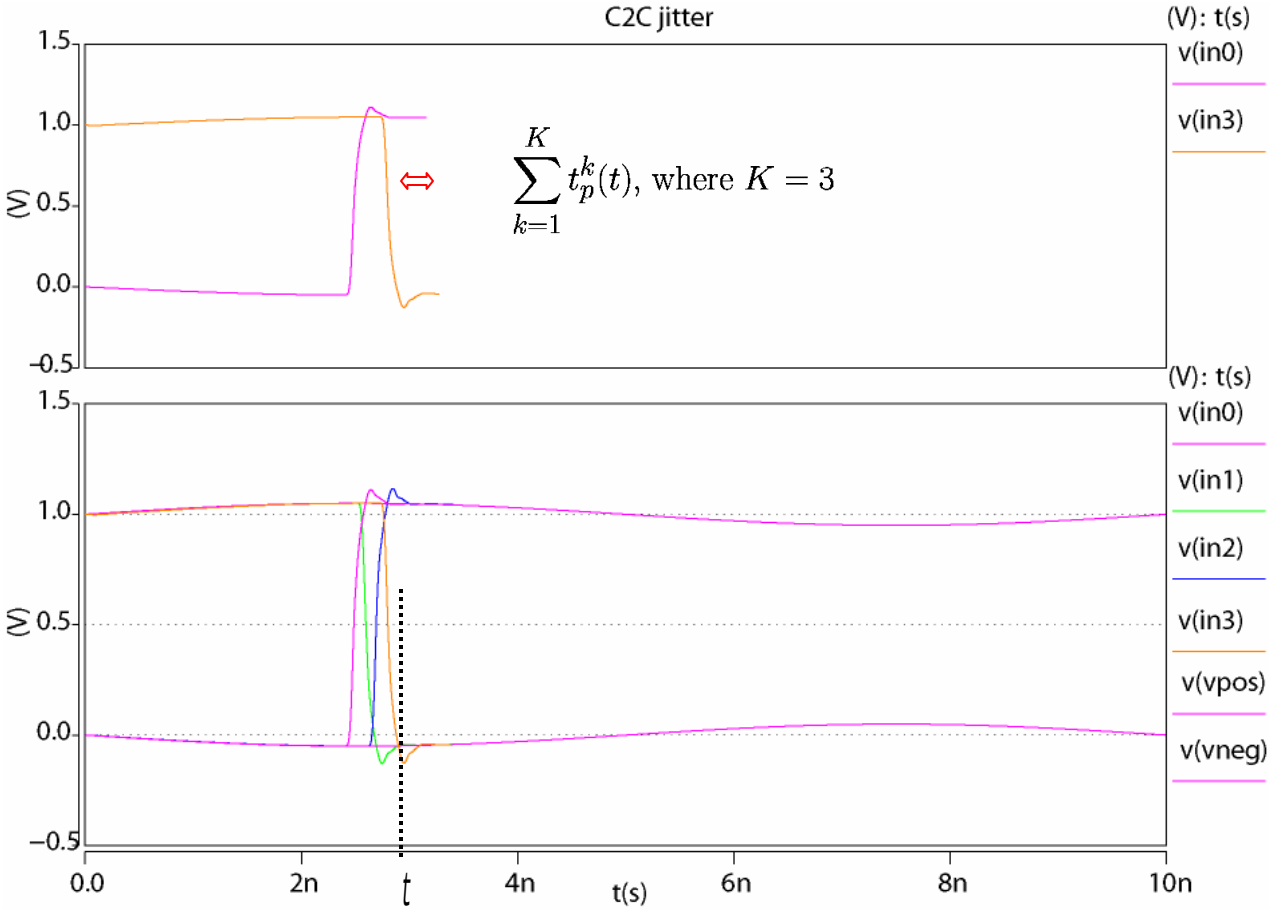
How sensitive is gate delay to V_{dd}?



Kundu 2004

Sinusoidal Supply Noise cycle-to-cycle jitter





Jang, Xu, Burleson
ISVLSI, 2005

Supply Noise models

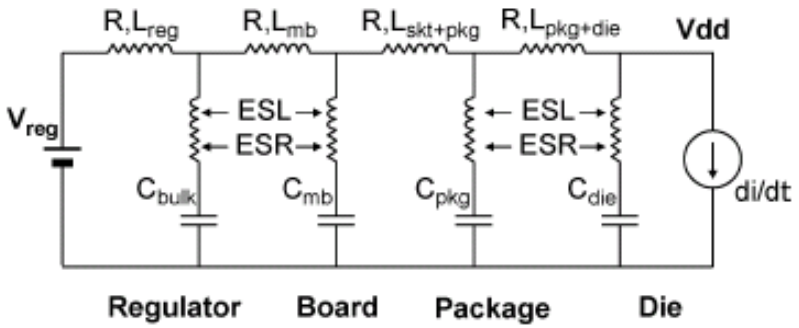


Fig. 1. Power delivery system with multiple stages.

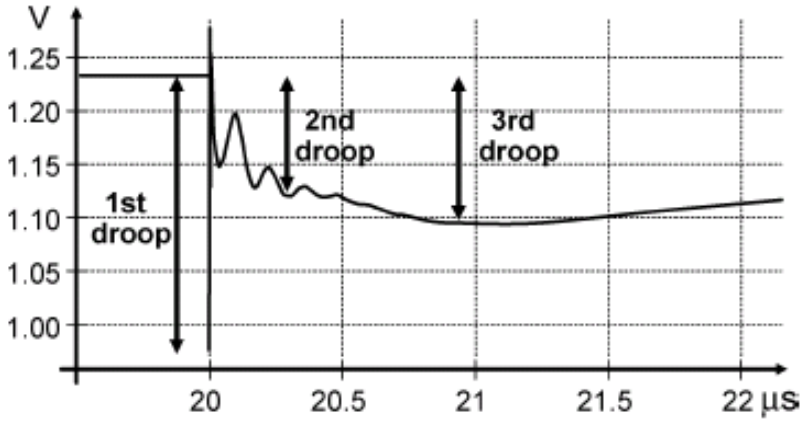
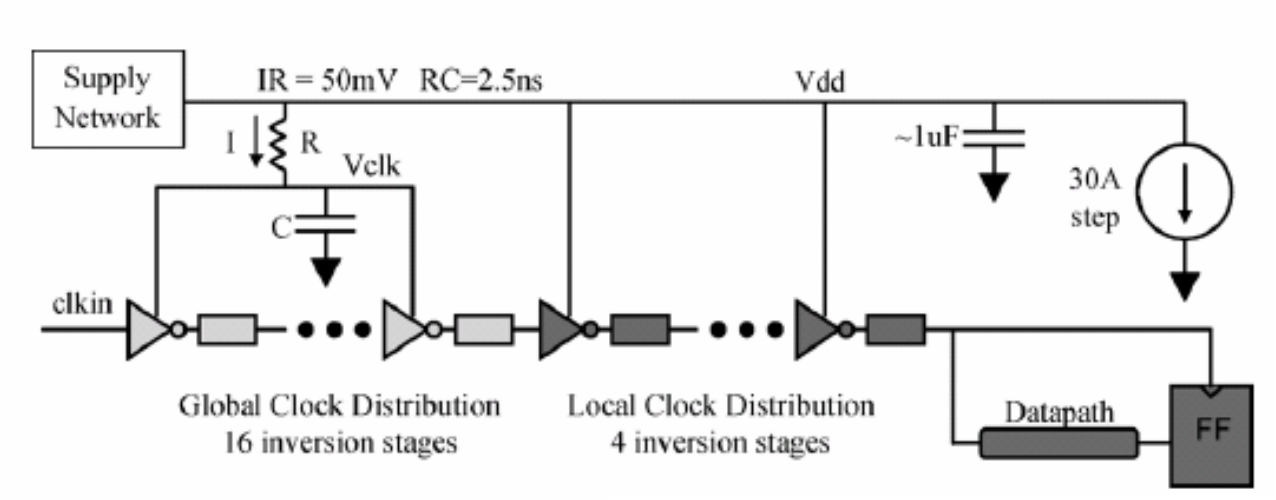


Fig. 2. Simulated voltage droops.

How large a problem is this?

Technology (nm)	1st Droop	2nd Droop	3rd Droop
250	9%	6%	0.50%
180	12%	7%	0.80%
130	17%	8%	1.20%
90	22%	9%	2.50%
65	27%	10%	4%
45	29%	14%	6%

Adaptive Clocking



Enhancing Microprocessor Immunity to Power Supply Noise With Clock-Data Compensation
Wong, Rahal-Arabi, Ma, Taylor, (Intel)
IEEE JSSC, April 2006

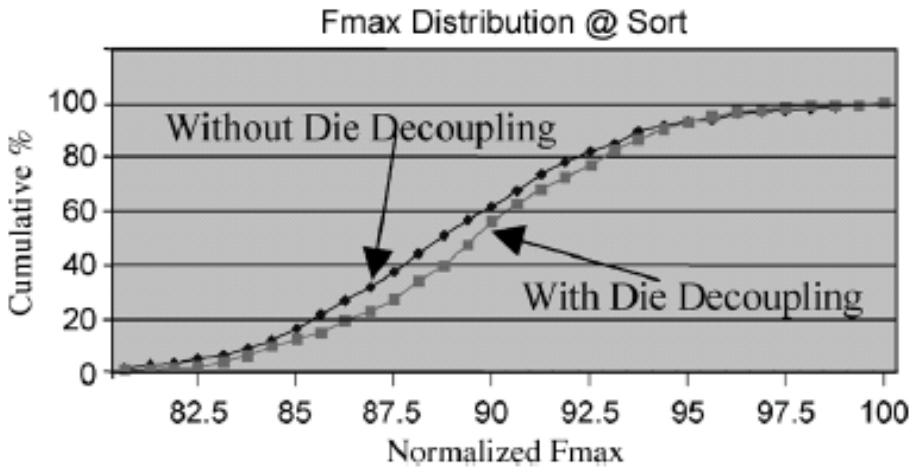
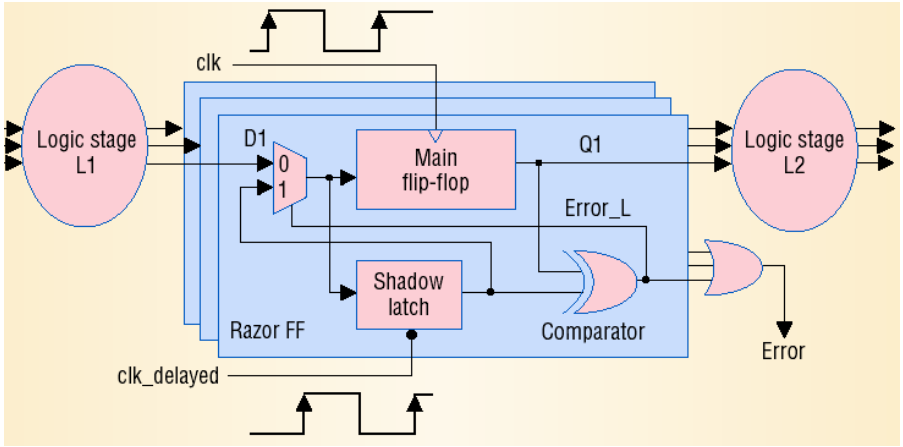
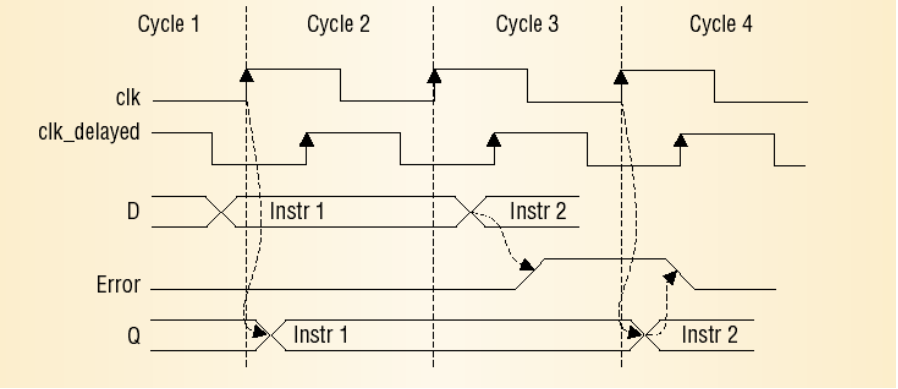


Fig. 22. Average frequency shift for a stepping of the Pentium 4 processor due to on-die capacitance removal.

Uncertainty – Variation-tolerant Design

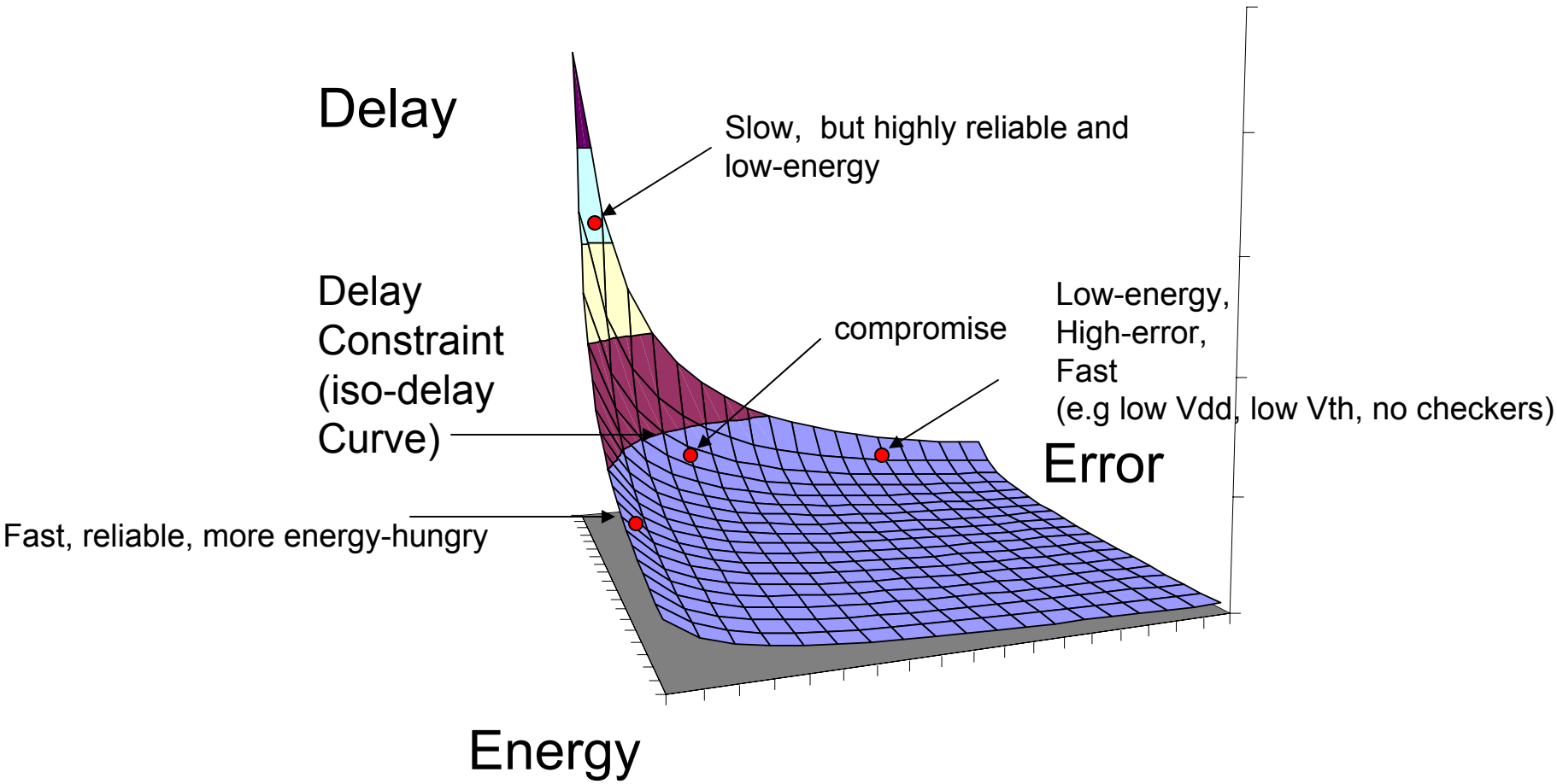




- Razor methodology
  - A voltage-scaling methodology based on real-time detection and correction of circuit timing errors
  - Allows for energy tuning of microprocessor pipeline
  - Application or Razor methodology results in up to 64% energy savings with less than 3% delay penalty for error recovery

Austin, Computer Magazine, 2004

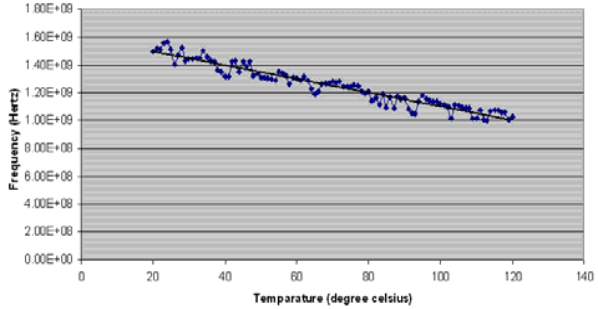
The Delay, Energy, Error space

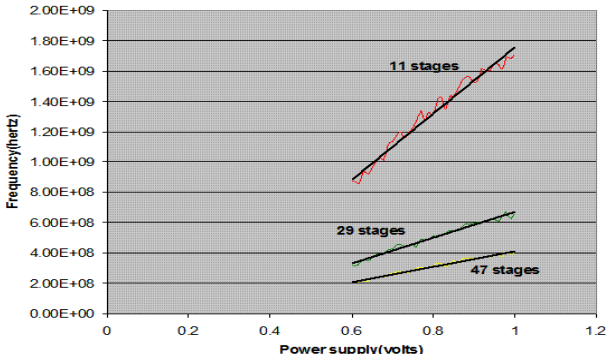


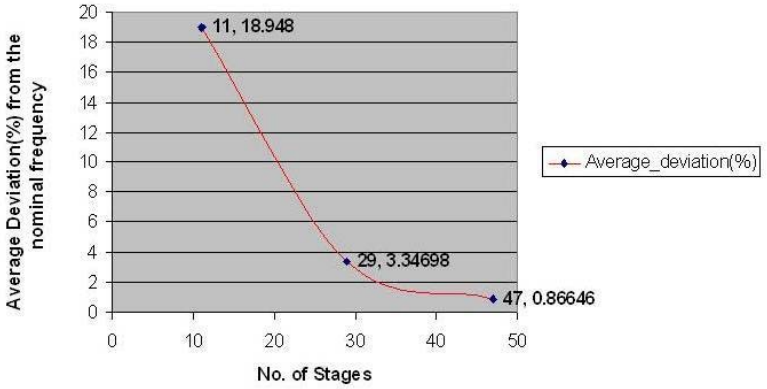
Burleson, BARC 2005

Thermal Sensing using Oscillators
Kumar, Datta, Burleson

- Study of **Ring Oscillator as a thermal sensor** in **65nm** technology-Dependence of oscillation frequency on temperature, power supply sensitivity, process variation sensitivity
- Ways to mitigate sensitivity to power supply noise, process variations – Device sizing, Increasing stages.
- Analysis performed by simulating an 11-stage ring oscillator in **HSPICE** and using Berkeley Predictive Model Technology files. To model effect of process variations, Monte Carlo analysis was performed in SPICE over a Gaussian distribution of process parameters.

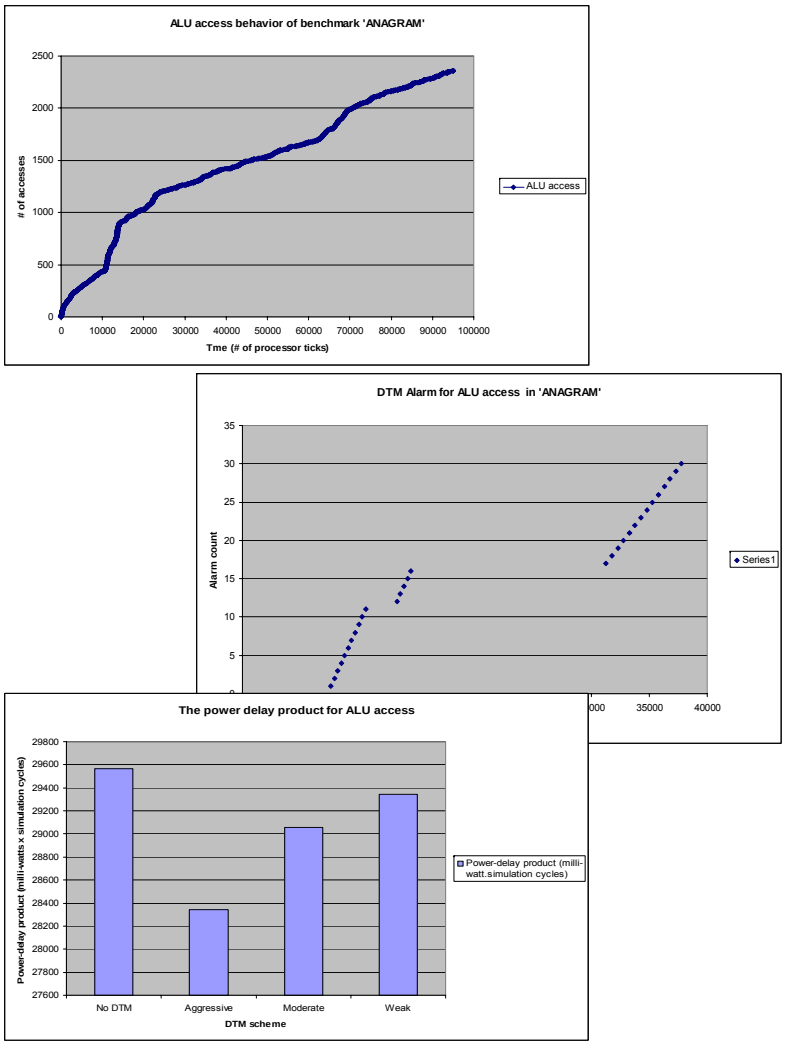






Run-time program statistics for thermal management

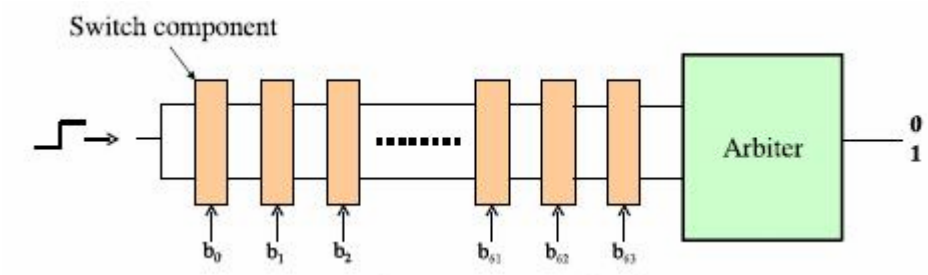
- Abstract temperature sensors with hardware access counters, monitor **access behavior** of resource units to predict imminent thermal risks
- Compute **run-time slope** of resource access – metric to determine "power/thermal risk potential" of thread in execution. At points of dangerously high unit access, alarm set off, stalling periods inserted
- For standard benchmark binaries, experimental results indicate significant Power-Delay-Product benefit. **HOTSPOT** results indicate thermal benefits and validate approach.
- **SIMPLESCALAR** used as the main architectural simulator, **WATTCH** (architectural level power simulator) code modified to integrate resource counters and a controlling monitor that implement an access –based DTM. Resultant power values ported to HOTSPOT to generate thermal profile of the architecture simulated

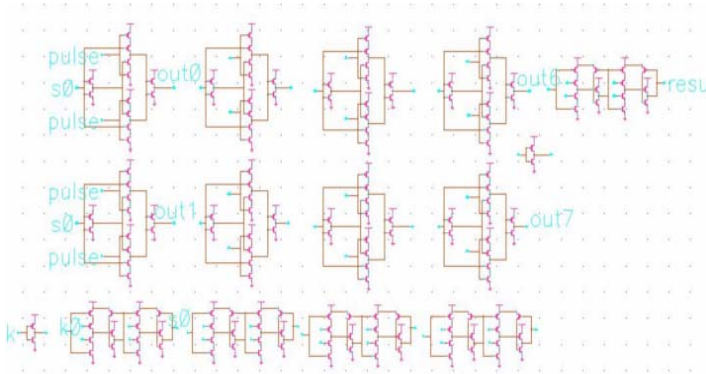


Impact of Soft Errors on the Physically Unclonable Function (PUF) circuit,

Holcomb, Lapointe, Burleson (UMASS)

- **Scenario** PUF circuits are designed such that the output depends on process variation. In this study, we evaluate how frequently particle strikes cause incorrect evaluation of a 4-bit arbiter based PUF circuit. We add process variation to the circuit and then analyze the FIT rate (failures in time, per 10^9 hrs) of it. The simplifying assumption is made that the variation is not spatially correlated.

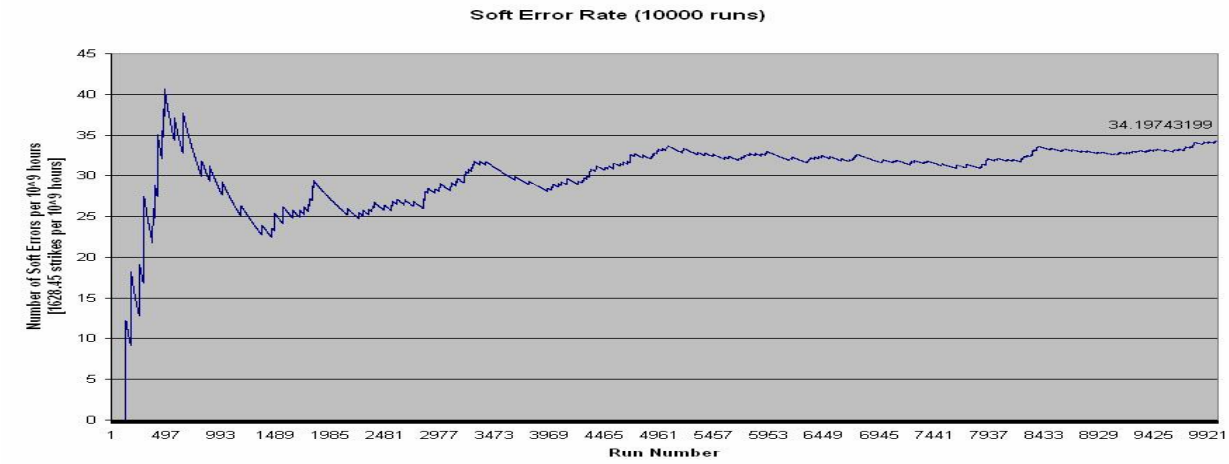




- **Sources of uncertainty:** The primary source of uncertainty is variation in transistor lengths and widths. The variations were modeled by replacing each nominal transistor dimension by a random size that is between 75% and 125% of nominal sizing. The secondary source of uncertainty is the location, and timing of particle strikes. The location of particle strikes is based on transistor sizing. Because the collection probability of a node is physically proportional to the diffusion area, we strike nodes with relative frequencies that are proportional to transistor widths. The distribution of the particle strike times is uniform over the clock cycle.

Soft-errors on PUF (continued)

- **Methodology:** The Monte Carlo variations were implemented using PERL, as was the parsing of the PUF circuit netlist to derive a list of nodes that could be struck and their relative probabilities of being struck. The circuit simulations were completed using PERL driving HSPICE in 130nm CMOS.
- **Results** The result for this particular PUF circuit was a FIT rate of 34.20 failures per 10^9 hrs. The plot below shows the convergence to this FIT rate over the course of 10000 simulations.



- **Reference** PUF circuit, Devadas et al,(MIT), ISCA05

Synchrotokens: A Deterministic Globally Asynchronous Locally Synchronous (GALS) Methodology for Validation, Debug, and Test

Heath, Burleson, Harris (UMASS, UCI)

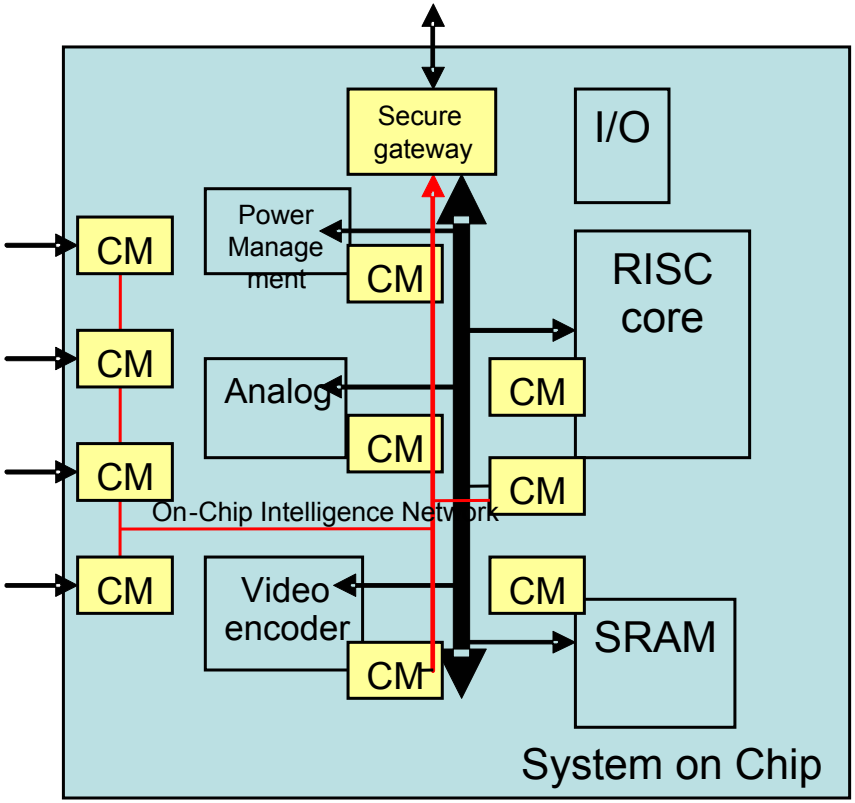
IEEE Trans Computers, Dec 2005

- GALS is a natural clocking methodology for SoC's
- Typical GALS designs are nondeterministic because asynchronous signals unpredictably transition before or after the sampling clock edge
- A nondeterministic implementation which conforms to a higher-level specification is functionally correct
- Nondeterminism makes validation, debug, and test harder because the expected response is not unique
- Synchro-tokens eliminates nondeterminism by adding control logic to the interface of synchronous blocks so that asynchronous input transitions are captured on deterministic local clock cycles
- Key components of synchro-tokens architecture:
  - Token ring nodes, hold counters, and recycle counters control when tokens are received and sent
  - Stoppable clocks ensure tokens are received on deterministic clock cycles
  - FIFO interfaces ensure deterministic data accompanies the token

On-Chip Security

(Burleson, Tessier, Gong, Wolf, Gogniat (France))

- Architectural support to **monitor** on-chip statistics and provide early defenses against attacks
  - Why hardware?
    - Low overhead (performance, power)
    - More rapid response
    - More secure than SW or OS
- What's hard?
  - Modeling proper vs. attacked behavior (easier for embedded systems)
  - What to monitor?
    - Digital data on buses (traces)
    - Current, voltage, temperature?
  - Real-time correlations/statistics
  - Fusion of monitor results to:
    - Detect real attacks
    - Reject false alarms



CM = Configurable Monitor
OCIN = On-Chip Intelligence Network

Dynamic Tradeoffs for System Adaptation/Reconfiguration

- Why?
  - Workload
  - Power source (battery health, lifetime, scavenging)
  - Thermal situation (cooling system)
  - Application Criticality
  - Security
- What is needed?
  - Degrees of freedom at circuit, logic and architectural levels (process is fixed…)
  - Policy for adjusting parameters to satisfy changing optimization scenarios
  - Capability of predicting changing scenarios

Dynamic Tradeoffs come at what cost?

- Additional and generalized resources
- Reconfiguration overhead (delay,power)
- Control algorithm (stability?)
- Design complexity
- Characterization
- Vulnerability?

Examples of run-time flexibility

- Circuit/Logic level
  - Variable Vdd/clock
  - Droop detection and mitigation
  - Body-bias
  - Enabling parity/ECC for detecting/correcting
  - Switchable capacitance (high overhead)
  - Sleep/nap modes
- Architectural level
  - Redundant multithreading, etc.
  - Instruction issue/scheduling
  - Cache scrubbing, etc.
  - RTOS task scheduling, etc.

Review of Outline

- My Perspective: VLSI Circuits and Architectures
- Motivations: Interconnects
- Why Statistics? Sources of Uncertainty, Metrics, Time Scales, Estimation
- Optimization Scenarios: Bounds, Constraints, Tradeoffs, Pareto-optimality
- Some Recent Work
- Dynamic Tradeoffs?
- Open Problems

Open Problems

- Statistical estimation tools
- Run-time monitoring as a method for improving statistical models
- Dynamic tradeoffs based on run-time statistics
- Coping with non-determinism at the system level (do we really want *better than worst-case design* if we can't predict how much better it is?)

Conclusions & Challenges

- Interconnects are a critical enabling abstraction in MPSoC
- Interconnects play a very large and increasing role in delay, energy, and design effort.
- Statistical approaches are needed to cope with the uncertainties arising in semiconductor technology as well as architectures and application workloads.
- Tradeoffs between statistical metrics are key to future design approaches. Run-time tradeoffs are promising but challenging.
- CAD support needed, especially
  - early estimation for architecture and floorplanning
  - final verification in the presence of uncertainties

VLSI Interconnects: A Design Perspective,

W. Burleson (UMass) and A. Maheshwari (Intel)

Morgan-Kaufmann. 2006-7

Coming Soon!

- 400-page textbook with HW problems, covering:
  - History (both off-chip and on-chip)
  - Process (metallization, dielectrics, etc.)
  - Architecture (processor, ASIC, FPGA, memory)
  - Theoretical models (graph, information-theoretic)
  - Wire models (R,C,L,M,…)
  - Statistical Approaches
  - Circuits (repeaters, boosters, sense-amps, etc.)
  - CAD (estimation, synthesis, optimization)
  - Case Studies (buses, memories, ASIC, FPGA)
  - Future (nano, optical, wireless, etc.)