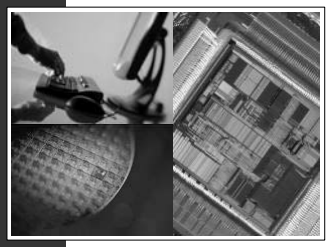
From Tape-out to the Fab

Dr. Raul Camposano
Chief Technology Officer, and
General Manager, Silicon Engineering Group



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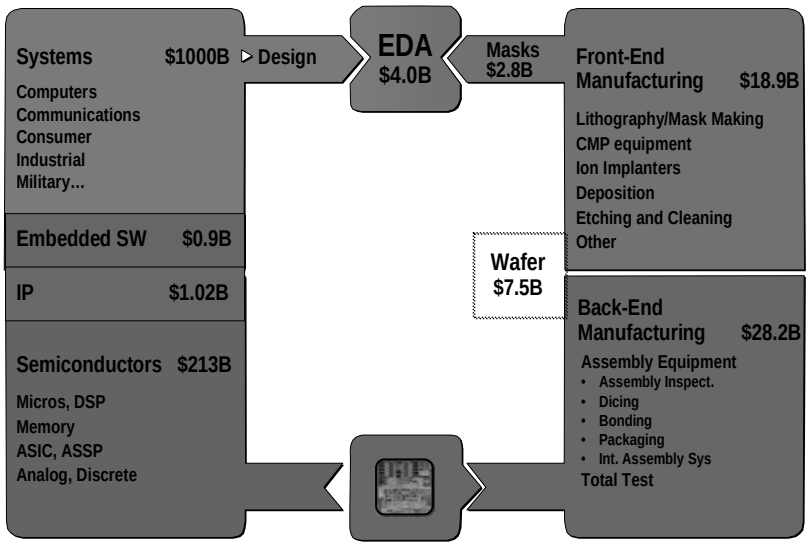
Semi Market



Market size for 2005 Sources: IC Insights 2005, Dataquest 2004, Synopsys Estimates

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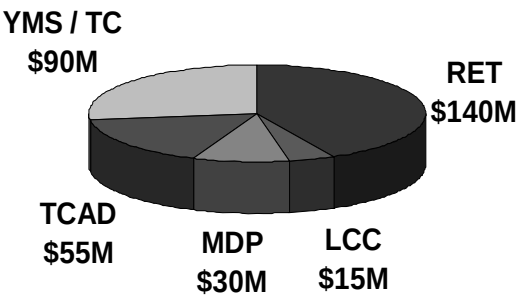
Specific “DFM” SW Markets

DFM

Manufacturing



Source: Internal estimates

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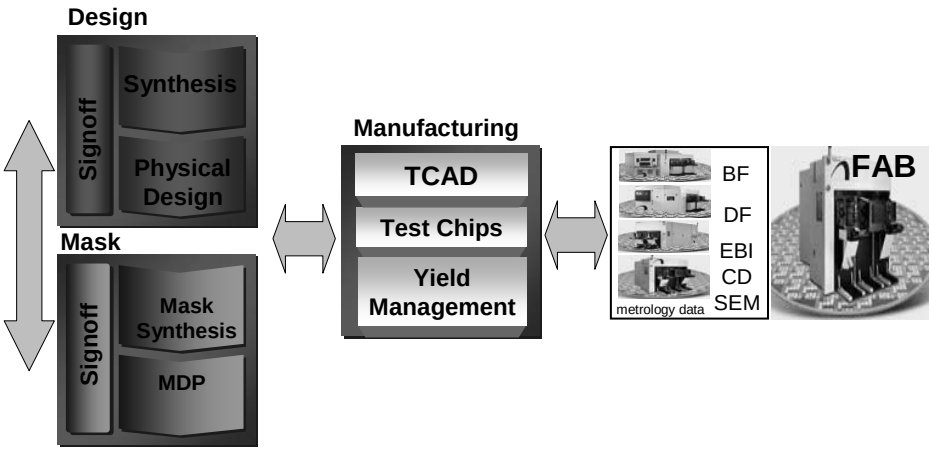
DFM:
Connecting Design and Manufacturing



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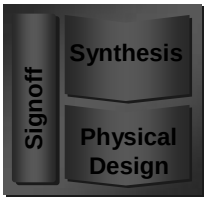
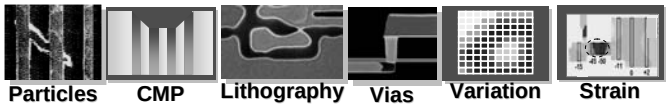
DFM

- Yield graded libraries in synthesis
- Physical design
  - 45nm rules
  - Double vias
  - Spacing
  - …
- M Checking

Design





Particles CMP Lithography Vias Variation Strain

- Extraction
  - CMP Flow
  - Litho Aware Extraction
- Statistical timing

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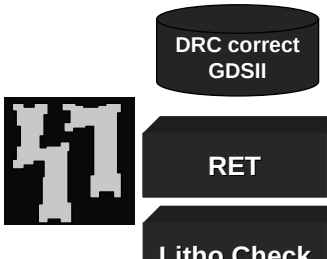
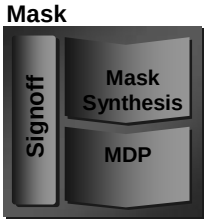
Mask



- AF, OPC, PSM...
- Detailed Litho check
- Writers, inspection
- Corrections (flare)
- Mask rules check

Mask



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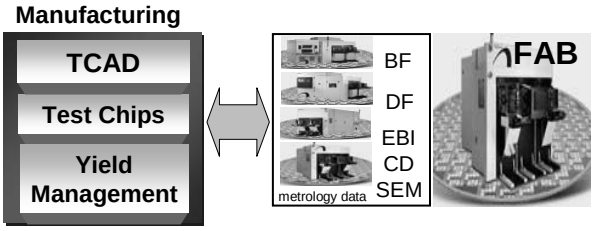
Manufacturing

- **TCAD**
  - **3D**
  - **Topography**
  - **Monte Carlo**
  - **RME link**
  - **PCM**
  - **Design link**
- **Test Chips**
  - **Discrete, Power**
  - **Array**
  - **FinFET**
  - **Design link**
- **YM**
  - **DB**
  - **Predictive defect and failed bitmap analysis methodology**



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Summary

- Connecting design and manufacturing has created a rapidly growing “EDA” market
- Its main components are
  - Design for manufacturing
  - Mask synthesis and verification
  - SW / IP for manufacturing

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