Reconfigurable Multiprocessor System-on-Chip for Embedded Applications

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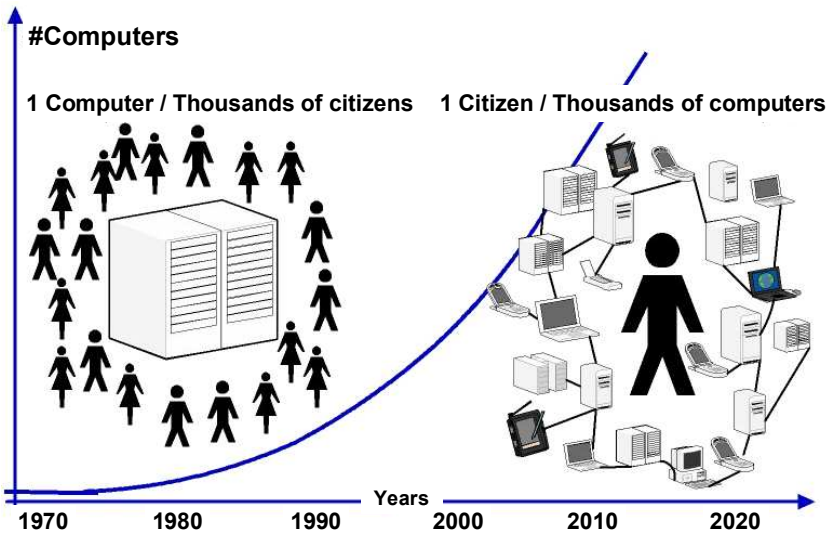
Outline

- More than Moore
- SCMP-LC architecture
- Development environment
- Validation and results
- Conclusion

Computing resources



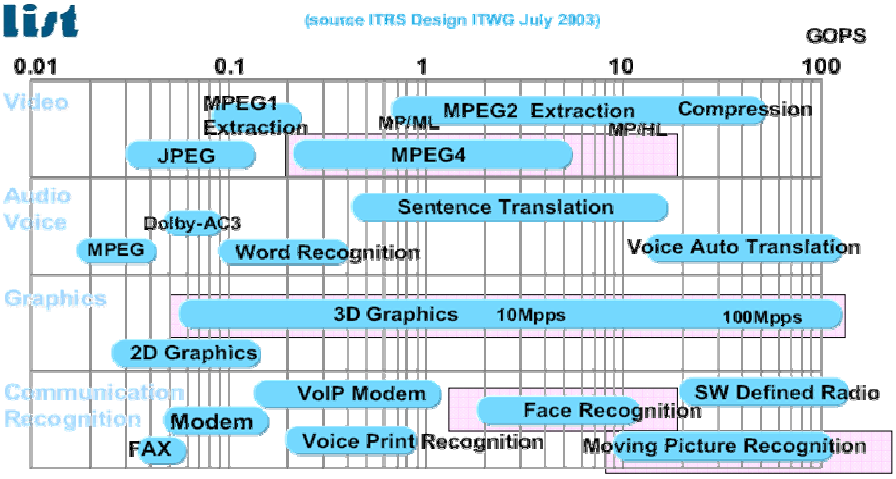
Embedded processing roadmap

x 40

Process Technology (nm)	*130*	*90*	*65*	*45*	*32*	*22*
Operation voltage (V)	1,2	1	0,8	0,6	0,5	0,4
Clock frequency (MHz)	150	300	450	600	900	1200
Application (MAX performance required)	Still Image Processing	Real Time Video Codec MPEG4/CIF		Real Time Interpretation		
Application (Others)	Web Browser Electric mailer Scheduler	TV phone (1:1) Voice recognition (input) Authentification (Crypto engine)		TV phone (>3:1) Voice recognition (operation)		
Processing Performance (GOPS)	0,3	2	14	77	461	2458
Parallelism factor	1	4	4	4	4	4
Communication speed (Kbps)	64	384	2304	13824	82944	497664
Energy Efficiency (MOPS/mW)	3	20	140	770	4160	24580
Peak Power Concumption (mW)	100	100	100	100	100	100
Stand-by Power Concumption (mW)	2	2	2	2	2	2
Battery Capacity (Wh/kg)	120	200		400		

Source ITRS Design ITWG July 2003

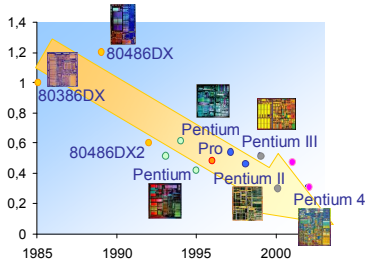
Embedded application roadmap



How to increase performances?

- Temporal acceleration
  - Putting memory near the processor ie duplication of the data and memories
  - Not relevant for embedded market
- Hardwired acceleration
  - Expensive but well suitable solution
  - Unable to cope with the moving environment

Evolution of Intel 32-bit processor performances area efficiency normalized with the 80386DX proc. (CMOS 0.13µm) *



* « Online control of heterogeneous and embedded multiprocessor systems », Ph.D Thesis, CEA LIST, September 2006

CEA LIST activities

- Spatial acceleration
  - Parallelism computing
  - Reconfigurable computing

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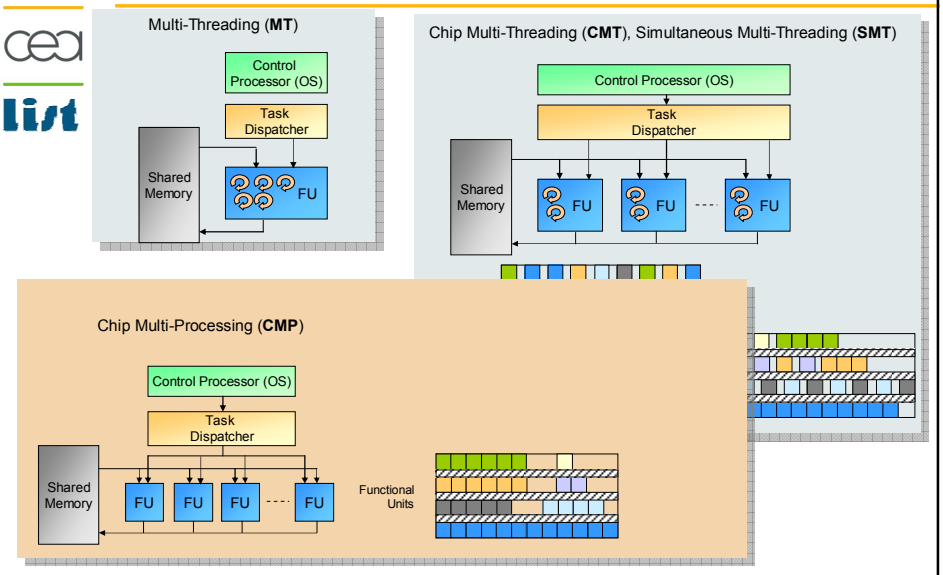
QoS
- •Embedded Realiability
- •Disponibility
- •Low power

Execution models



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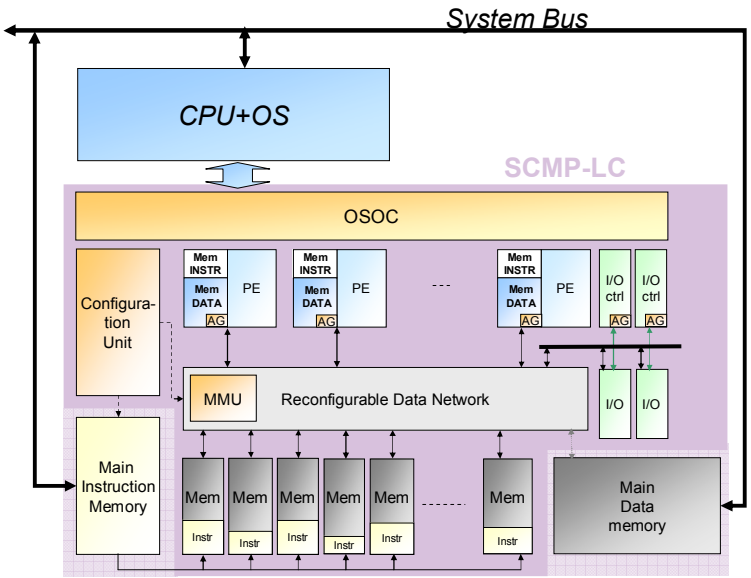
SCMP-LC features

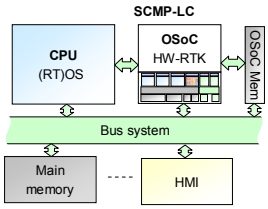
- Multiprocessing architecture
  - CMP based execution model
  - Heterogeneous computing resources
  - Fully determinist control and communication mechanisms
  - Logically shared distributed memories
  - Simple coupling mechanisms with standard operating systems
- Online task management
  - Real time support
  - Online allocation with task preemption and migration
  - Online scheduling based on task laxities
  - Activation of idle states and control of DVFS modes based on slack time distribution
  - Operating system hardware acceleration to reduce control overhead

The SCMP-LC architecture



OSoC: Operating System accelerator on Chip*

- HW Operating System accelerator (OSoC)
- Task selection
  - Data and control dependency management
  - Simple coherency policy management
  - Dynamic execution flow management

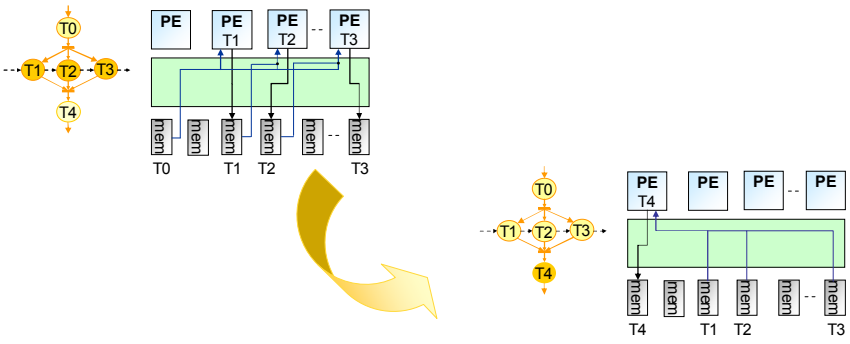


- Task scheduling
  - Online real-time and non-real-time scheduling
  - Energy consumption management (idle states, DVFS)
- Task allocation
  - Heterogeneous computing resources
  - Preemption and migration

* « Online control of heterogeneous and embedded multiprocessor systems », Ph.D Thesis, CEA LIST, September 2006

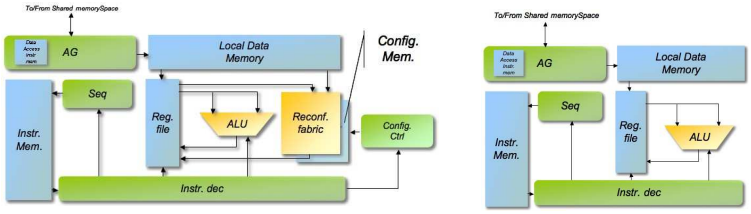
Communications

- Ensure data sharing between tasks
- Based on a logical sharing of distributed memories
- Dynamic memory allocation to processors managed by dedicated controllers
- Exchanges with peripheral devices supervised by the OSoC



Processing resources

- Control structure are simple microsequencers
- Dedicated structures (AG) allow computation and communication overlap
- Dedicated local storage resources
- Large range of computation units are possible
  - From simple ALUs to complex pipeline of reconfigurable operators



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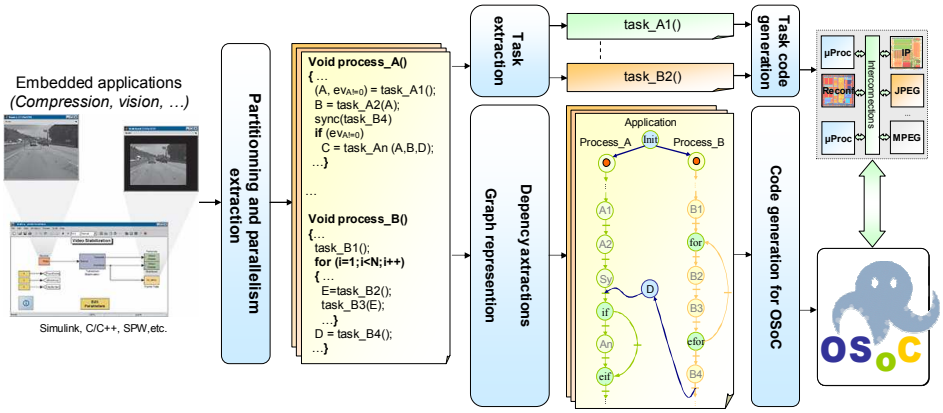
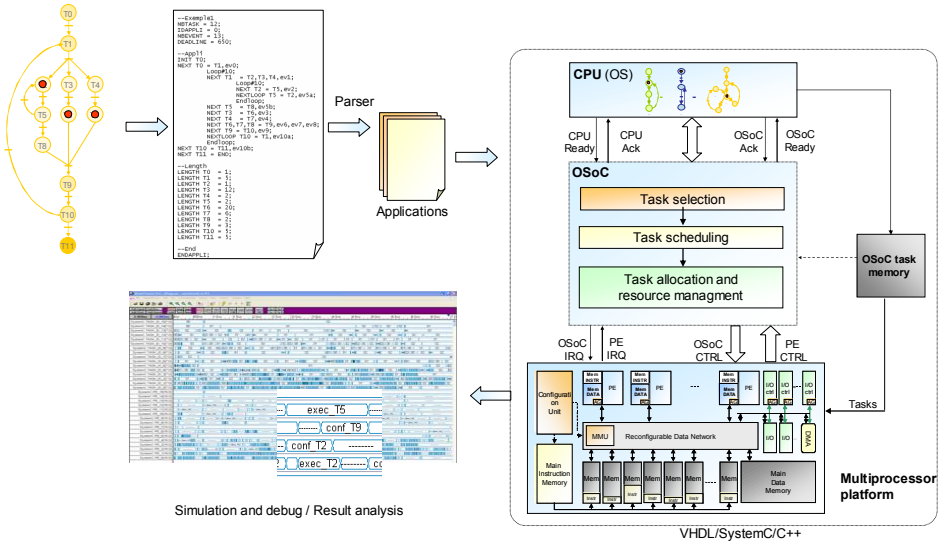
Programming model of SCMP-LC architecture

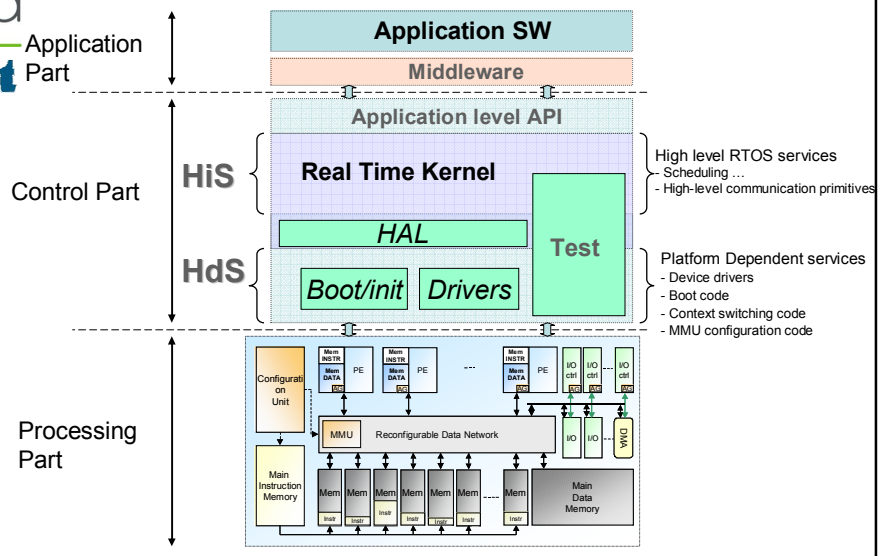
- Different abstraction programming levels
- Independent tasks
- Task extraction according to data and control dependencies



Simulation platform



System level modelling of the control part



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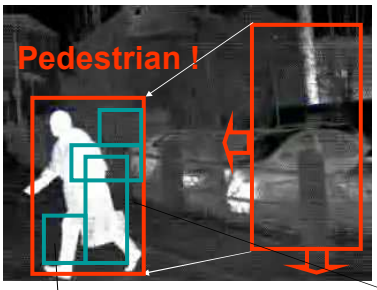
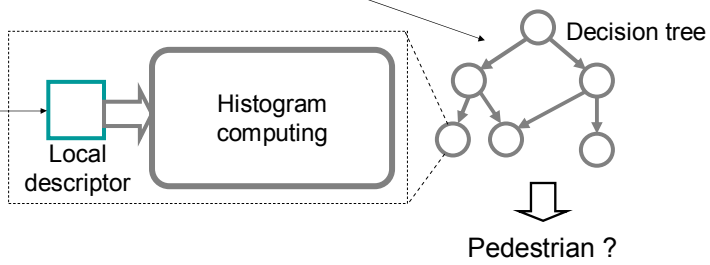
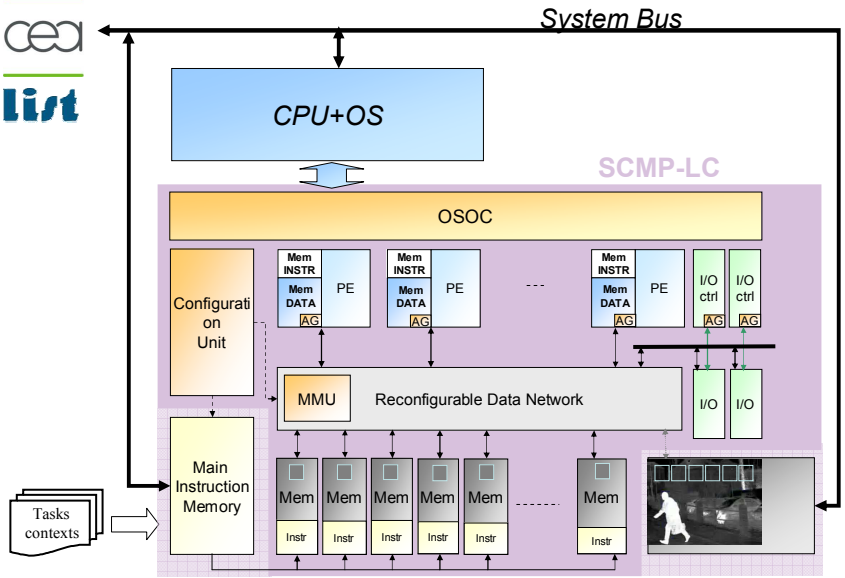
Computer vision application



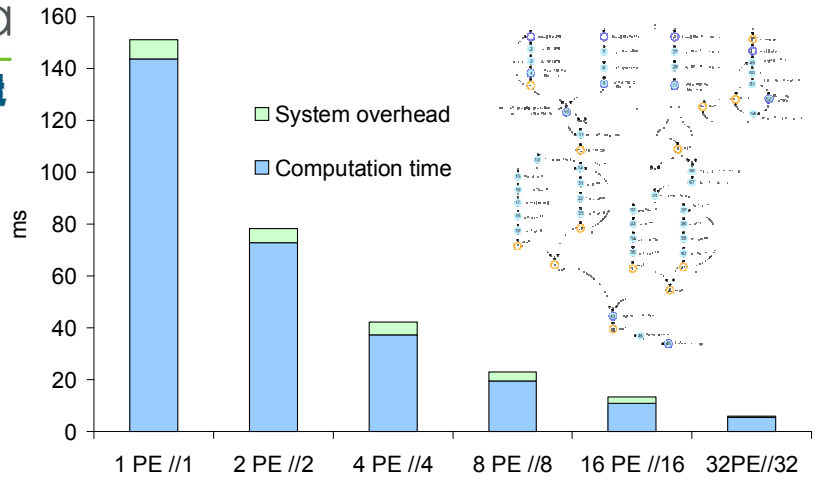
- Windows are used to search pedestrian
- Windows are shrunk and moved



Exemple : computer vision application (2)

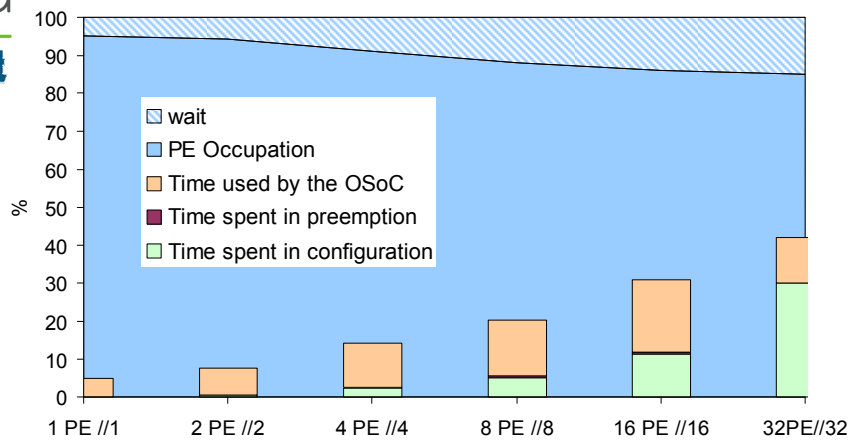


Results on MPEG 4 AVC application (1)



Overall execution time of the MPEG4-AVC encoder on 64MBs
(OSoC - ARM920T processors)

Results on MPEG 4 AVC application (2)



Resource utilization with the MPEG4-AVC encoder
(OSoC - ARM920T processors)

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Conclusion

- Proposition of a new multicore architecture for embedded applications:
  - CMP execution model and TLP
  - Online task managment
  - Hardwired Operating System accelerator (OSoC)
  - Cacheless architecture
- Programming model based on graph description of the applications
- Silicon implementation under progress
- High parallism rate (near 90%) for 32 cores on embedded applications.