QoS profiling using NoC Adaptive Design Information System

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THE NETWORK-ON-CHIP COMPANY

MPSOC

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Founder & CTO

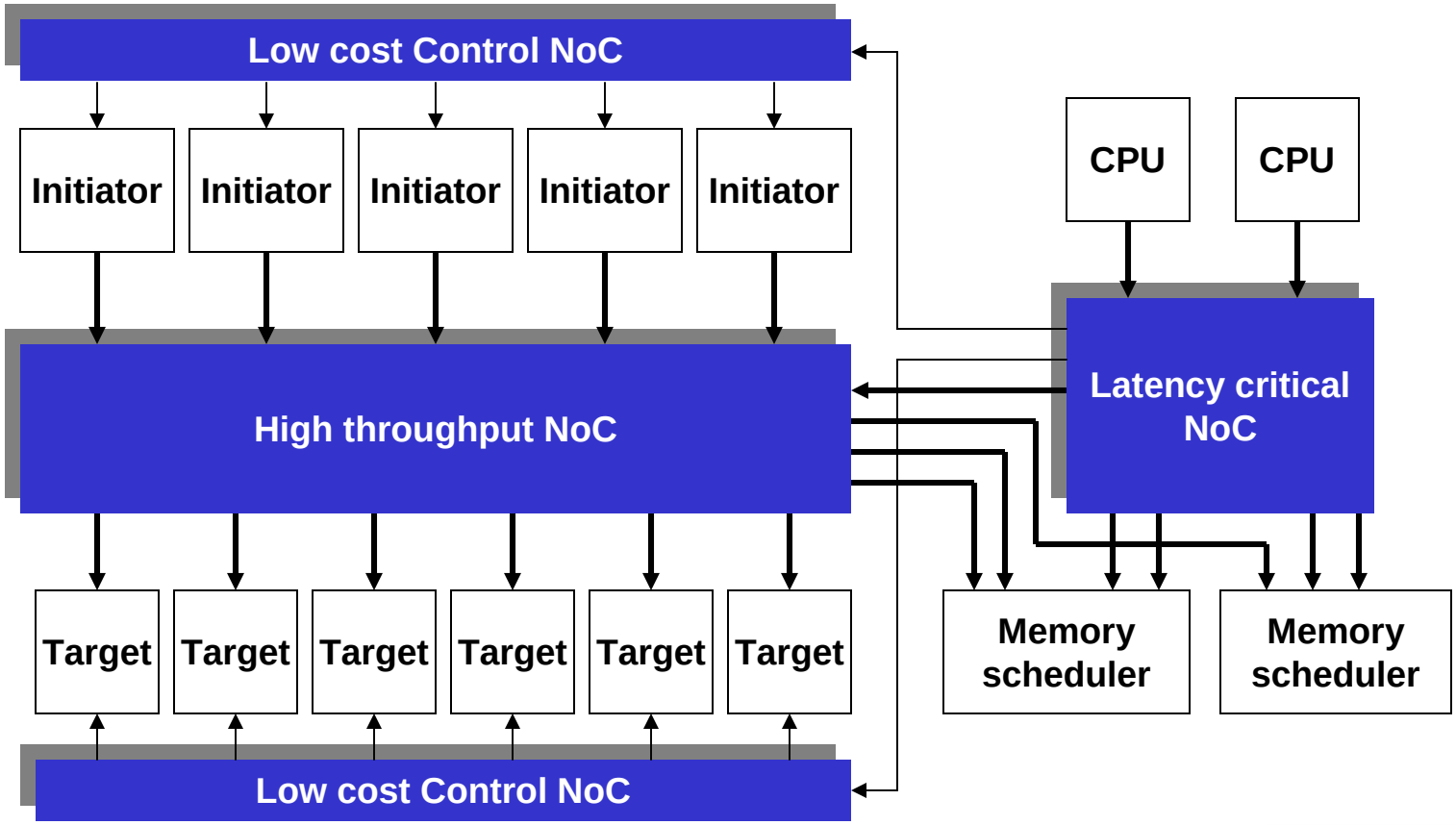
Agenda

- SoC complexity and cost constraints challenge on-chip communication system architecture.
- On-chip Data flows Quality (QoS) drive new taxonomy, language and new implementation techniques
- ARTERIS proposes an Adaptive Information System environment to solve this designer's challenge
- Let's work on an example: Multimedia consumer SoC
- Next

System Determinism

- **By construction:**
  - Time Division Multiplexing or Circuit switched Network guarantees determinism by construction.
- **By Cognition:**
  - Adaptive Network Information System guarantees determinism by traffic simulation & scheduling techniques

NoC - Separate traffic classes



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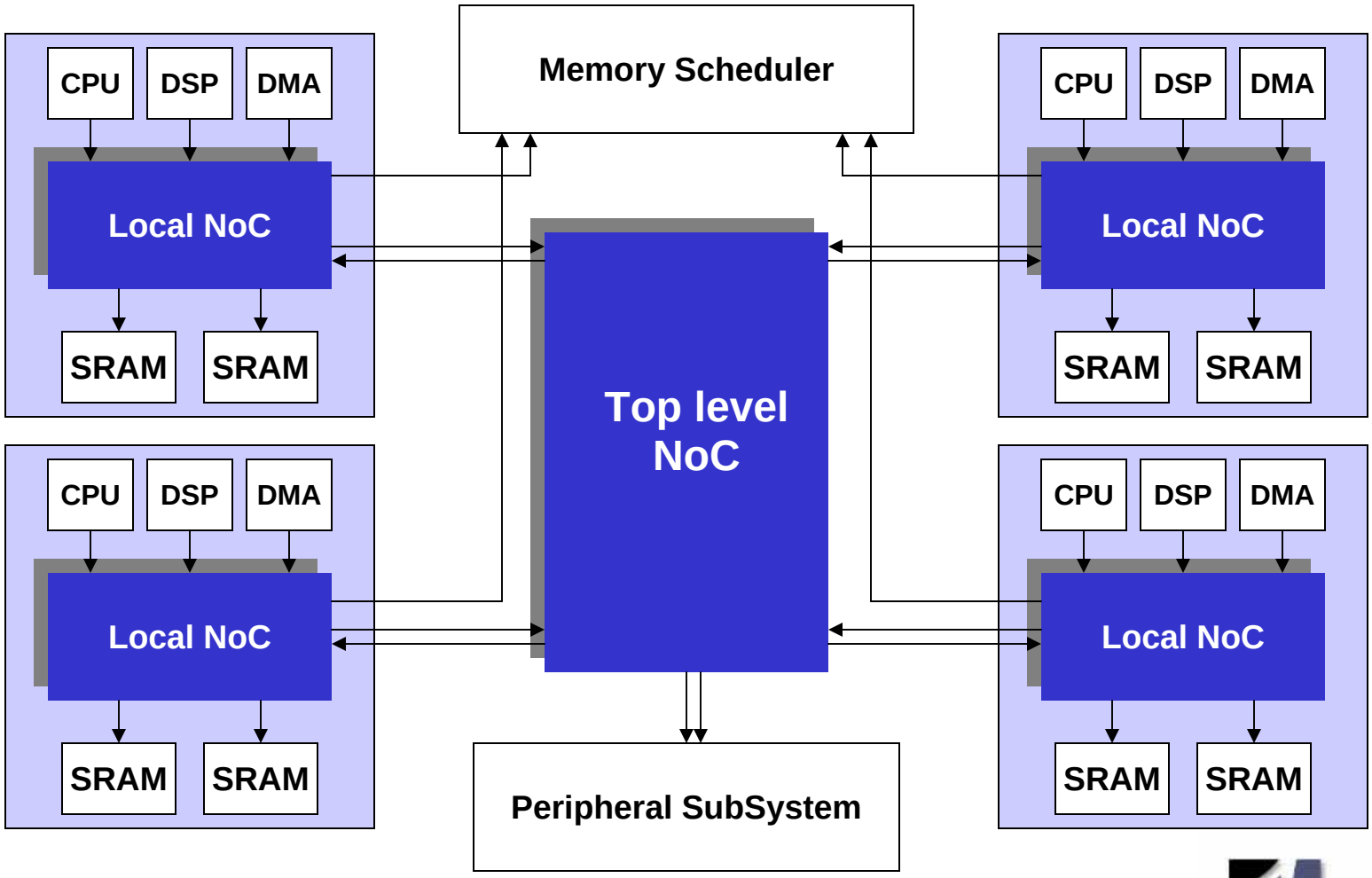
NoC - Clustered Design



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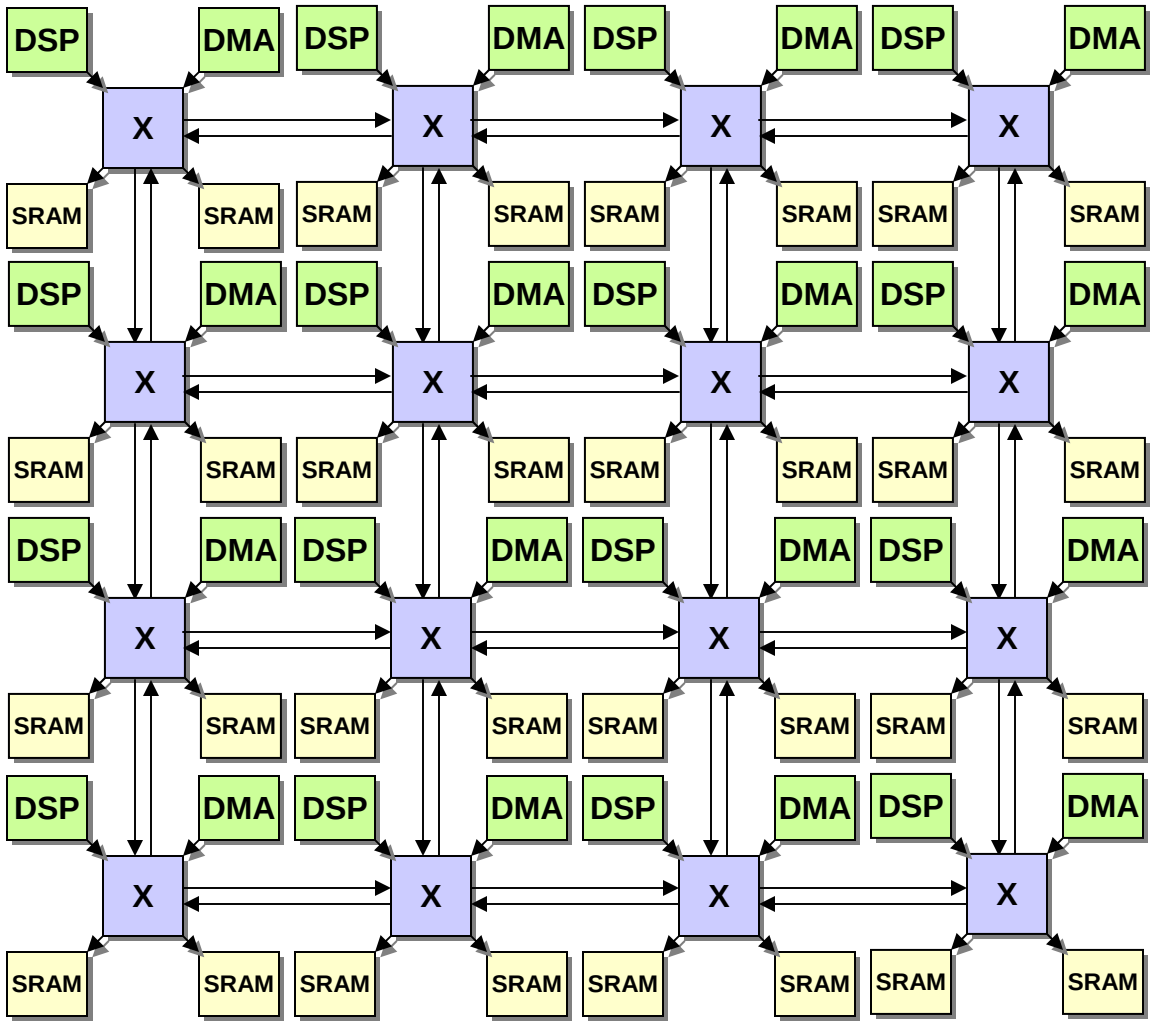
NoC - 2D mesh



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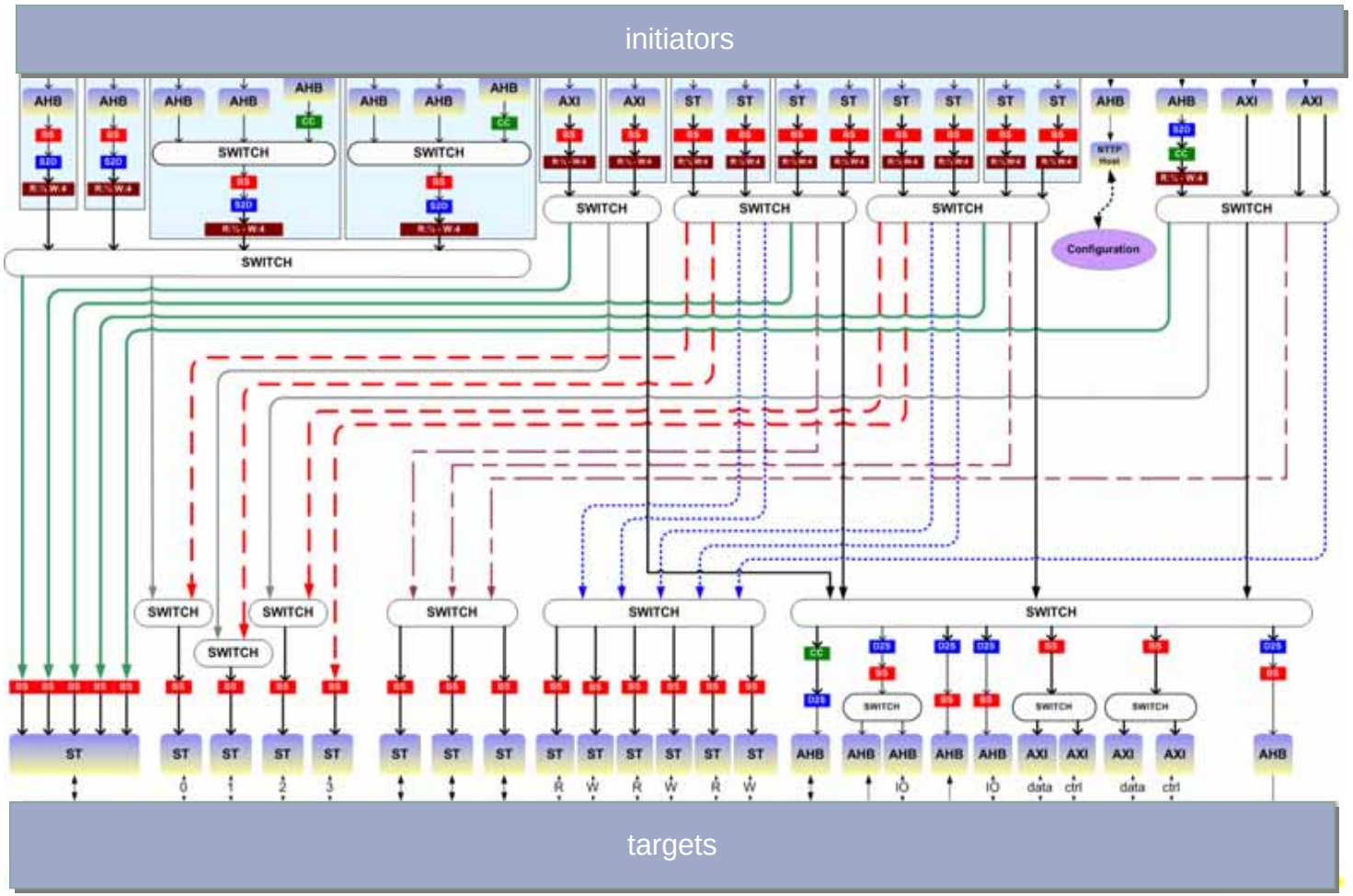
SoC Application (*)



(*) Authorized by STMicroelectronics Wireless Infrastructure Division

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Designer Challenges

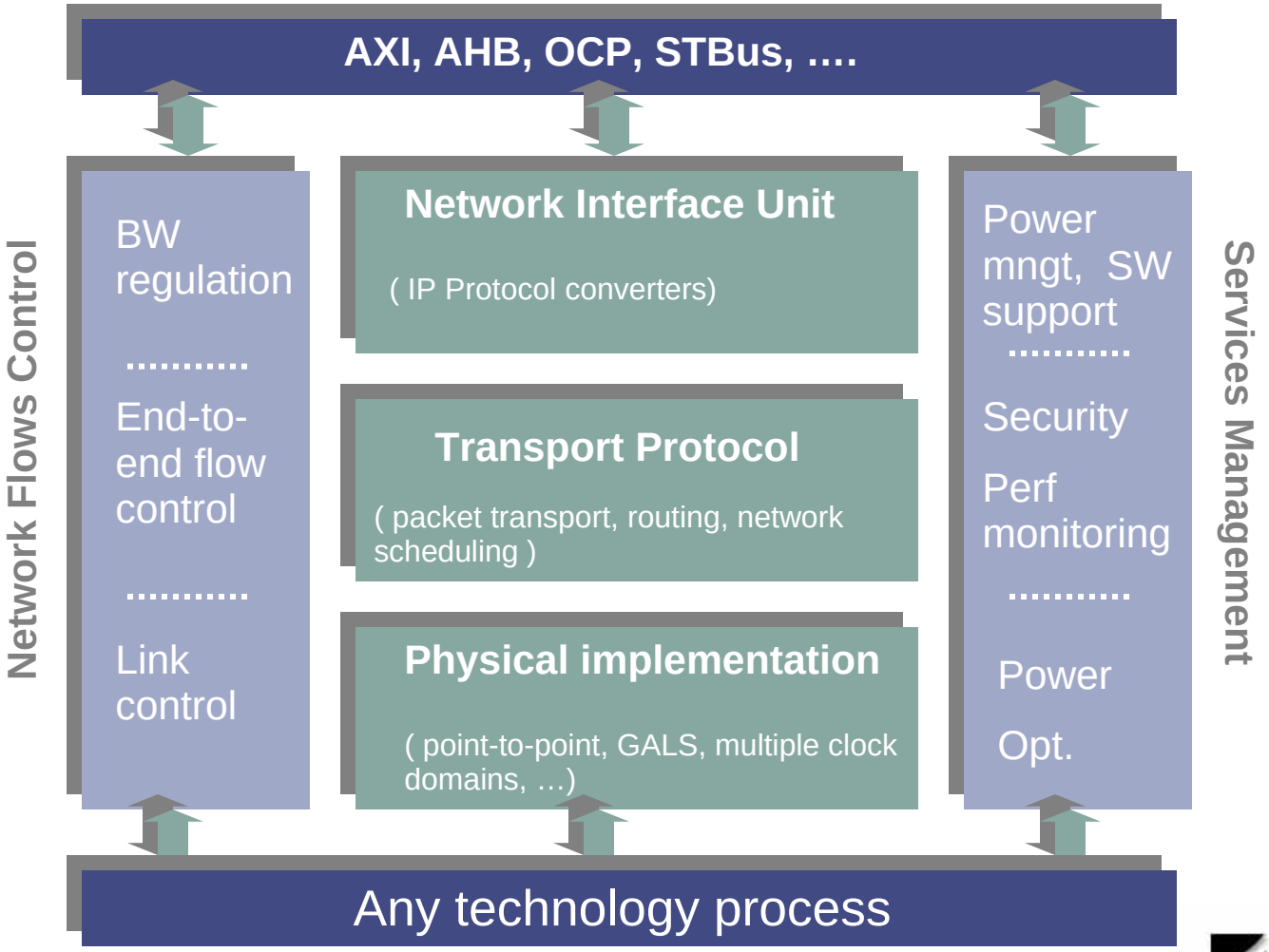
- Different Application domains
- Cost Of Design full determinism Networks
- Information flows are asynchronous
- QoS formal analysis is not applicable

ARTERIS Approach

- **Few data flows required “hard” determinism**

- **ARTERIS communication system is based on:**
  - Highly flexible & structured Network On Chip architecture
  - An adaptive Network system information environment to reach completeness in designing QoS.

Structured NoC



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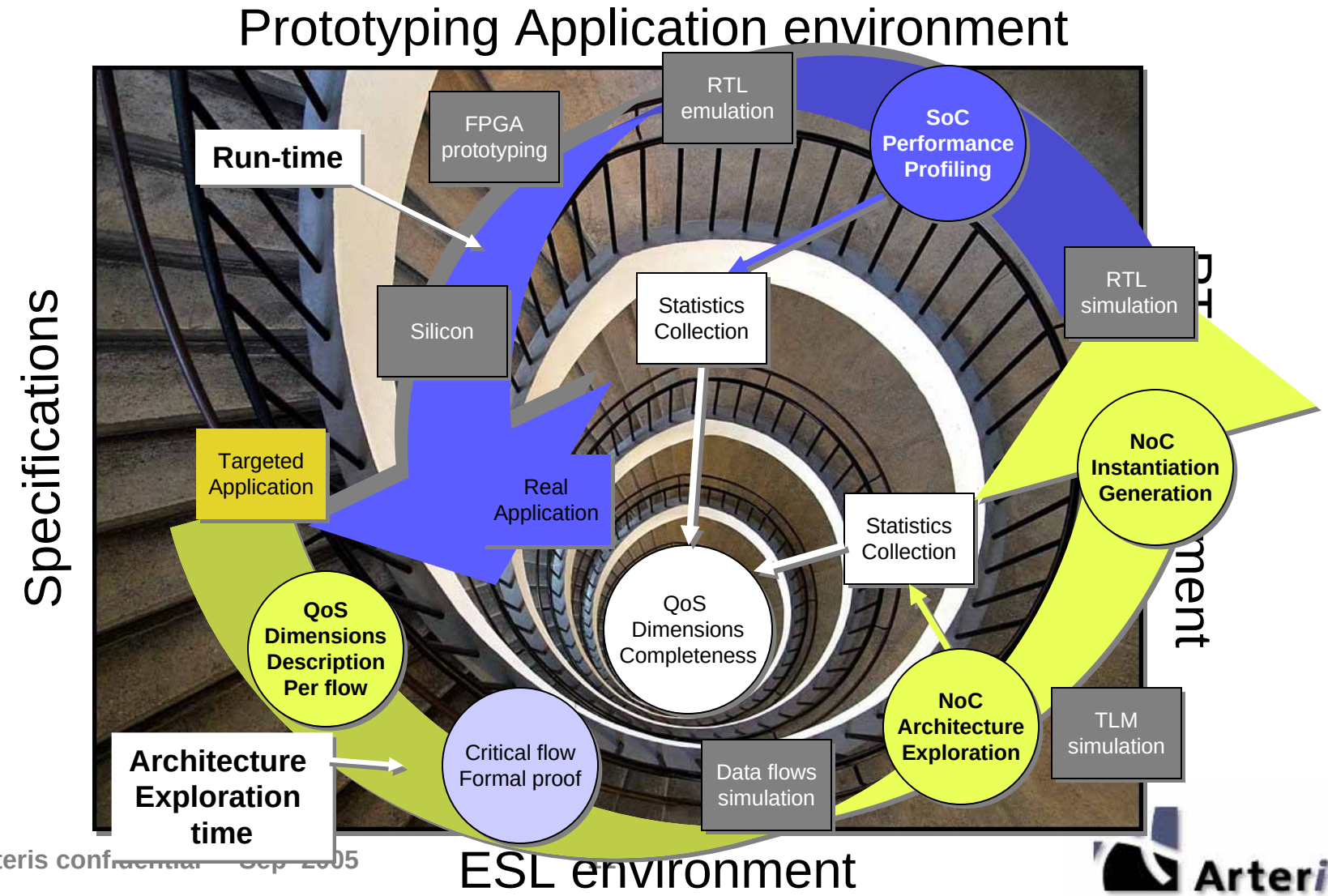
Adaptive Information System



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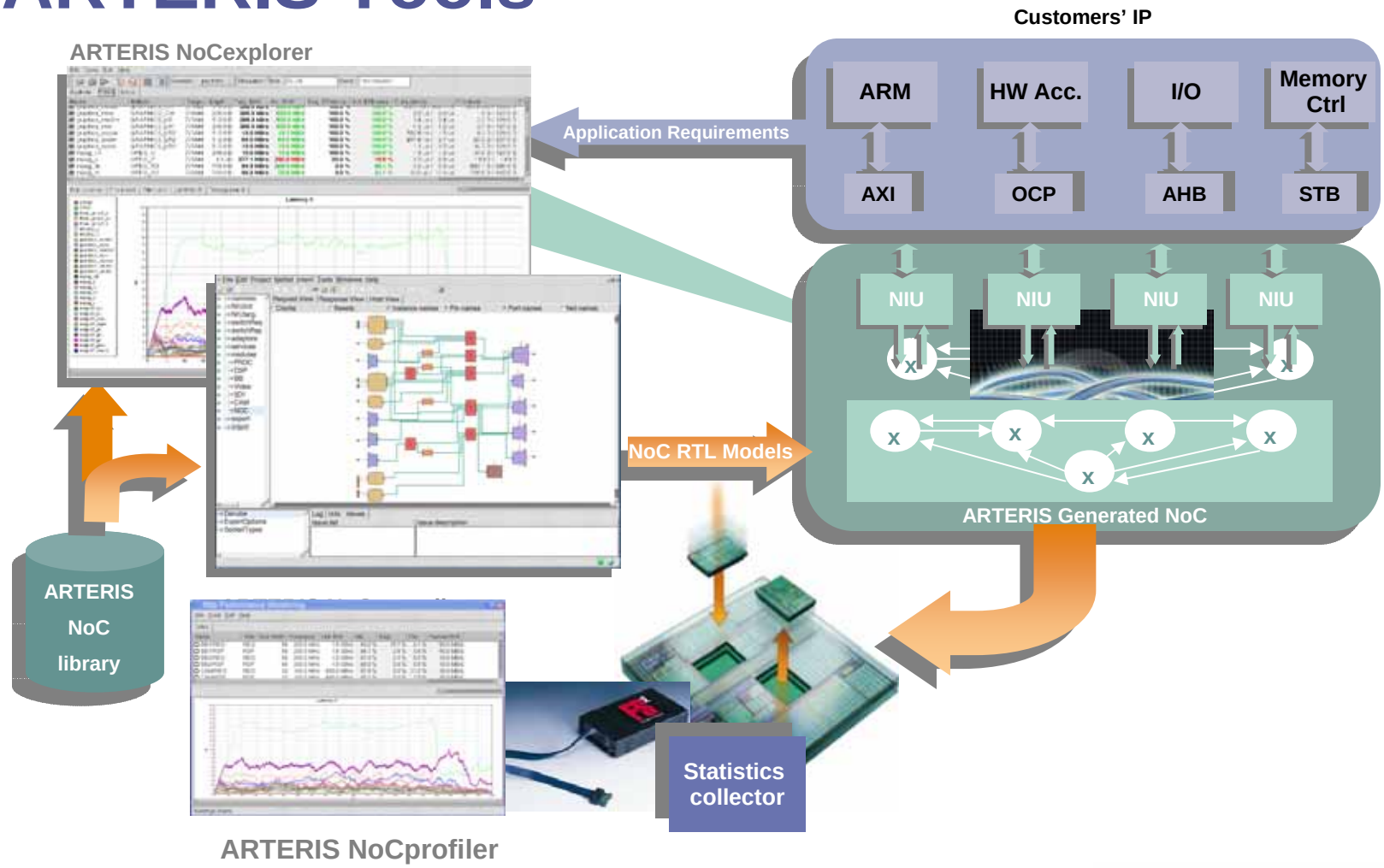
Models

- **Interface models**
  - IP sockets, connectivity map & memory map
- **Data flow models**
  - QoS dimensions / metrics (Throughput, latency, security level)
  - Policies (level of service, tolerances, interdependency, scheduling policies)
- **Architectural models**
  - Devices & network components

Methods

- **Exploration time**
  - Data flow modeling
    - Modified Khan computing model
    - Very efficient data flow abstraction level
    - Communication modeling (scheduling, efficiency)
    - Target modeling
  - Architectural modeling
    - Network architecture implementation & abstraction level views (TLM, RTL) fully independent to data flow modeling
    - ARTERIS NoC Specific (topology, buffering, arbitration)
- **Run-time**
  - Selective NoC specific flow probing

ARTERIS Tools



Customer's SoC

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QoS dimensions & Architectural models

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Quality taxonomy

Class	Definition	Metrics	Example
A	Guaranteed Data integrity	Security (addr. mapping)	Security, fault tolerant, firewall,
B	Constant guaranteed throughput on short period	Bit rate	Video In/Out, Sonet, Audio…
C	Latency guaranteed until a given throughput	Latency	CPU
D	Guaranteed IP task throughput on long period within a given MTBF	Bandwidth / Tolerance	MPEG or CDMA processing
E	Best Effort	Efficiency / Tolerance	CPU when not latency guaranteed

Data flow Policies

- Store
- Load
- Stress
- Flows dependencies
- Scheduling (random,…)
- Flows synchronization
- Flows Decoupling

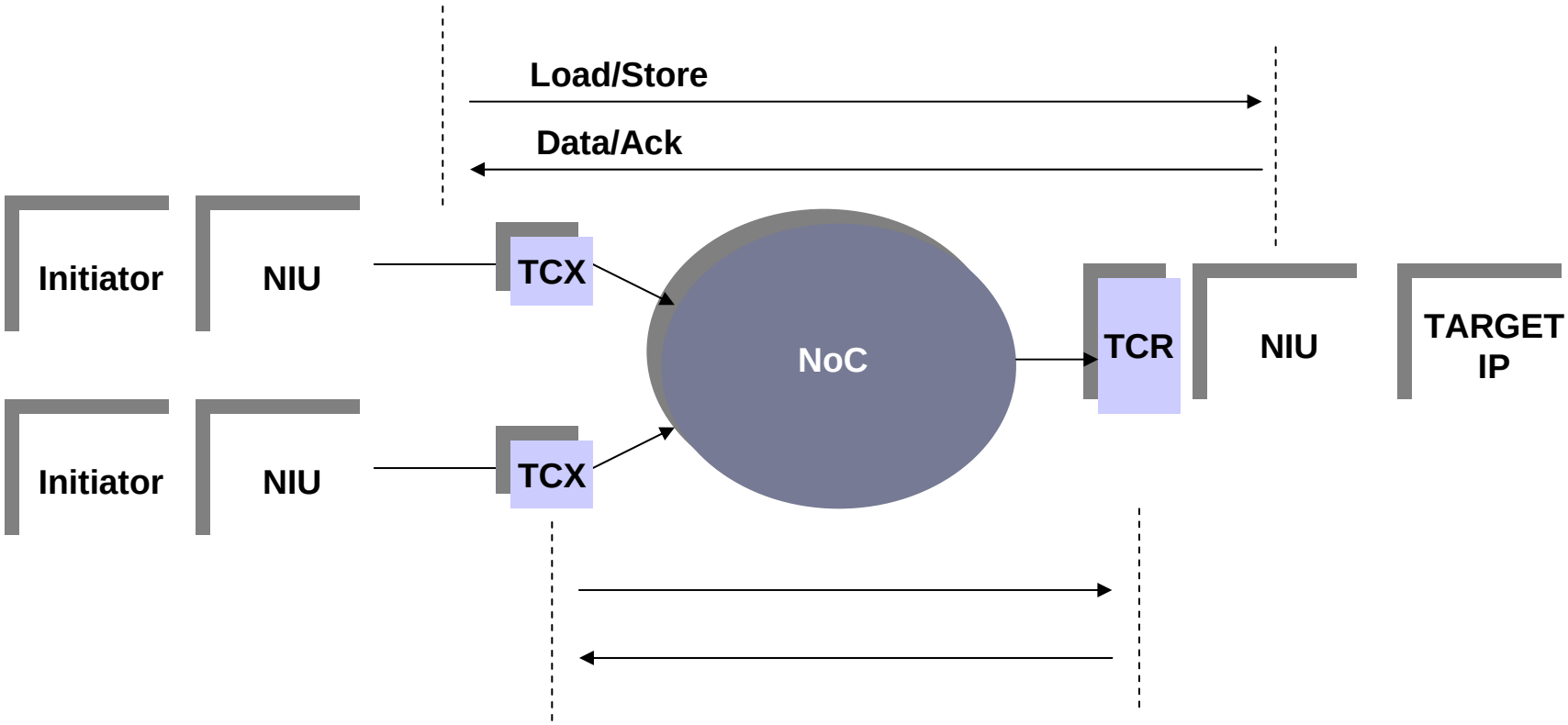
Architectural models

- **IP Initiators:**
  - IP sockets (AXI, OCP, AHB,..)
- **IP Targets:**
  - IP sockets (AXI, OCP, AHB,..)
  - DRAM device and scheduler
  - SRAM
- **Network components**
  - Switches (), Links (), FIFO()
  - Rate adapters (), Size converters ()
  - QoS components (end-to-end FC, arbiter, Bandwidth regulator, multiclock domain..)
  - Chip-to-chip link

QoS Components

Complexity / NoC Features	< 30 I.P.	< 100 I.P.	> 100 I.P.
NoC Predictability	- Sparse packet crossbar	- Threaded IP - Virtual Channel link	- End-to-End NoC Flow control
NoC Scheduling	- Application Pressure - Fixed Priority - Multiple Arbitration scheme	- Bandwidth Regulator - Events: DmaReq and Interrupts	- New arbitration schemes (weighted fair queuing, scheduling, ..)
Technology	130/90 nm	65/45 nm	< 45 nm

End-to-end flow control components



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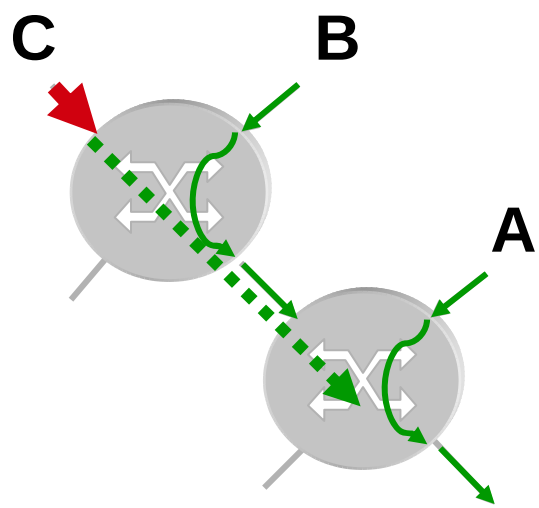
NoC Scheduling - Arbitration



- **Dynamic packet priority scheme**
  - Per-output arbitration
- **Priority propagates ahead of packets (pressure)**
- **When pressure is equal**
  - Fixed Priority (reprogrammable)
  - Round-robin
  - Aging
- **Pressure generation**
  - By the IP: FIFO Threshold
  - By the NIU: Guaranteed bandwidth

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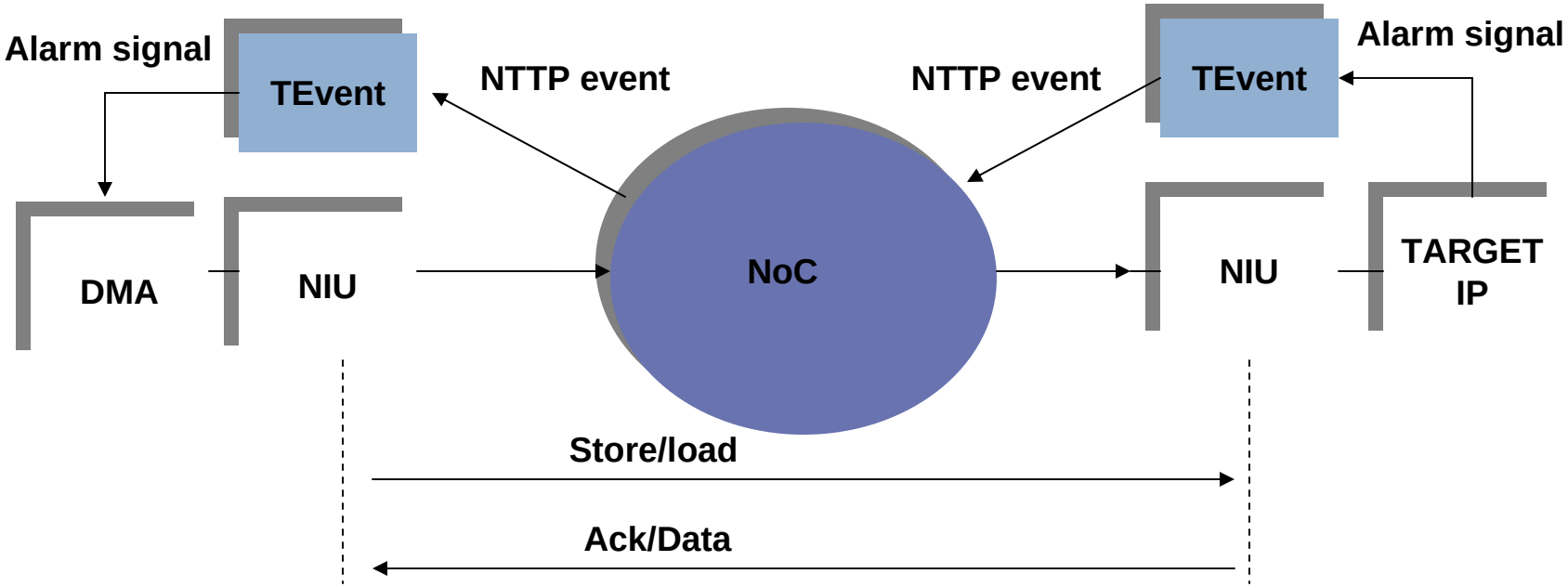
NoC Scheduling - Signalisation



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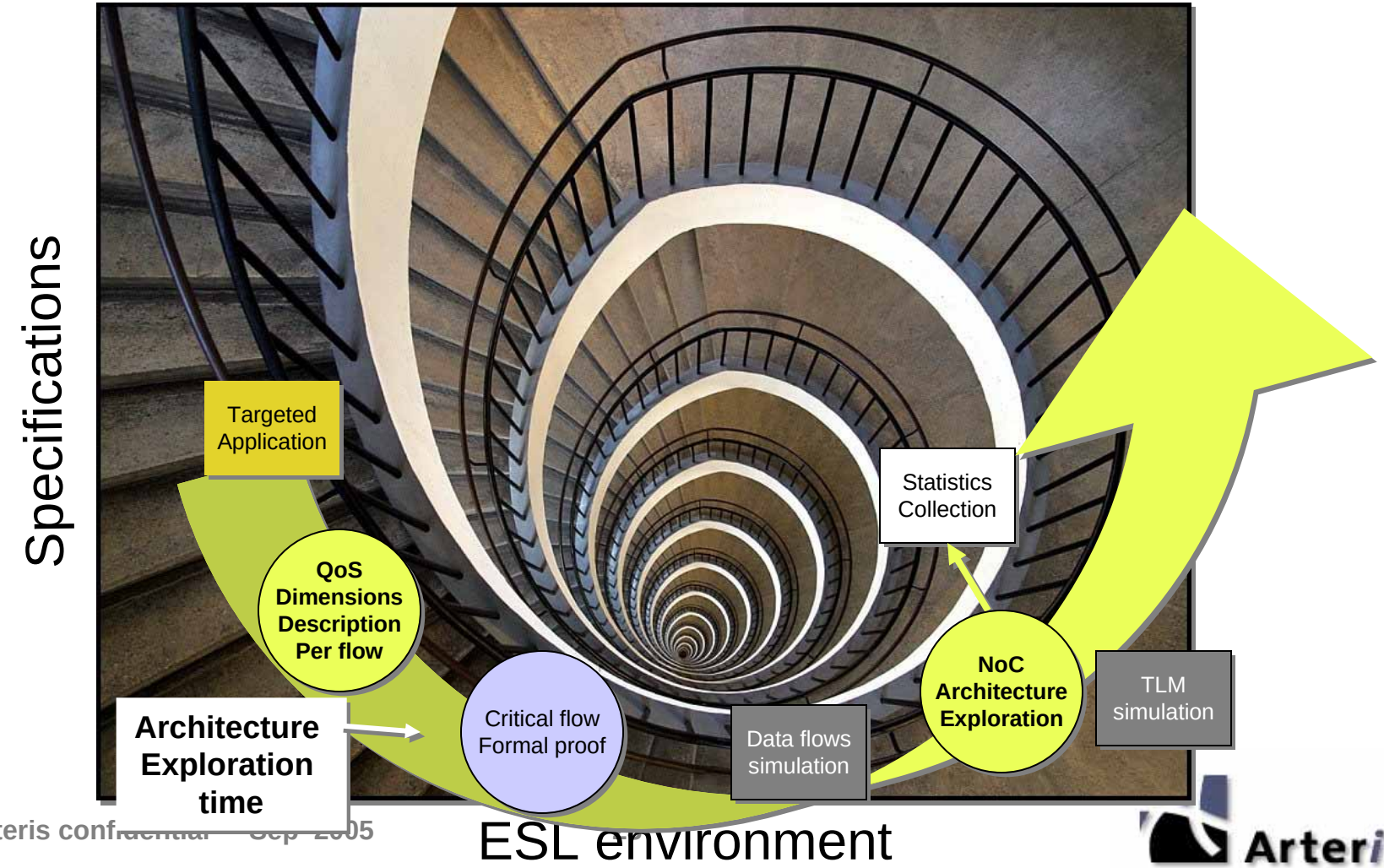
Architecture Exploration



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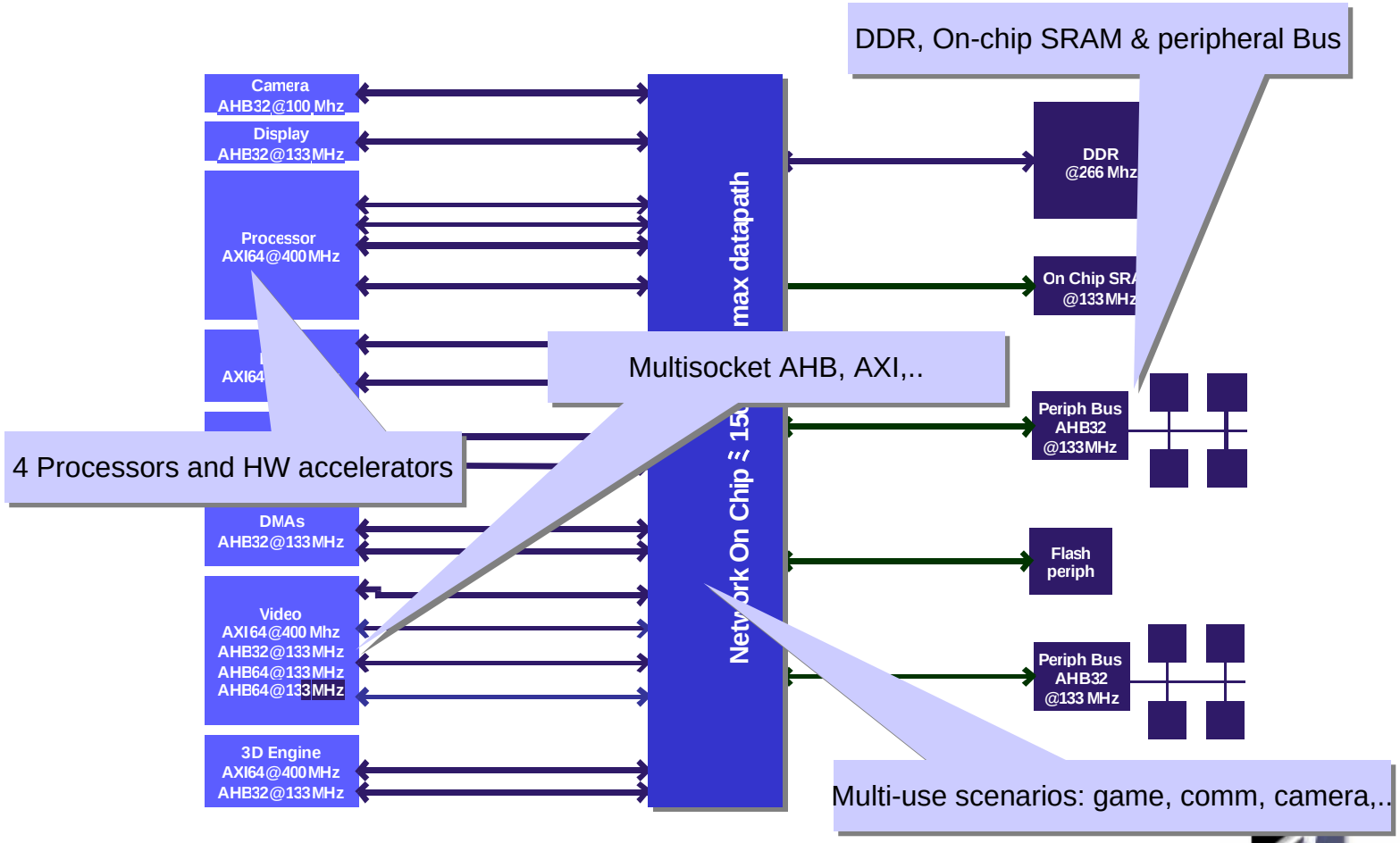
Wireless Multimedia Application Processor



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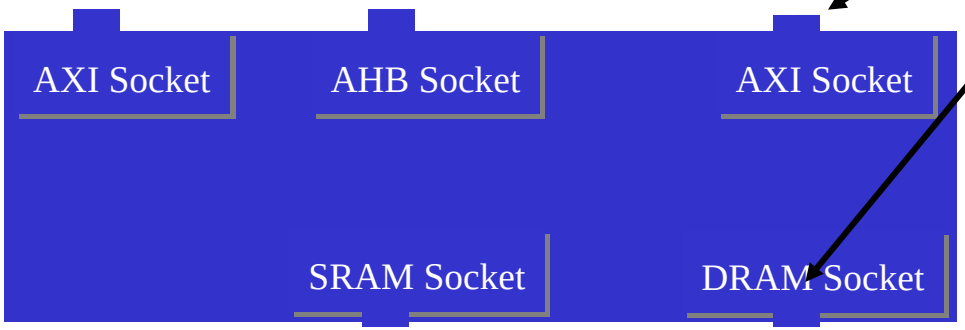
NoC Interfaces Modeling

- **Create your socket classes**
- **Use them when defining your interface**
  - Socket have mandatory attributes
    - Width (aData)
    - Operating frequency (frequency)
  - And optional ones
    - For initiators
      - maxPendingTransaction
      - maxPendingTarget
      - maxPendingVolume
    - For targets:
      - bankDelay
      - rwDelay
      - wrDelay

```
class myAxiSocket(AxiInitiator) :
            aData     = 64
            frequency = 200e6
Classs myDramSocket(DramTarget) :
            aData     = 64
            frequency = 200e6
            bankDelay = 50e-9
            turnDelay = 10e-9

class myIfce(NocInterface):
            class AXI_Socket(myAxiSocket)  : pass
            class DRAM_Socket(myDramSocket): pass
…
```



Target model

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NoC explorer view

NoCexplorer (/disk056/gilles/BASE/DACdemoTest/base/customers/demos/dac2006/s...

File Tools Edit Help

Scenario : diag0ap2 Simulation Time : 2e-04 Seed : 1151917466

Sockets | Flows | Links

Name	Side	Bus Width	Frequency	Link BW	Payload BW
BB1	INIT	64	200.0 MHz	1.6 GB/s	-
BB2	INIT	64	200.0 MHz	1.6 GB/s	-
CAM	INIT	32	133.0 MHz	532.0 MB/s	-
CPUD	INIT	64	400.0 MHz	3.2 GB/s	-
CPUI	INIT	64	400.0 MHz	3.2 GB/s	-
CPUP	INIT	32	400.0 MHz	1.6 GB/s	-
CPUT	INIT	64	400.0 MHz	3.2 GB/s	-
DDD1	INIT	32	400.0 MHz	1.6 GB/s	-
DDD2	INIT	32	133.0 MHz	532.0 MB/s	-
DISP	INIT	32	133.0 MHz	532.0 MB/s	-
DMA1	INIT	32	133.0 MHz	532.0 MB/s	-
DMA2	INIT	32	133.0 MHz	532.0 MB/s	-
DSP1	INIT	64	200.0 MHz	1.6 GB/s	-
DSP2	INIT	64	200.0 MHz	1.6 GB/s	-
PER1	TARG	32	133.0 MHz	532.0 MB/s	-
PER2	TARG	32	133.0 MHz	532.0 MB/s	-
PER3	TARG	32	133.0 MHz	532.0 MB/s	-
SDRAM	TARG	64	133.0 MHz	1.1 GB/s	-
SRAM	TARG	64	133.0 MHz	1.1 GB/s	-
USB	INIT	32	133.0 MHz	532.0 MB/s	-
VIDEO1	INIT	64	133.0 MHz	1.1 GB/s	-
VIDEO2	INIT	64	133.0 MHz	1.1 GB/s	-
VIDEO3	INIT	64	400.0 MHz	3.2 GB/s	-
VIDEO4	INIT	32	133.0 MHz	532.0 MB/s	-

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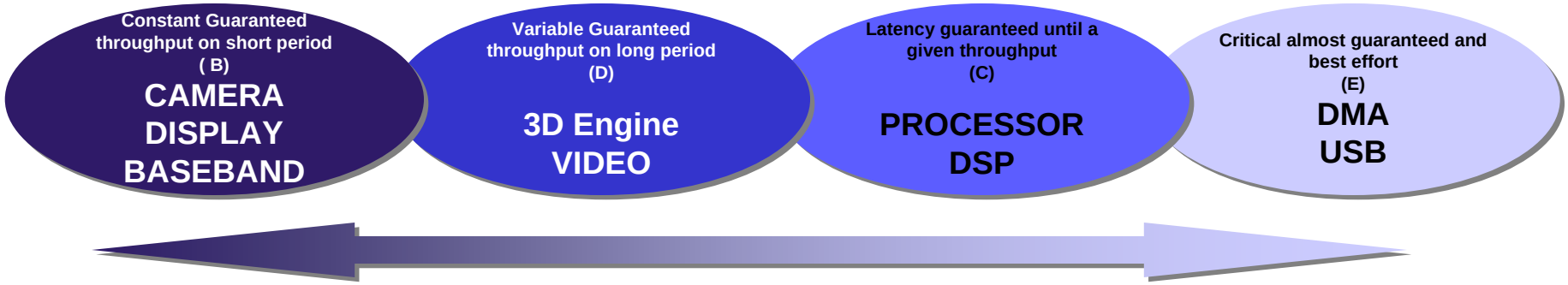
QoS Dimensions



BW in MB/s	Initiator Target	Processor				3D Engine		DSP		VIDEO				CAM	DISP	USB	DMA		BaseB		Total(DRAM)	
frequency (MHz)		400	400	400	400	400	133	200	200	400	133	133	133	100	133	133	133	133	200	200		
socket / Width		AXI64	AXI64	AXI64	AXI64	AXI64	AHB32	AXI64	AXI64	AXI64	AHB32	AHB64	AHB64	AHB32	AHB32	AHB32	AHB32	AHB32	AXI64	AXI64		
Port name		D	T	I	P	#1	#2	#1	#2	VID3	VID4	VID1	VID2				#1	#2	#1	#2		
Scenario 1	DRAM	70	15	100			100	30	30	60		50	50		150			45	40	10	750	70.5%
Scenario 2	DRAM	70	15	100			100	30	30	120				140	140			45	40	10	840	78.9%
Scenario 3	DRAM	70	15	100		200		30	30						150			45	40	10	690	64.8%
	SRAM	10																130				
	Per1																20					
	Per2				3						5						10					
	Per3				3																	

Scenario1: Audio - Video - Telecom - Storage

Scenario 2: Video (encode only) - preview picture - audio - telecom

Scenario 3: Audio - Game - Telecom - storage

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SoC traffic modeling

NoCexplorer (/disk056/gilles/BASE/DACdemoTest/base/customers/demos/dac2006/suite/NoC.py)

File Tools Edit Help

Scenario : diag0ap2 | Simulation Time : 2e-04 | Seed : 1151917466

Sockets | Flows | Links

Name	Initiator	Target	Depth	Targ. B/W	Act. B/W	Req. Efficiency	Act. Effic	Full Latency	Socket Latency	Fifo level
cam	CAM	SDRAM	256.0 B	180.0 MB/s	0.0 B/s	100.0 %	-	- / -	- / -	- / -
cell1_sdram	BB1	SDRAM	256.0 B	48.0 MB/s	0.0 B/s	100.0 %	-	- / -	- / -	- / -
cell2_sdram	BB2	SDRAM	64.0 B	12.0 MB/s	0.0 B/s	100.0 %	-	- / -	- / -	- / -
cpuD	CPUD	SDRAM	32.0 B	96.6 MB/s	0.0 B/s	70.0 %	-	- / -	- / -	- / -
cpuI	CPUI	SDRAM	32.0 B	193.2 MB/s	0.0 B/s	70.0 %	-	- / -	- / -	- / -
cpuT	CPUT	SDRAM	32.0 B	20.7 MB/s	0.0 B/s	70.0 %	-	- / -	- / -	- / -
disp	DISP	SDRAM	256.0 B	180.0 MB/s	0.0 B/s	100.0 %	-	- / -	- / -	- / -
dma1_per1	DMA1	PER1	32.0 B	24.0 MB/s	0.0 B/s	100.0 %	-	- / -	- / -	- / -
dma1_per2	DMA1	PER2	32.0 B	6.0 MB/s	0.0 B/s	100.0 %	-	- / -	- / -	- / -
dma2_sdram	DMA2	SDRAM	128.0 B	60.0 MB/s	0.0 B/s	100.0 %	-	- / -	- / -	- / -
dma2_sram	DMA2	SRAM	128.0 B	12.0 MB/s	0.0 B/s	100.0 %	-	- / -	- / -	- / -
dsp1	DSP1	SDRAM	16.0 B	48.0 MB/s	0.0 B/s	70.0 %	-	- / -	- / -	- / -
dsp2	DSP2	SDRAM	16.0 B	48.0 MB/s	0.0 B/s	70.0 %	-	- / -	- / -	- / -
rdr1	DDD2	SDRAM	1.6 kB	64.5 MB/s	0.0 B/s	65.0 %	-	- / -	- / -	- / -
rdr2	DDD2	SDRAM	1.6 kB	64.5 MB/s	0.0 B/s	65.0 %	-	- / -	- / -	- / -
tmd_sdram_cache	VIDEO3	SDRAM	256.0 B	60.0 MB/s	0.0 B/s	100.0 %	-	- / -	- / -	- / -
tmd_sdram_word	VIDEO3	SDRAM	256.0 B	12.0 MB/s	0.0 B/s	100.0 %	-	- / -	- / -	- / -

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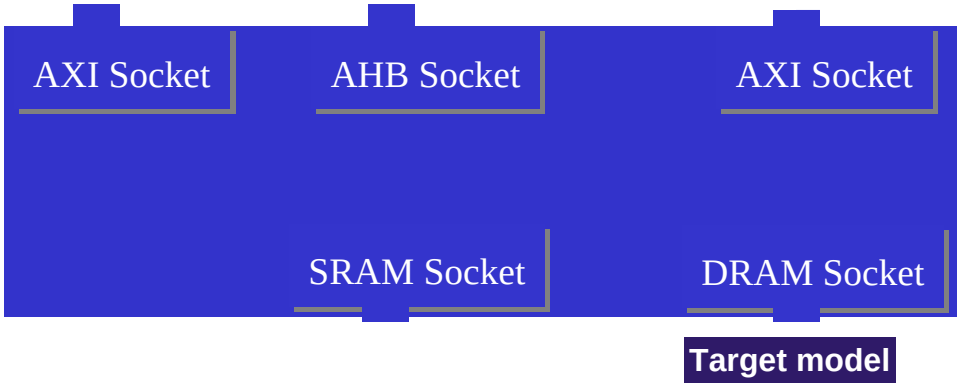
Data Flow modeling

- **Flows have the following attributes**
  - **initiator** (initiator socket they are attached to)
  - **target** (target socket they access)
  - **stress** (the traffic they play
  - **depth** (size of the internal FIFO they model)
  - **efficiency** (percentage of the time they are not blocked)
- **First, attach the Flow to an initiator socket**
- **Then, define the destination of the flow**

```
Class myFlow(Flow):
            initiator  = myIfce.AXI_Socket
            target     = myIfce.DRAM_Socket
            stress     =
            depth      =
            efficiency =
```




```
class myIfce(NocInterface):
            class AXI_Socket(myAxiSocket)  : pass
            class DRAM_Socket(myDramSocket): pass
…
```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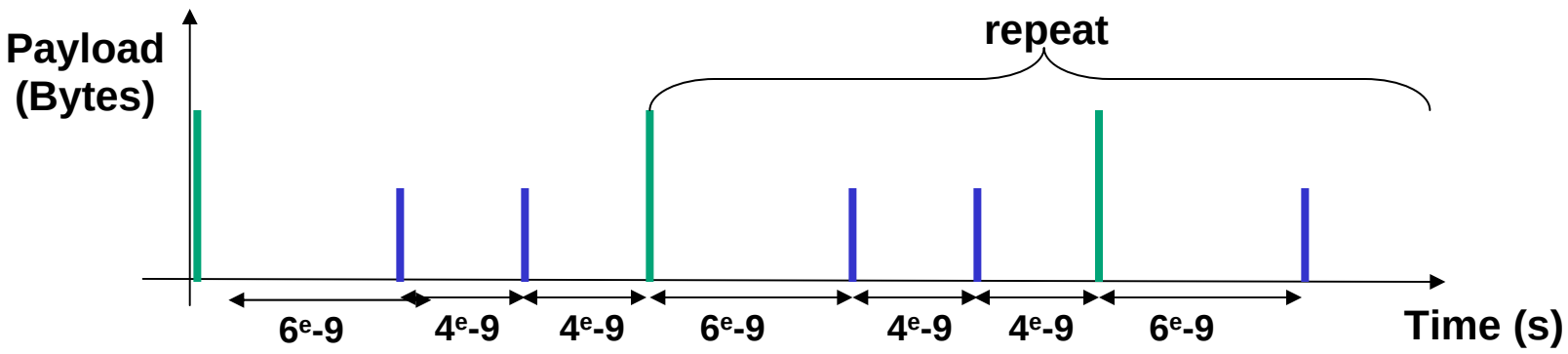
Data Flow Stress

- **IP traffic are modelized at transaction level.**
- **Uses store, load, posted store.**
  - A set of multiple transactions will create a trafic pattern wich is repeated until the simulation ended

Ex: Store(32)/6e-9 + Load(16)/4e-9 * 2



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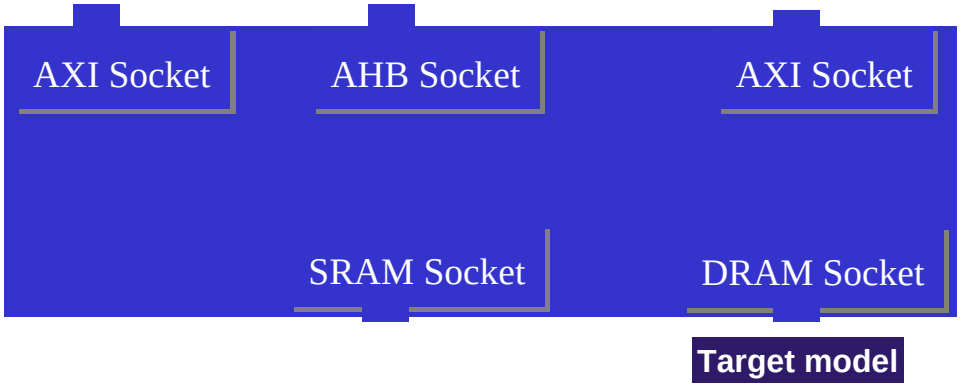
NoCexplorer view

- **Stress definition for a 1600x1200 video flow**
  - Doing 48 bytes stores (16 pixels) every 64ns
  - A line is composed of 100 accesses (1600 pixels)
  - Line frequency is 75kHz (every 13us)
  - A Frame is composed of 1200 lines
  - Frame frequency is 60Hz (every 16ms)

```
Class myFlow(Flow):
            initiator  = myIfce.AXI_Socket
            target     = myIfce.DRAM_Socket
            stress     = ((Store(48)/64e-9*100/13e
            depth      =
            efficiency =
```

Stress = ((Store(48) / 64e-9) * 100 / 13e-6 * 1200 / 16e-3)




```
class myIfce(NocInterface):
            class AXI_Socket(myAxiSocket)   : pass
            class DRAM_Socket(myDramSocket): pass
…
```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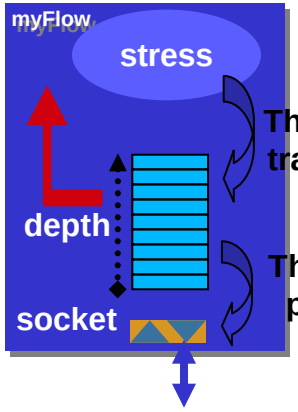
Data flow Efficiency modeling

- **Depth is the size of the IP FIFO modeled**
- **What if the FIFO is full?**
  - Then, the stress gets stall
- **A 100% efficiency targeted for a flow means that it will be never stalled.**
- **If a stress which has 70% of efficiency means that it was stalled 30% of the simulation time.**
- **Comparison between simulated and targeted efficiency will constitute information on the quality of QoS Dimensions**

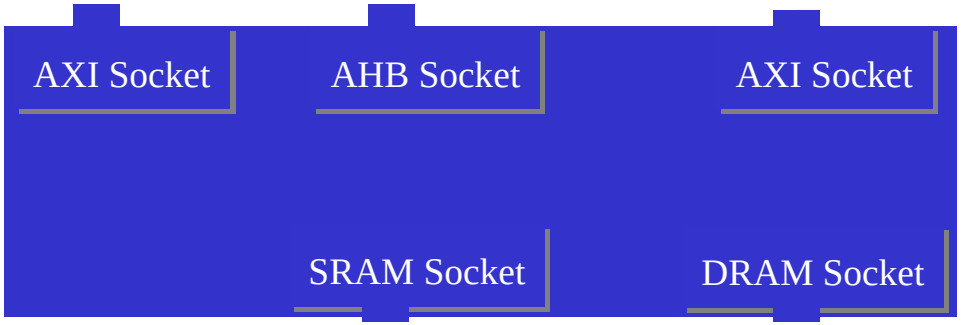
```
Class myFlow(Flow):
        initiator  = myIfce.AXI_Socket
        target     = myIfce.DRAM_Socket
        stress     = ((Store(48)/64e-9*100/13e-6*126
        depth      = 256
        efficiency = 0.7
```



The stress deposits the transaction in the FIFO

The socket sends/receives packets to/from the NoC

```
class myIfce(NocInterface):
            class AXI_Socket(myAxiSocket)   : pass
            class DRAM_Socket(myDramSocket): pass
…
```



Target model

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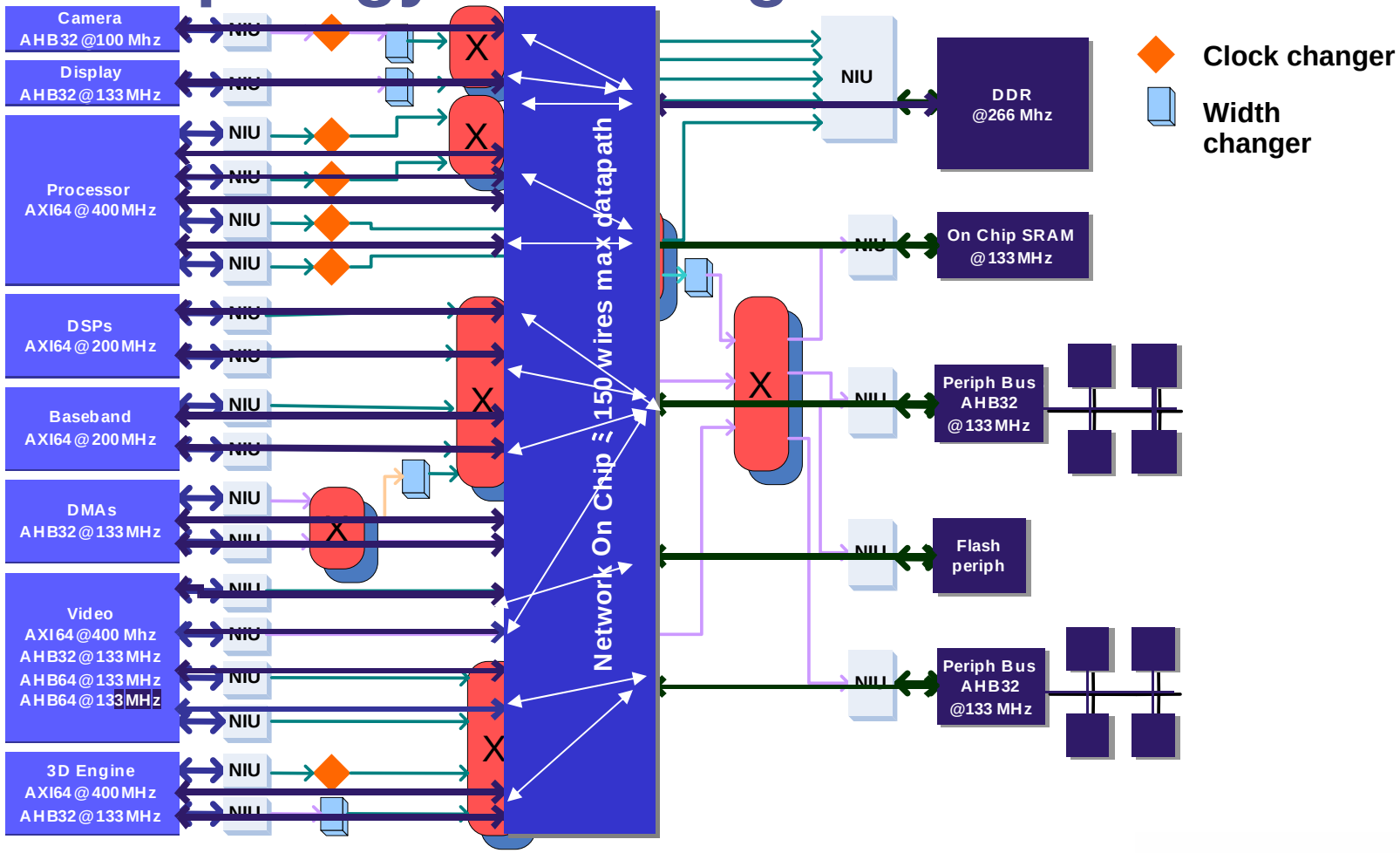
NoC topology modeling



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Architecture exploration - no QoS

NoCexplorer (/disk056/gilles/BASE/DACdemoTest/base/customers/demos/dac2006/suite/Noc.py)

File Tools Edit Help

Scenario : step1 | Simulation Time : 2e-04 | Seed : 1151919724

Sockets | Flows | Links

Name	Initiator	Target	Depth	Targ. B/W	Act. B/W	Req. Efficiency	Act. Efficiency	Full Latency	Socket Latency	Fifo level
cam	CAM	SDRAM	256.0 B	150.0 MB/s	149.9 MB/s	100.0 %	100.0 %	293.6 ns / 519.3 ns	159.1 ns / 375.6 ns	44.0 B / 96.0 B
cell1_sdram	BB1	SDRAM	256.0 B	40.0 MB/s	39.8 MB/s	100.0 %	100.0 %	1.2 us / 1.5 us	403.7 ns / 1.3 us	47.0 B / 64.0 B
cell2_sdram	BB2	SDRAM	64.0 B	10.0 MB/s	10.0 MB/s	100.0 %	100.0 %	821.0 ns / 1.6 us	820.8 ns / 1.6 us	8.2 B / 32.0 B
cpuD	CPUD	SDRAM	32.0 B	80.5 MB/s	21.0 MB/s	65.0 %	21.2 %	2.6 us / 5.9 us	1.5 us / 3.5 us	55.6 B / 64.0 B
cpuI	CPUI	SDRAM	32.0 B	161.0 MB/s	7.7 MB/s	65.0 %	5.3 %	7.8 us / 19.1 us	4.1 us / 11.9 us	62.3 B / 64.0 B
cpuT	CPUT	SDRAM	32.0 B	17.2 MB/s	5.8 MB/s	65.0 %	41.6 %	7.4 us / 20.3 us	4.3 us / 12.9 us	44.7 B / 64.0 B
disp	DISP	SDRAM	256.0 B	150.0 MB/s	150.1 MB/s	100.0 %	100.0 %	290.3 ns / 483.2 ns	290.0 ns / 483.2 ns	43.6 B / 128.0 B
dma1_per1	DMA1	PER1	32.0 B	20.0 MB/s	20.0 MB/s	100.0 %	100.0 %	29.2 ns / 82.7 ns	24.4 ns / 60.2 ns	583.5 mB / 16.0 B
dma1_per2	DMA1	PER2	32.0 B	5.0 MB/s	5.0 MB/s	100.0 %	100.0 %	36.5 ns / 75.2 ns	31.0 ns / 60.2 ns	184.1 mB / 16.0 B
dma2_sdram	DMA2	SDRAM	128.0 B	50.0 MB/s	49.9 MB/s	100.0 %	100.0 %	795.2 ns / 1.4 us	587.7 ns / 1.3 us	39.7 B / 96.0 B
dma2_sram	DMA2	SRAM	128.0 B	10.0 MB/s	10.0 MB/s	100.0 %	100.0 %	534.7 ns / 1.4 us	50.3 ns / 109.0 ns	5.3 B / 16.0 B
dsp1	DSP1	SDRAM	16.0 B	40.0 MB/s	3.7 MB/s	70.0 %	13.8 %	7.8 us / 18.8 us	4.2 us / 9.9 us	29.5 B / 32.0 B
dsp2	DSP2	SDRAM	16.0 B	40.0 MB/s	3.8 MB/s	70.0 %	10.5 %	7.7 us / 21.3 us	4.1 us / 12.8 us	30.3 B / 32.0 B
rdr1	DDD2	SDRAM	1.6 kB	53.8 MB/s	27.9 MB/s	65.0 %	40.6 %	46.9 us / 60.1 us	306.7 ns / 1.3 us	1.5 kB / 1.6 kB
rdr2	DDD2	SDRAM	1.6 kB	53.8 MB/s	27.8 MB/s	65.0 %	40.6 %	47.5 us / 60.3 us	279.9 ns / 1.3 us	1.5 kB / 1.6 kB
tmd_sdram_cache	VIDEO3	SDRAM	256.0 B	50.0 MB/s	49.9 MB/s	100.0 %	100.0 %	670.9 ns / 1.4 us	328.7 ns / 859.2 ns	33.7 B / 128.0 B
tmd_sdram_word	VIDEO3	SDRAM	256.0 B	10.0 MB/s	9.9 MB/s	100.0 %	100.0 %	1.3 us / 2.7 us	1.1 us / 2.7 us	13.3 B / 32.0 B

Full Latency | Socket Latency | Fifo Level | Fifo Lvl /t | Latency /t | Throughput /t

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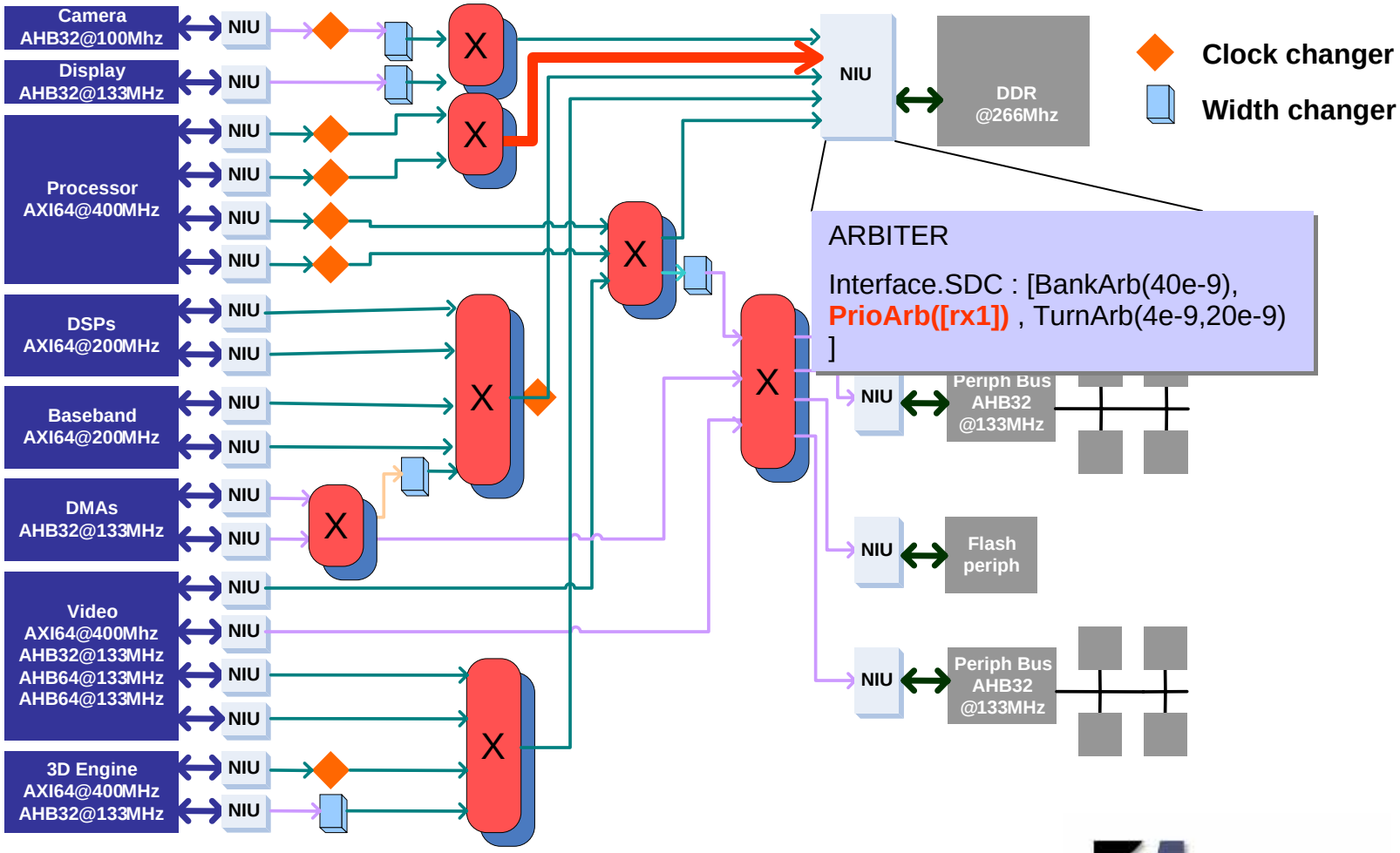
QoS added - CPU Latency



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Architecture exploration cont's

NoCexplorer (/disk056/gilles/BASE/DACdemoTest/base/customers/demos/dac2006/suite/Noc.py)

File Tools Edit Help

Scenario : step2 | Simulation Time : 2e-04 | Seed : 1151919724

Sockets | Flows | Links

Name	Initiator	Target	Depth	Targ. B/W	Act. B/W	Req. Efficiency	Act. Efficiency	Full Latency	Socket Latency	Fifo level
cam	CAM	SDRAM	256.0 B	150.0 MB/s	132.5 MB/s	100.0 %	88.9 %	1.4 us / 3.7 us	386.5 ns / 1.2 us	192.1 B
cell1_sdram	BB1	SDRAM	256.0 B	40.0 MB/s	40.0 MB/s	100.0 %	100.0 %	303.7 ns / 1.4 us	300.3 ns / 1.4 us	12.1 E
cell2_sdram	BB2	SDRAM	64.0 B	10.0 MB/s	10.0 MB/s	100.0 %	100.0 %	343.6 ns / 1.3 us	343.6 ns / 1.3 us	3.4 E
cpuD	CPUD	SDRAM	32.0 B	80.5 MB/s	66.6 MB/s	65.0 %	72.8 %	320.0 ns / 1.5 us	315.0 ns / 1.5 us	21.3 E
cpuI	CPUI	SDRAM	32.0 B	161.0 MB/s	150.1 MB/s	65.0 %	90.7 %	102.3 ns / 382.1 ns	100.8 ns / 382.1 ns	15.4 E
cpuT	CPUT	SDRAM	32.0 B	17.2 MB/s	16.0 MB/s	65.0 %	97.0 %	127.2 ns / 297.0 ns	119.9 ns / 274.0 ns	2.0 E
disp	DISP	SDRAM	256.0 B	150.0 MB/s	149.8 MB/s	100.0 %	100.0 %	386.4 ns / 976.2 ns	385.4 ns / 976.2 ns	58.0 B
dma1_per1	DMA1	PER1	32.0 B	20.0 MB/s	20.0 MB/s	100.0 %	100.0 %	29.2 ns / 82.7 ns	24.4 ns / 60.2 ns	583.5 mE
dma1_per2	DMA1	PER2	32.0 B	5.0 MB/s	5.0 MB/s	100.0 %	100.0 %	36.5 ns / 75.2 ns	31.0 ns / 60.2 ns	184.1 mE
dma2_sdram	DMA2	SDRAM	128.0 B	50.0 MB/s	50.1 MB/s	100.0 %	100.0 %	336.5 ns / 1.4 us	313.9 ns / 1.3 us	16.9 E
dma2_sram	DMA2	SRAM	128.0 B	10.0 MB/s	10.0 MB/s	100.0 %	100.0 %	170.9 ns / 1.4 us	138.4 ns / 1.2 us	1.7 E
dsp1	DSP1	SDRAM	16.0 B	40.0 MB/s	32.5 MB/s	70.0 %	91.1 %	99.8 ns / 493.3 ns	93.0 ns / 394.4 ns	3.2 E
dsp2	DSP2	SDRAM	16.0 B	40.0 MB/s	37.3 MB/s	70.0 %	89.9 %	97.1 ns / 465.9 ns	90.1 ns / 378.3 ns	3.6 E
rdr1	DDD2	SDRAM	1.6 kB	53.8 MB/s	49.7 MB/s	65.0 %	66.9 %	24.4 us / 35.5 us	298.6 ns / 1.0 us	1.3 kB
rdr2	DDD2	SDRAM	1.6 kB	53.8 MB/s	48.0 MB/s	65.0 %	66.8 %	26.0 us / 35.7 us	302.9 ns / 1.0 us	1.4 kB
tmd_sdram_cache	VIDEO3	SDRAM	256.0 B	50.0 MB/s	49.9 MB/s	100.0 %	100.0 %	347.5 ns / 1.3 us	339.1 ns / 1.3 us	17.6 B
tmd_sdram_word	VIDEO3	SDRAM	256.0 B	10.0 MB/s	10.0 MB/s	100.0 %	100.0 %	267.4 ns / 1.2 us	262.4 ns / 1.2 us	2.7 E

Full Latency | Socket Latency | Fifo Level | Fifo Lvl /t | Latency /t | Throughput /t

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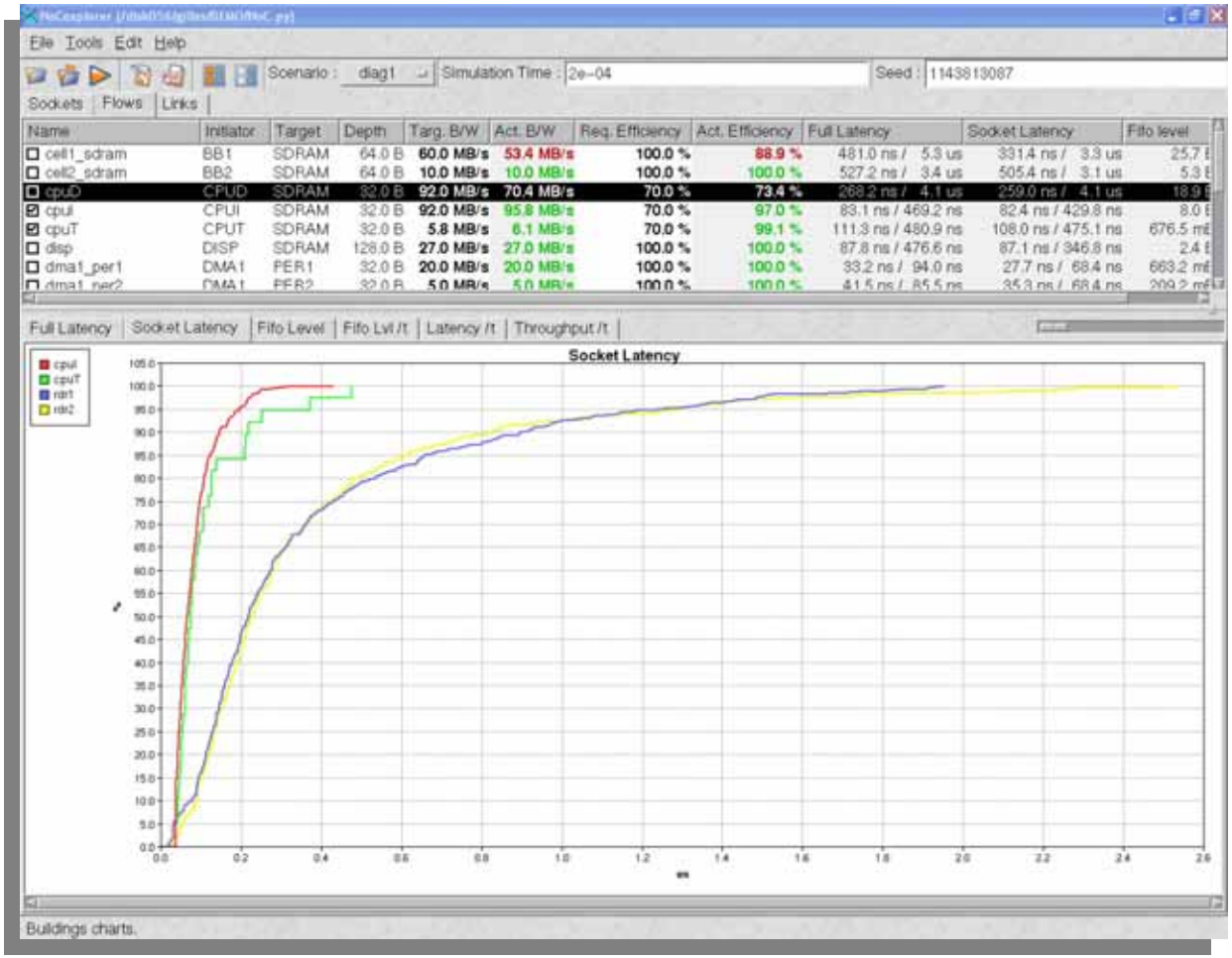
Latency First results



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Bandwidth First Results

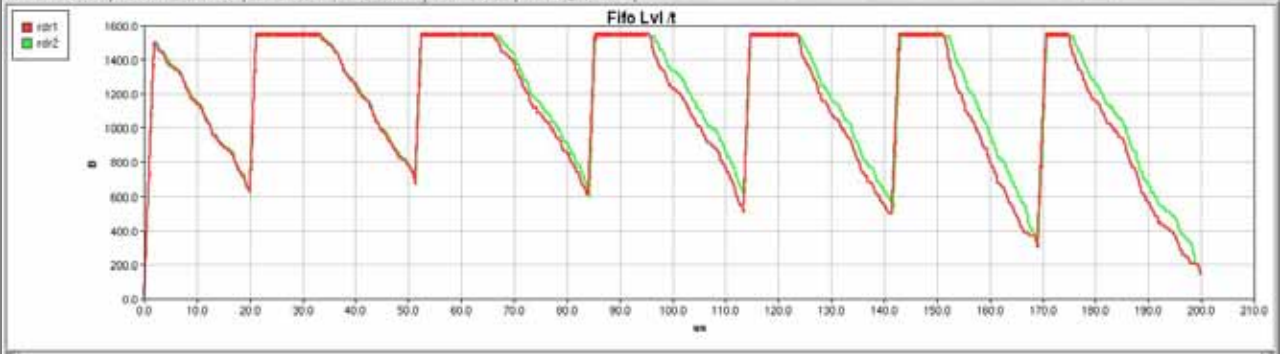
File Tools Edit Help

Scenario : diag1 Simulation Time : 2e-04 Seed : 1143813087

Sockets | Flows | Links

Name	Initiator	Target	Depth	Targ. B/W	Act. B/W	Req. Efficiency	Act. Efficiency	Full Latency	Socket Latency	Fifo level
cell1_sdram	BB1	SDRAM	64.0 B	60.0 MB/s	59.9 MB/s	100.0 %	99.9 %	180.9 ns / 1.2 us	174.9 ns / 1.2 us	10.9 B / 80.0 B
cell2_sdram	BB2	SDRAM	64.0 B	10.0 MB/s	10.0 MB/s	100.0 %	100.0 %	226.1 ns / 730.2 ns	226.0 ns / 730.2 ns	2.3 B / 16.0 B
cpuD	CPUD	SDRAM	32.0 B	92.0 MB/s	86.7 MB/s	70.0 %	82.1 %	165.9 ns / 614.8 ns	163.7 ns / 611.9 ns	14.4 B / 64.0 B
cpuI	CPUI	SDRAM	32.0 B	92.0 MB/s	88.3 MB/s	70.0 %	96.1 %	108.1 ns / 922.4 ns	106.6 ns / 786.2 ns	9.5 B / 64.0 B
cpuT	CPUT	SDRAM	32.0 B	5.8 MB/s	6.1 MB/s	70.0 %	98.5 %	197.2 ns / 821.6 ns	192.0 ns / 815.9 ns	1.2 B / 64.0 B
disp	DISP	SDRAM	128.0 B	27.0 MB/s	27.0 MB/s	100.0 %	100.0 %	109.2 ns / 798.8 ns	107.7 ns / 633.6 ns	3.0 B / 32.0 B
dma1_per1	DMA1	PER1	32.0 B	20.0 MB/s	20.0 MB/s	100.0 %	100.0 %	33.2 ns / 94.0 ns	27.7 ns / 68.4 ns	663.2 mB / 16.0 B
dma1_per2	DMA1	PER2	32.0 B	5.0 MB/s	5.0 MB/s	100.0 %	100.0 %	41.5 ns / 85.5 ns	35.3 ns / 68.4 ns	209.2 mB / 16.0 B
dma2_sdram	DMA2	SDRAM	32.0 B	20.0 MB/s	20.0 MB/s	100.0 %	100.0 %	210.8 ns / 808.6 ns	209.6 ns / 808.6 ns	4.2 B / 32.0 B
dma2_sram	DMA2	SRAM	32.0 B	20.0 MB/s	20.0 MB/s	100.0 %	100.0 %	238.7 ns / 851.4 ns	158.4 ns / 700.3 ns	4.8 B / 32.0 B
dsp1	DSP1	SDRAM	16.0 B	46.0 MB/s	39.3 MB/s	70.0 %	78.6 %	211.1 ns / 1.1 us	199.8 ns / 1.1 us	8.3 B / 32.0 B
dsp2	DSP2	SDRAM	16.0 B	46.0 MB/s	36.9 MB/s	70.0 %	79.2 %	215.8 ns / 1.4 us	202.3 ns / 1.3 us	8.0 B / 32.0 B
hw1	VIDEO1	SDRAM	64.0 B	50.0 MB/s	50.0 MB/s	100.0 %	100.0 %	134.3 ns / 650.0 ns	133.9 ns / 650.0 ns	6.7 B / 48.0 B
hw2	VIDEO2	SDRAM	64.0 B	50.0 MB/s	49.9 MB/s	100.0 %	100.0 %	224.0 ns / 768.4 ns	223.2 ns / 768.4 ns	11.2 B / 48.0 B
rdr1	DDD2	SDRAM	1.5 kB	53.8 MB/s	53.0 MB/s	65.0 %	73.6 %	21.0 us / 33.3 us	269.3 ns / 867.9 ns	1.1 kB / 1.6 kB
rdr2	DDD2	SDRAM	1.5 kB	53.8 MB/s	53.0 MB/s	65.0 %	73.5 %	21.9 us / 33.3 us	271.9 ns / 1.3 us	1.2 kB / 1.6 kB
tmd_sdram_cache	VIDEO3	SDRAM	128.0 B	50.0 MB/s	50.6 MB/s	100.0 %	100.0 %	200.3 ns / 642.1 ns	198.8 ns / 642.1 ns	10.1 B / 128.0 B
tmd_sdram_word	VIDEO3	SDRAM	16.0 B	10.0 MB/s	10.0 MB/s	100.0 %	100.0 %	116.8 ns / 720.3 ns	115.8 ns / 714.6 ns	1.2 B / 16.0 B

Full Latency | Socket Latency | Fifo Level | Fifo Lvl /t | Latency /t | Throughput /t



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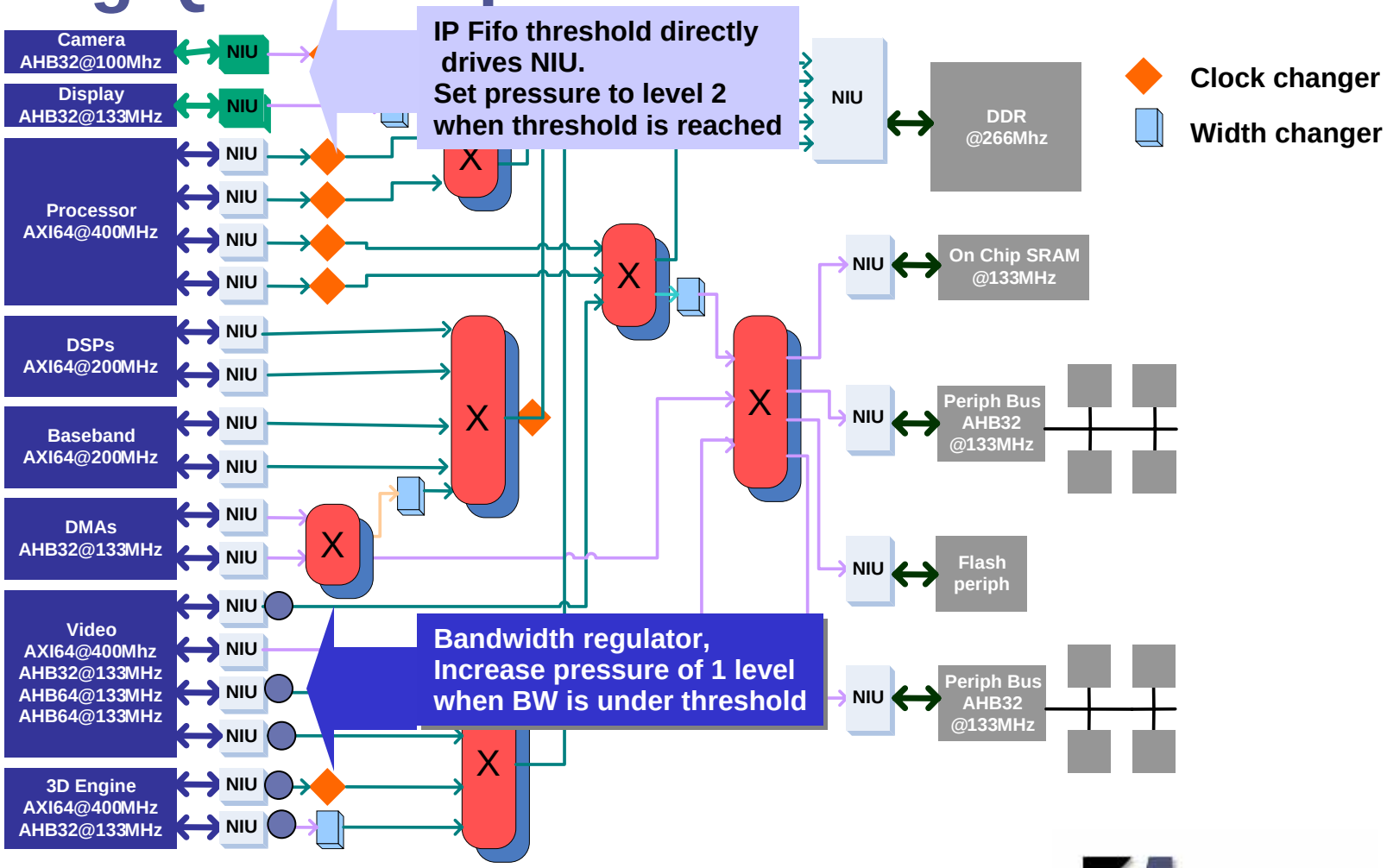
Adding QoS component



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Architecture exploration completeness

NoCexplorer (/disk056/gilles/BASE/DACdemoTest/base/customers/demos/dac2006/suite/Noc.py)

File Tools Edit Help

Scenario : step3 | Simulation Time : 2e-04 | Seed : 1151919724

Sockets | Flows | Links

Name	Initiator	Target	Depth	Targ. B/W	Act. B/W	Req. Efficiency	Act. Efficiency	Full Latency	Socket Latency	Fifo level
cam	CAM	SDRAM	256.0 B	150.0 MB/s	149.8 MB/s	100.0 %	100.0 %	176.5 ns / 543.1 ns	171.3 ns / 543.1 ns	26.5 E
cell1_sdram	BB1	SDRAM	256.0 B	40.0 MB/s	40.0 MB/s	100.0 %	100.0 %	405.5 ns / 1.4 us	395.0 ns / 1.4 us	16.2 E
cell2_sdram	BB2	SDRAM	64.0 B	10.0 MB/s	10.0 MB/s	100.0 %	100.0 %	448.3 ns / 1.5 us	448.3 ns / 1.5 us	4.5 E
cpuD	CPUD	SDRAM	32.0 B	80.5 MB/s	58.6 MB/s	65.0 %	68.4 %	403.6 ns / 1.8 us	401.2 ns / 1.8 us	23.6 E
cpuI	CPUI	SDRAM	32.0 B	161.0 MB/s	125.9 MB/s	65.0 %	74.7 %	209.9 ns / 1.7 us	196.6 ns / 1.7 us	26.4 E
cpuT	CPUT	SDRAM	32.0 B	17.2 MB/s	13.1 MB/s	65.0 %	93.7 %	347.4 ns / 1.8 us	293.8 ns / 1.6 us	4.6 E
disp	DISP	SDRAM	256.0 B	150.0 MB/s	150.1 MB/s	100.0 %	100.0 %	211.7 ns / 416.4 ns	211.5 ns / 416.4 ns	31.8 E
dma1_per1	DMA1	PER1	32.0 B	20.0 MB/s	20.0 MB/s	100.0 %	100.0 %	29.2 ns / 82.7 ns	24.4 ns / 60.2 ns	583.5 mE
dma1_per2	DMA1	PER2	32.0 B	5.0 MB/s	5.0 MB/s	100.0 %	100.0 %	36.5 ns / 75.2 ns	31.0 ns / 60.2 ns	184.1 mE
dma2_sdram	DMA2	SDRAM	128.0 B	50.0 MB/s	49.9 MB/s	100.0 %	100.0 %	445.3 ns / 1.6 us	407.6 ns / 1.5 us	22.3 E
dma2_sram	DMA2	SRAM	128.0 B	10.0 MB/s	10.0 MB/s	100.0 %	100.0 %	250.3 ns / 1.3 us	194.5 ns / 1.3 us	2.5 E
dsp1	DSP1	SDRAM	16.0 B	40.0 MB/s	32.3 MB/s	70.0 %	77.9 %	248.5 ns / 1.5 us	223.2 ns / 1.3 us	8.0 E
dsp2	DSP2	SDRAM	16.0 B	40.0 MB/s	28.8 MB/s	70.0 %	82.5 %	225.1 ns / 1.2 us	198.0 ns / 964.0 ns	6.5 E
rdr1	DDD2	SDRAM	1.6 kB	53.8 MB/s	53.8 MB/s	65.0 %	83.0 %	20.1 us / 32.2 us	249.8 ns / 1.3 us	1.1 kB
rdr2	DDD2	SDRAM	1.6 kB	53.8 MB/s	53.8 MB/s	65.0 %	83.0 %	20.6 us / 32.2 us	254.1 ns / 1.5 us	1.1 kB
tmd_sdram_cache	VIDEO3	SDRAM	256.0 B	50.0 MB/s	50.6 MB/s	100.0 %	100.0 %	249.3 ns / 818.4 ns	236.6 ns / 818.4 ns	12.6 B
tmd_sdram_word	VIDEO3	SDRAM	256.0 B	10.0 MB/s	10.0 MB/s	100.0 %	100.0 %	374.8 ns / 1.6 us	373.6 ns / 1.6 us	3.7 E

Full Latency | Socket Latency | Fifo Level | Fifo Lvl /t | Latency /t | Throughput /t

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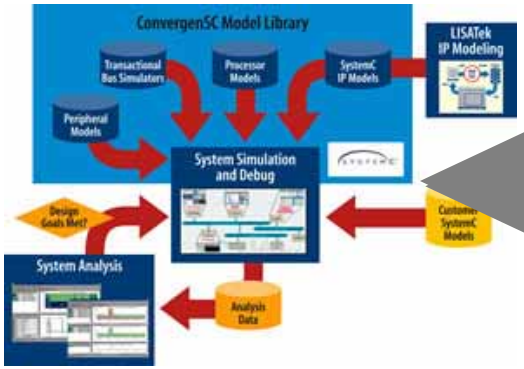
NoC views Exportation to ESL world

QuickTime™ and a
TIFF (Uncompressed) decompressor
are needed to see this picture.



NoC
ESL views export

QuickTime™ and a
TIFF (Uncompressed) decompressor
are needed to see this picture.

SoC Designer

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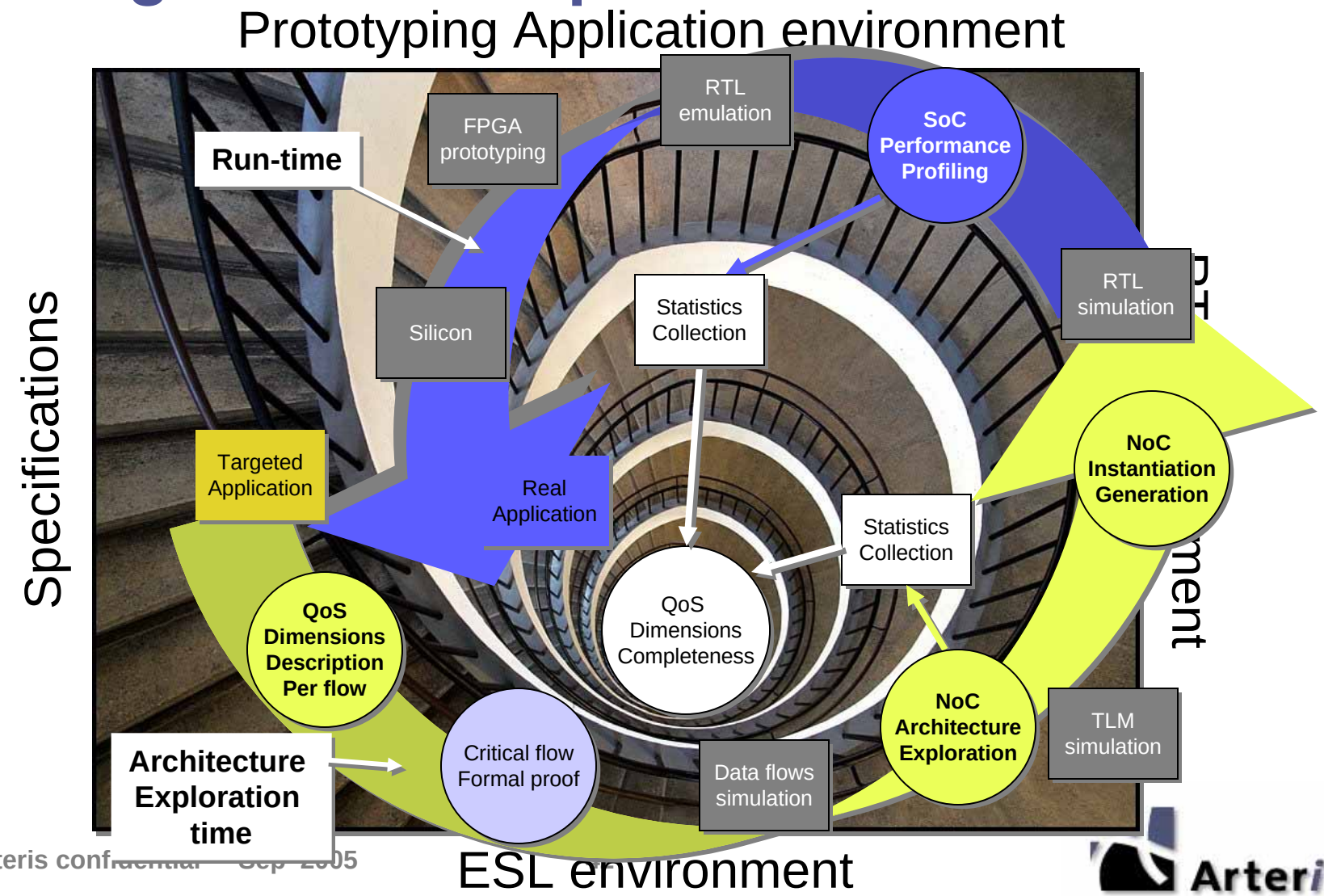
NoC generation & performance monitoring



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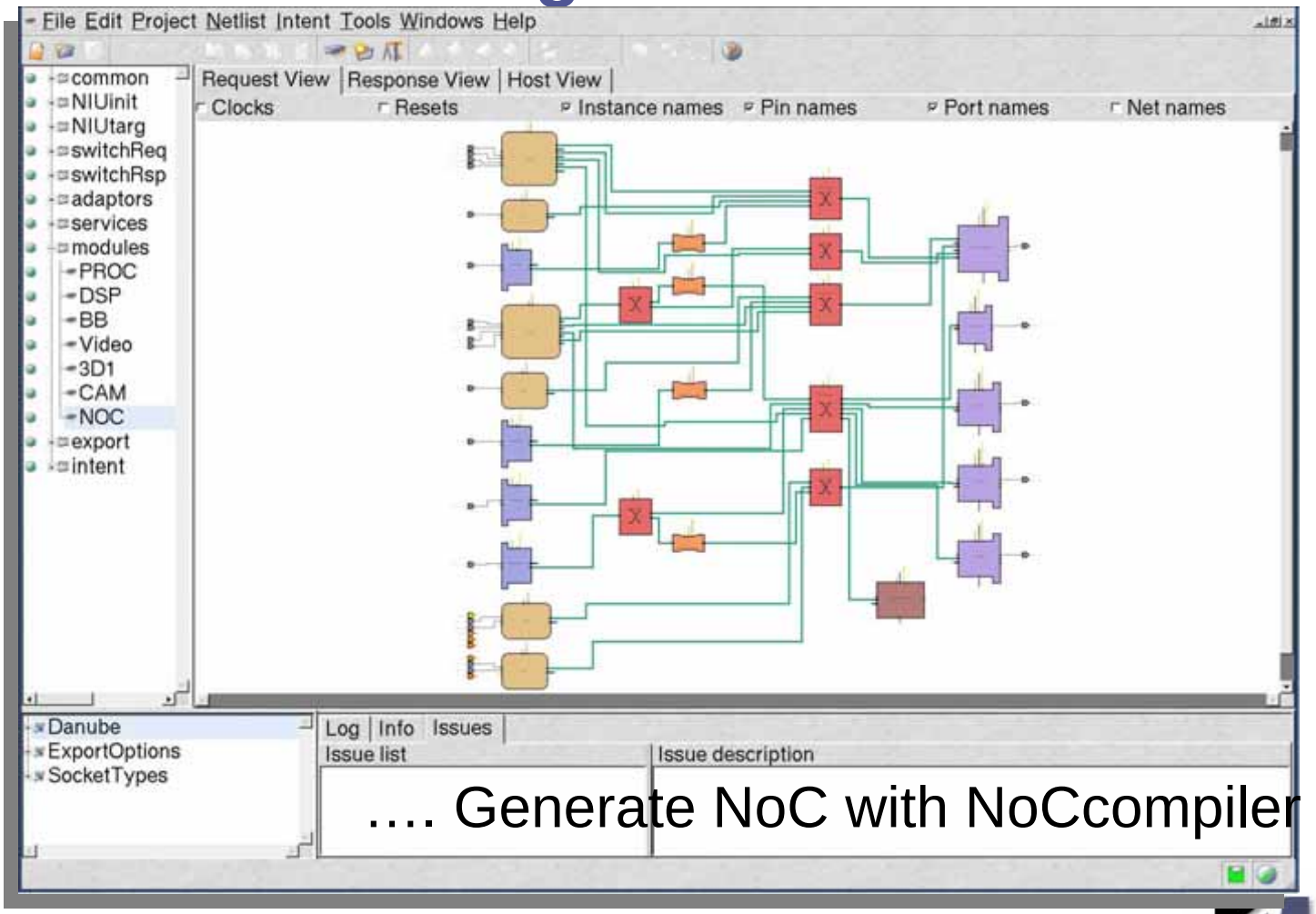
NoC RTL views generation



…. Generate NoC with NoCcompiler

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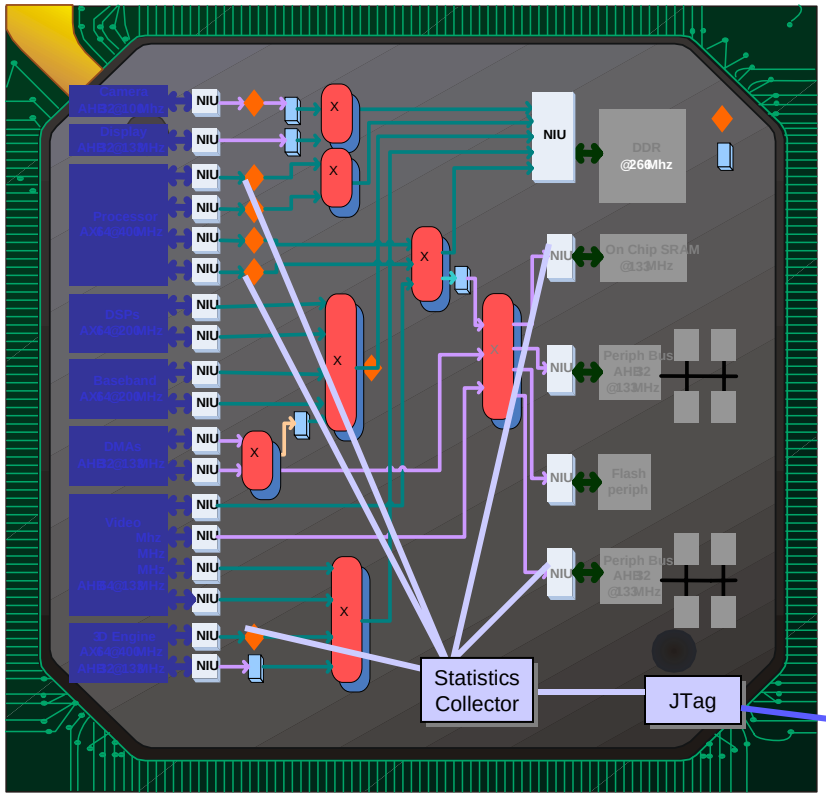
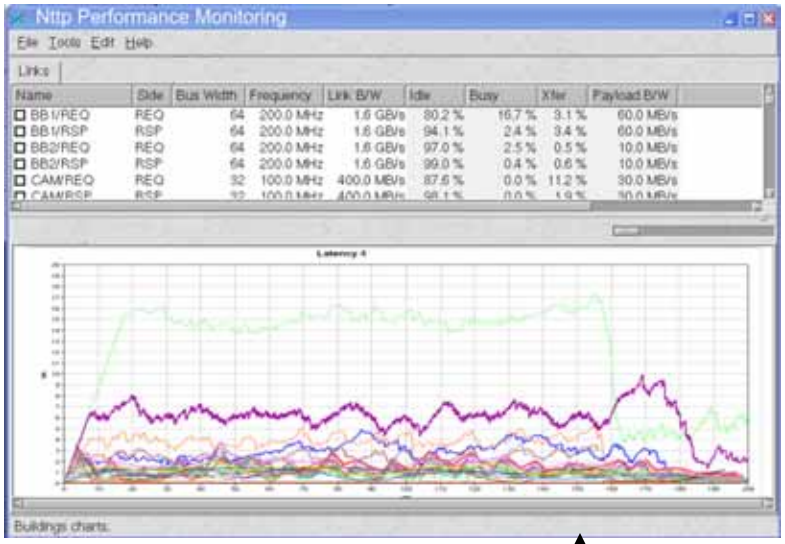
QoS Dimensions Monitoring





FS2
API

… using NoCprofiler

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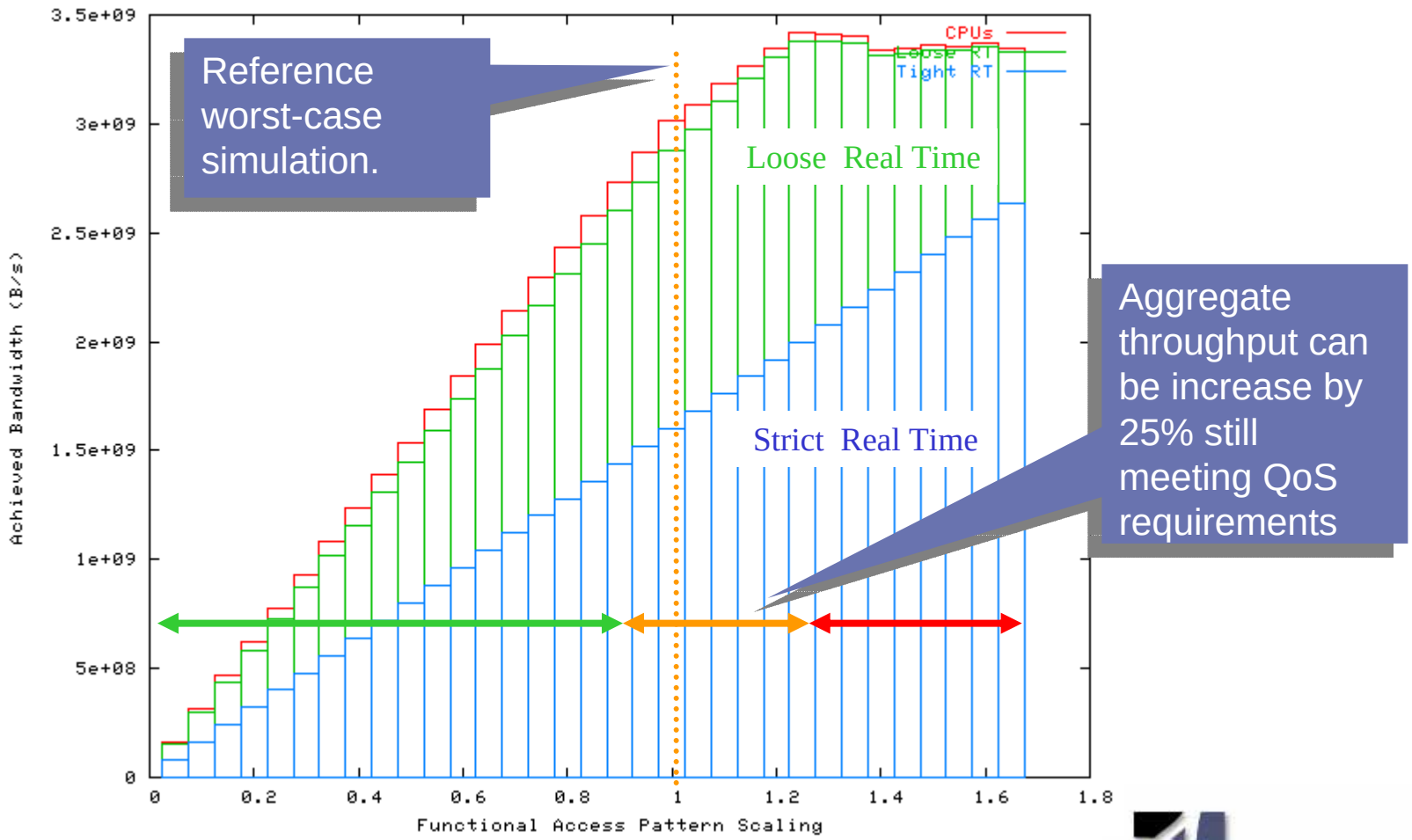
Optimized architecture



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SoC Results

- Improve Wire efficiency by x4 (40% wires saving)
- Reduce gates count by 2 (180Kgates)
- Scale with performance roadmap
- Improve Design Productivity
- Improve Product Quality
- Improve Power management

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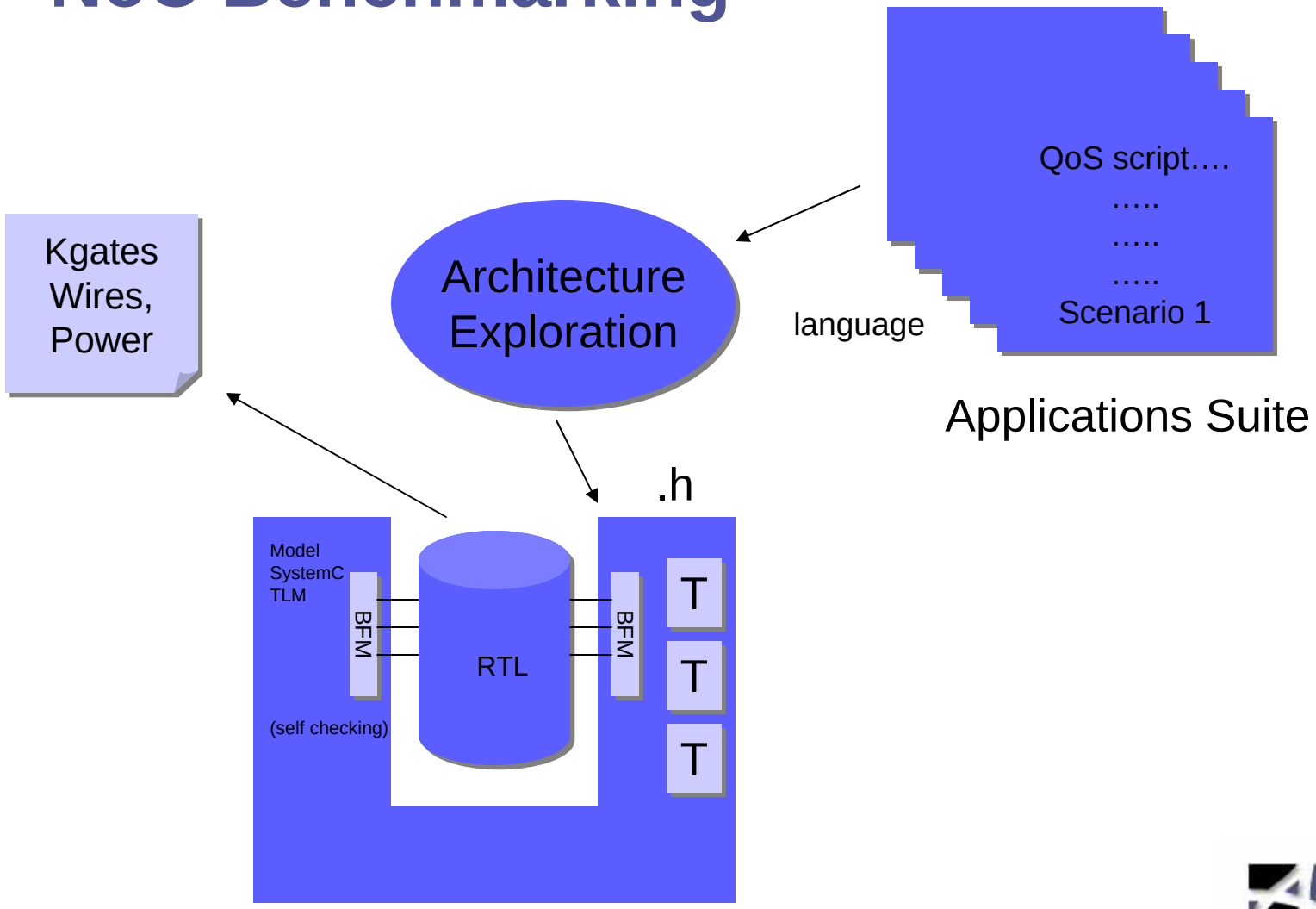
Next

- **Improve Description language Productivity**
- **Increase implementation views**
  - Architectural models, floor-planning, Gates & Power estimates
- **Performance Monitoring directly coupled to architecture exploration tools**
- **Support methodology for NoC Benchmarking**

NoC Benchmarking



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Conclusion

- **Adaptive network communication system is the solution to scale**
- **QoS dimensions profiling at architecture exploration time and run time**
- **ARTERIS provides an innovative Adaptive Network Information System environment to solve this designer's challenge**

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