Programming Models and Software Architecture for MPSoC

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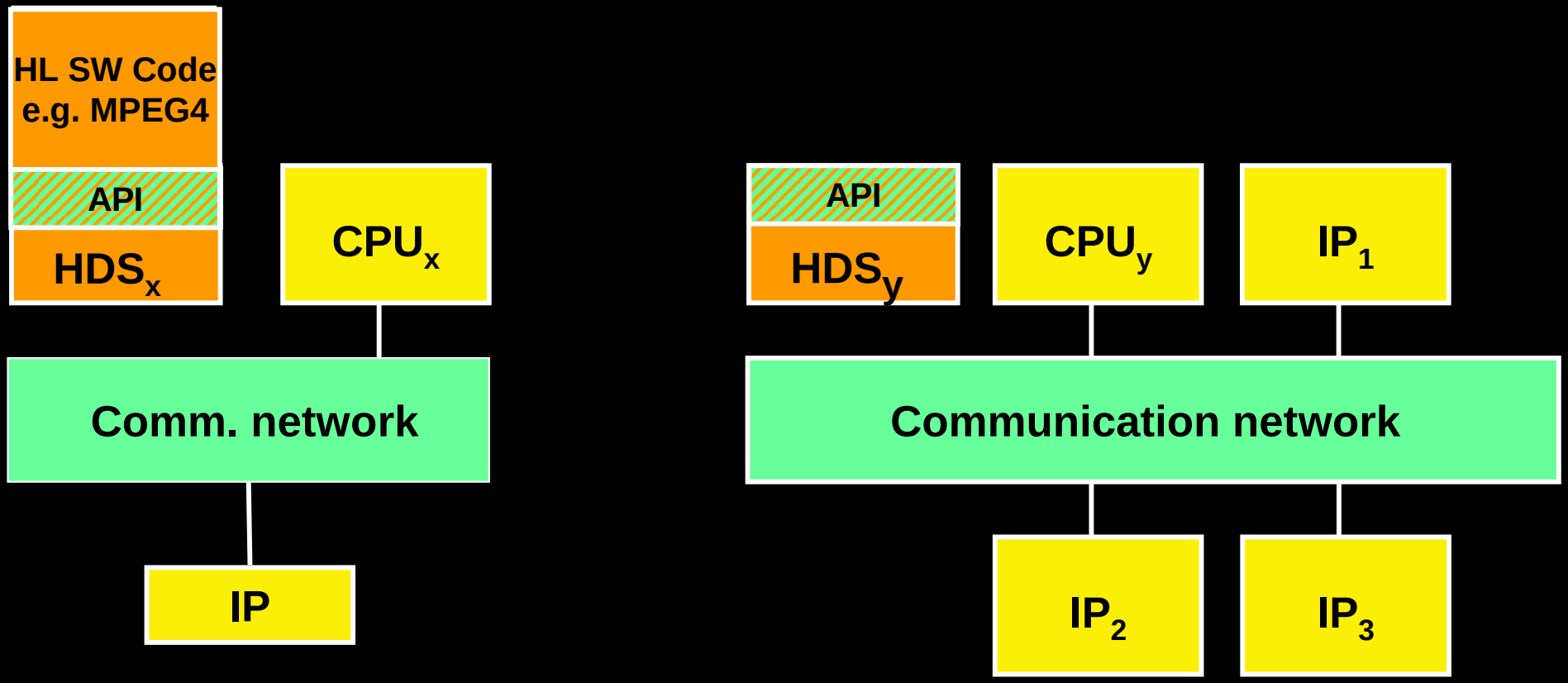
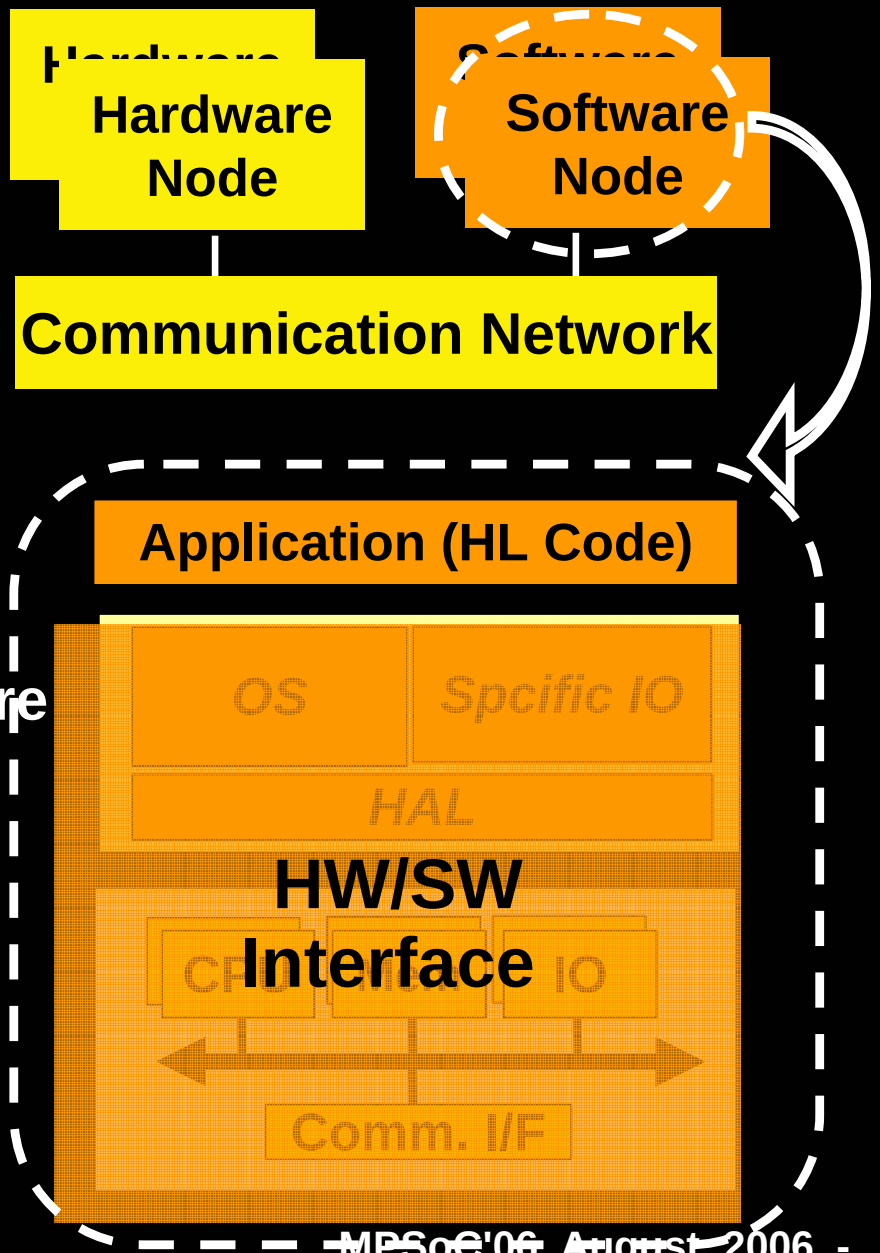
Programming Model: The Classical Solution to Abstract HW-SW Interfaces

- Abstract HW model for SW design
  - Programming language with implicit primitives (e.g. module hierarchy & threads in SystemC)
  - API (MPI, PThreads) & Simulation model (MPICH, Linux)
- Requires an additional SW layer called HW dependent SW (HDS)

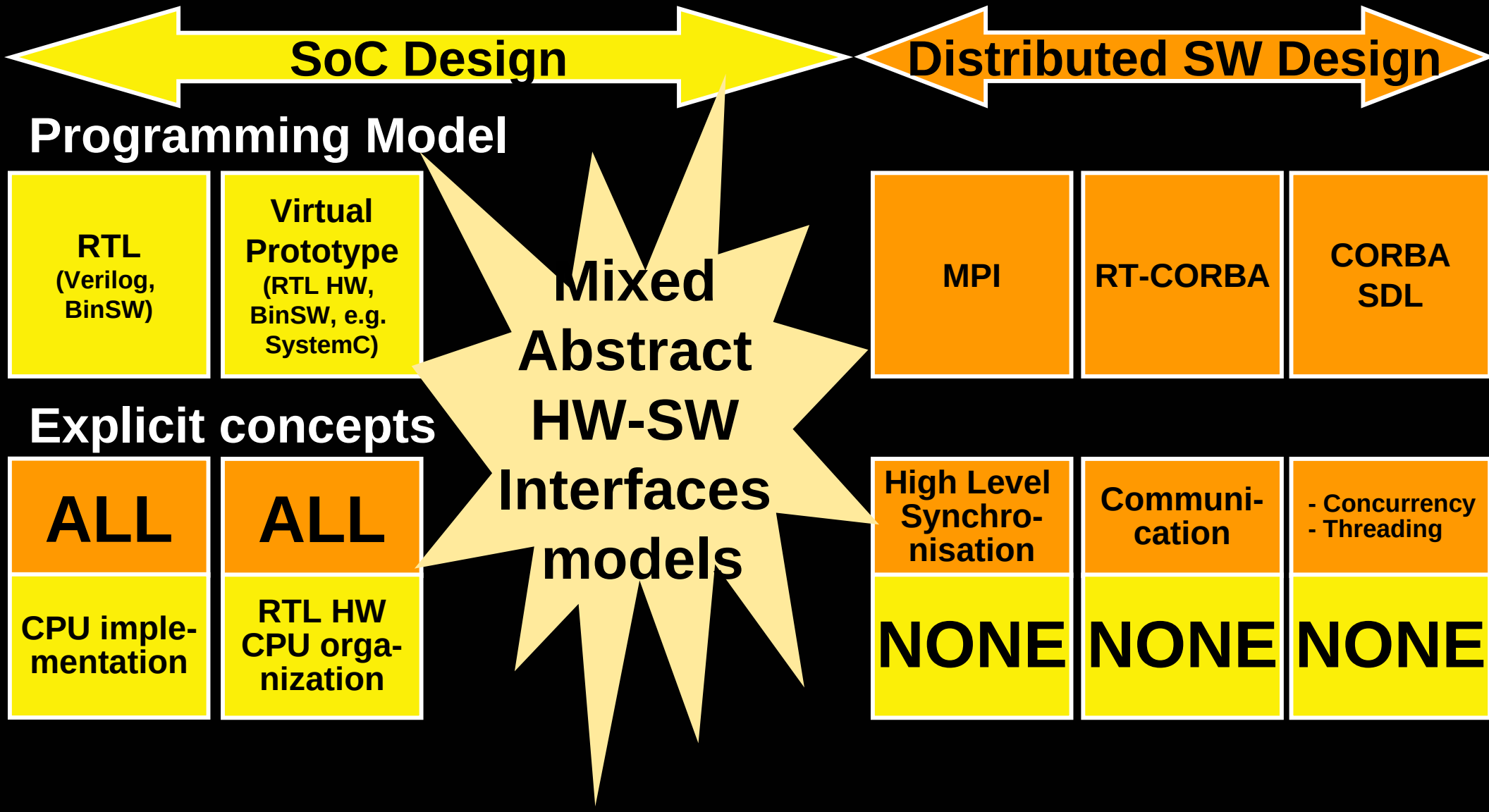


Context : Heterogeneous MPSoC

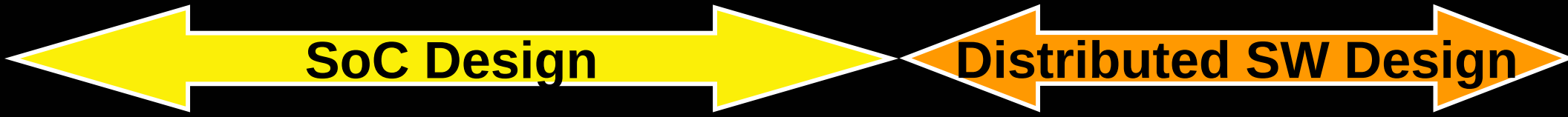
- Heterogeneous MPSoC
- software node :
  - Specific CPU subsystem
    - GPP, DSP, ASIP…
    - I/O and Memory architecture
  - Layered SW architecture
    - High level Application Code
    - HDS: Hardware dependent Software
- A Programming Model Abstracts HW-SW interfaces for SoC design
  - Specific I/O => specific API
  - HDS adapts HL SW to specific HW
  - Different abstraction levels



Parallel Programming Models: The mixed HW-SW interfaces GAP



Parallel Programming Models for MPSoC



Programming Model

RTL (Verilog, BinSW)	Virtual Prototype (RTL HW, BinSW, e.g. SystemC)	Transaction Accurate (TLM HW, TLM SW , e.g. SystemC++)	Virtual Architecture (Abstract HW, Threads, e.g. SystemC, Simulink)	MPI	RT-CORBA	CORBA SDL

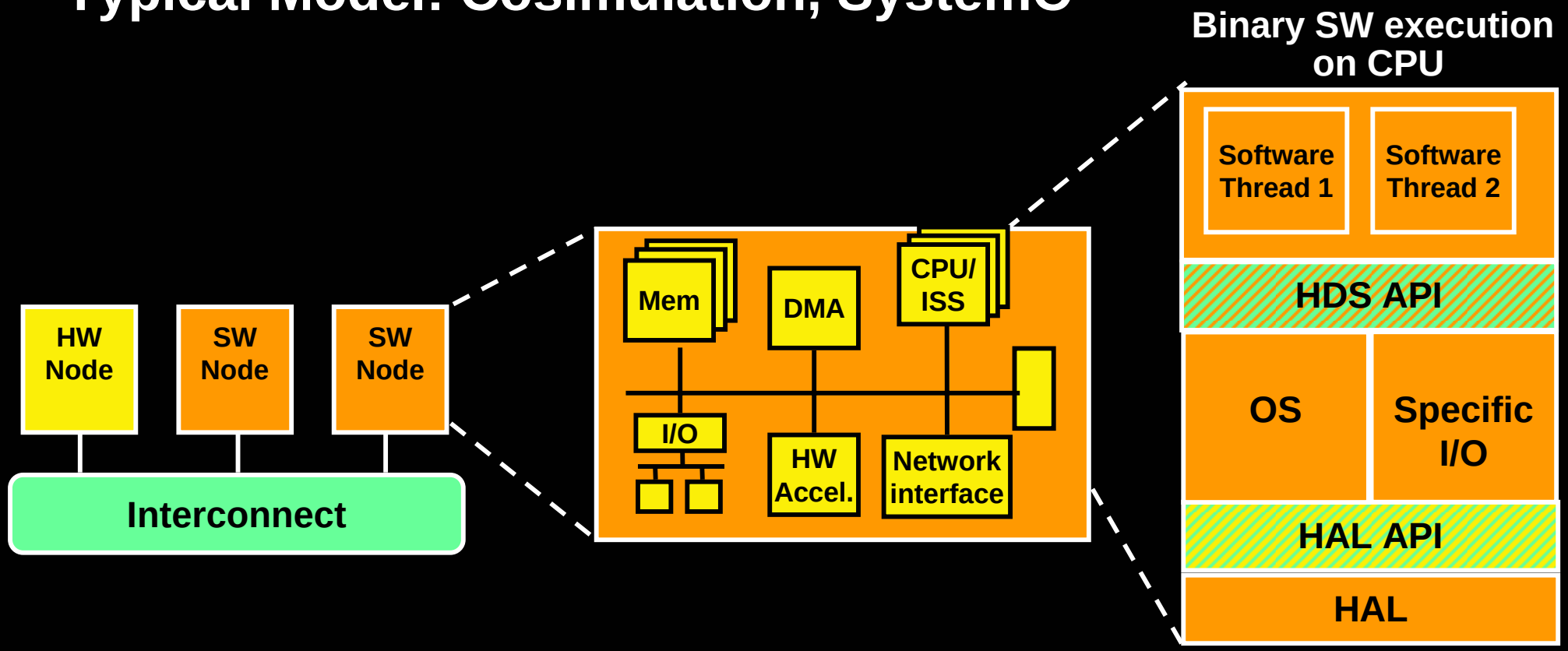
Explicit concepts

ALL	ALL	- OS - Specific I/O	Communication/ Computation Modules	Synchro-nisation	Communi-cation	- Concurrency - Threading
CPU imple-mentation	RTL HW CPU orga-nization	-CPU Subsystem - Explicit HW modules	Abstract Interconnect	NONE	NONE	NONE

- New HW-SW Abstraction levels
- Hiding CPU in addition to HW & SW

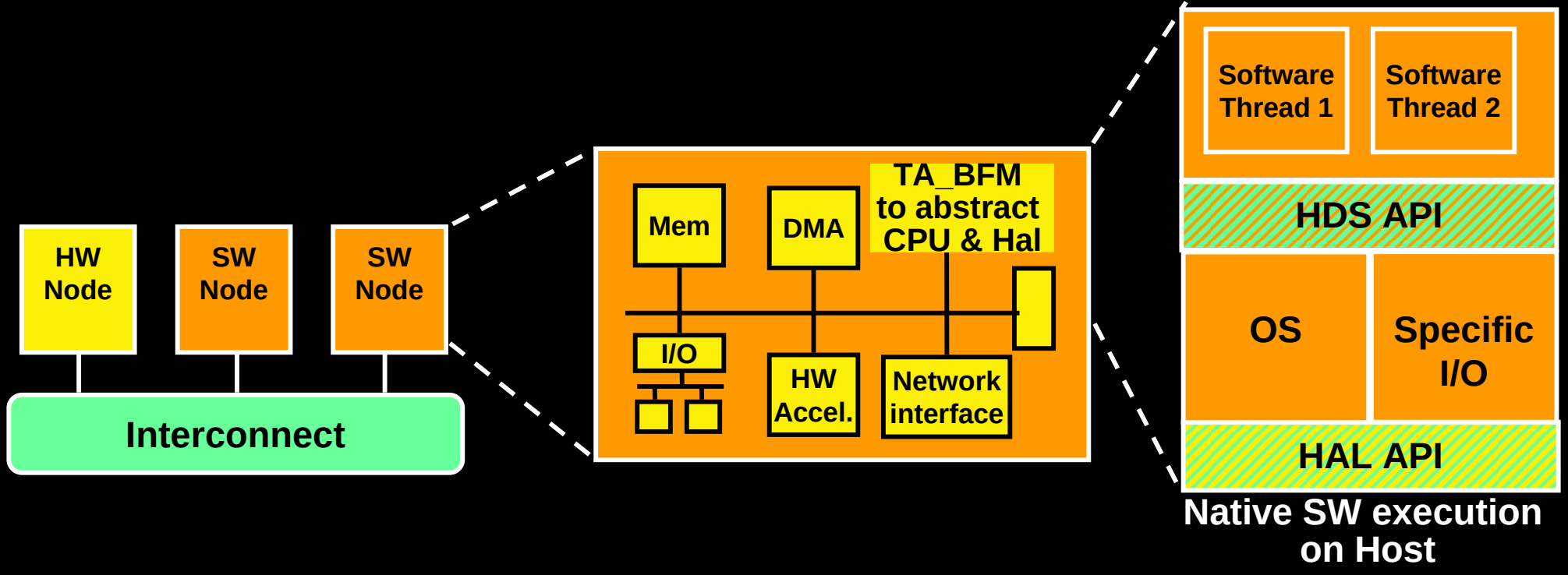
Programming Models for MPSoC Virtual Prototype

- Explicit SW (Binary)
- Explicit HW
- Implicit CPU Implementation (ISS)
- Cycle accurate Model
- Typical Model: Cosimulation, SystemC



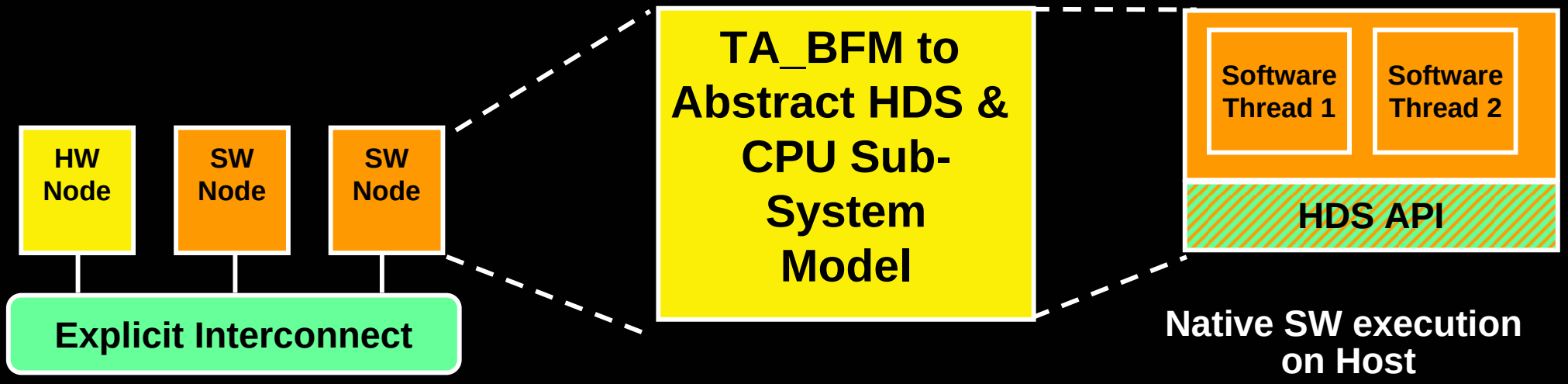
Programming Models for MPSoC Transaction Accurate model

- Explicit OS
- Explicit CPU Subsystem Architecture
- Implicit CPU/HAL (TA_BFM)
- Transaction cycle accurate HW
- Typical Model : Native SW Execution [ST/TIMA]



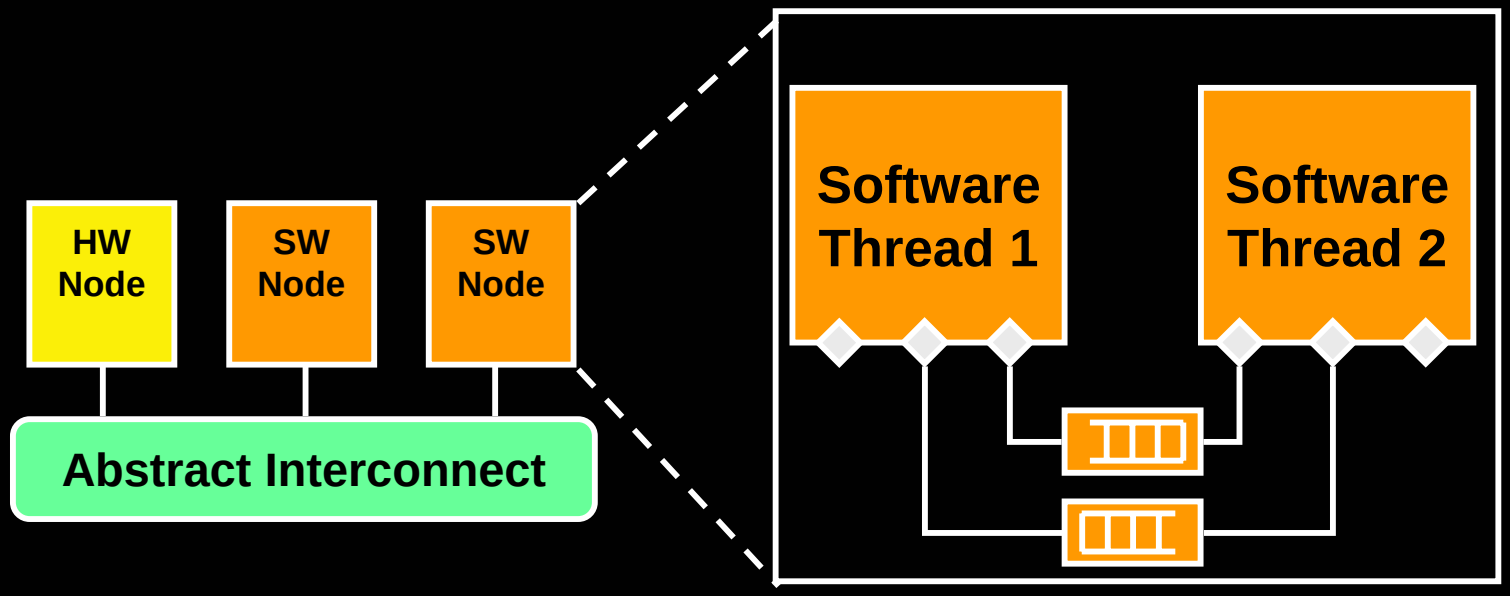
Programming Models for MPSoC Virtual Architecture model

- Explicit SW communication API
- Explicit System Interconnect
- Implicit HDS (OS, Communication Implementation)
- Typical Models: TTL, DSoC, Pthreads



Programming Models for MPSoC System Architecture model

- Explicit thread/subsystems & HW-SW partition
- Implicit communication
- Typical Models: MPI, Simulink, KPN



Implicit SW execution as a simulation module

Conclusions: Programming Models for MPSoC

- Abstract HW-SW Interfaces to enable Higher than RTL design
- Application-specific Implementation allows to reach cost and performances requirements
- Need new design automation techniques
- Is an opportunity for new HW-SW codesign approaches and architecture Exploration

Thank You