Multiprocessors in Wireless Multimedia Terminals

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Nokia / Technology Platforms / Symbian Product Platforms

15 August 2006
MPSOC Forum, Colorado, USA

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Outline

- Nokia HW/SW and S60 Platforms
- Multimedia Computers and Teardown
- Power Consumption
- Multimedia Application Processors
- General-Purpose Processors/Multicore
- Multimedia Processors
- Key Messages

Nokia Structure

Business Groups

Horizontal Groups

- Customer and Market Operations
- Technology Platforms
- Brand and design
  Developer support
  Research and venturing
  Business infrastructure

Mobile Phones	Multimedia	Enterprise Solutions	Networks
			

Corporate Functions

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Nokia HW/SW Platforms

- Complete, verified HW/SW engines with memories, EM, displays and cellular/proximity radio modems.
- Business groups take a variety of chipsets according to product needs (low/mid/high-end).
- Product price point generally specifies the chosen platform.
- Multimedia accelerators extend features in high-end terminals.
- S60 / Symbian 9.1
- S40, S30 / Nokia RTOS
- Linux 2.6

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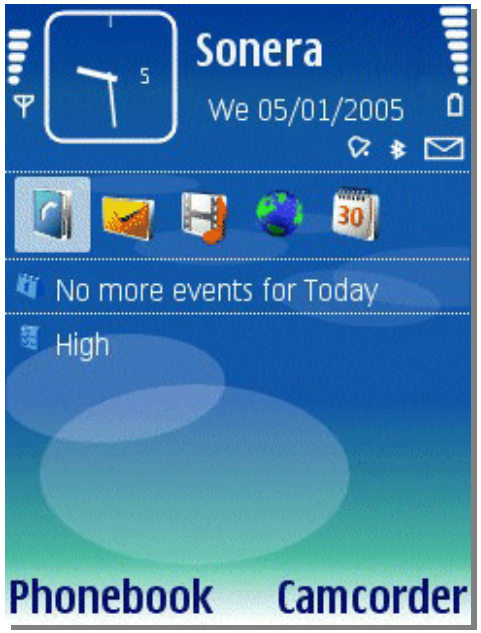
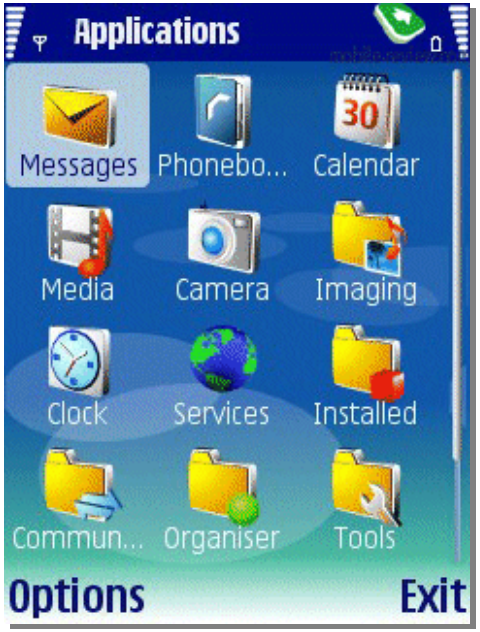
S60 Platform

S60 Open to new features

- Complete software package for smartphones.
- S60 UI concept: **Global design & UI system implementation including Symbian optimisations.**
- Application suite: **Telephony, messaging, browsing, PIM, imaging, connectivity, etc.**
- Localised to over 30 languages **including Chinese.**
- Licensed in source-code form **with extensive documentation, consultation for product integration & modifications.**
- Native Symbian / S60 C++ & Java (MIDP) interfaces open **to 3rd parties (S60 SDK) & closer partners.**
- S60 Release 2.6 and 2.8: Symbian version 8.x
- S60 Release 3.0: Symbian version 9.1





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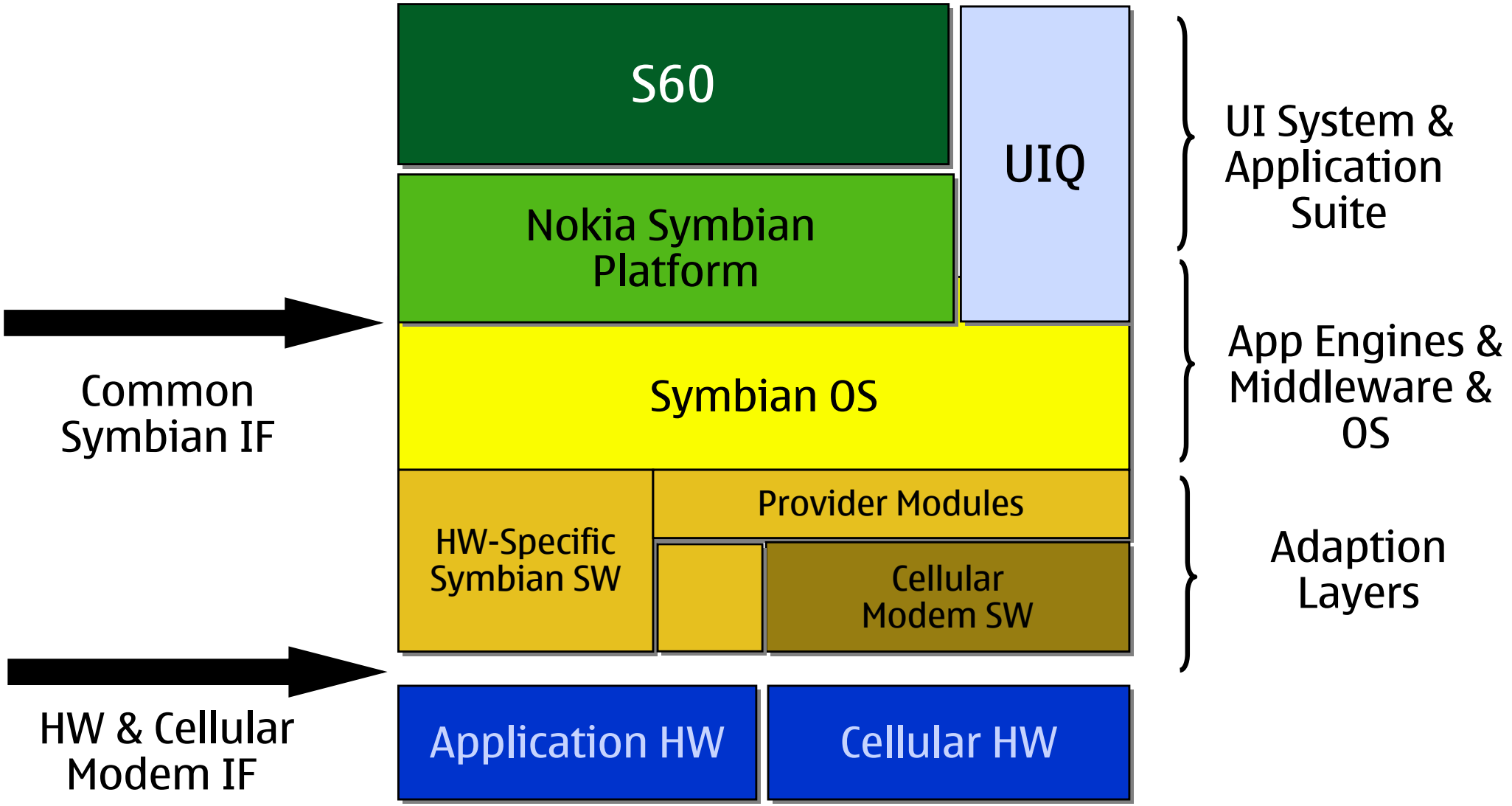
S60/Symbian Architecture



Mobile Technologies and My Favourite Features

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Multimedia Computers

Nokia 770

770: Internet Web Tablet

- Hildon UI/Apps, Linux OS 2.6 kernel
- 800 x 480 (24bpp)
- 250MHz ARM926 + C55 DSP (OMAP1710)
- WLAN 802.11b/g, Bluetooth 1.2
- 1800mAh Lithium-Ion

Nokia N93

N93: Camcorder Phone

- S60 3.0 Edition UI/Apps, Symbian OS 9.2 kernel
- 320 x 240 (18bpp), TV-out, 3D Accelerator (MBX/VGP)
- 330MHz ARM1136, 220MHz C55 DSP + IVA (OMAP2420)
- GSM/GPRS/WDCMA (128/384kbps), WLAN 802.11b/g, Bluetooth
- 1100mAh Lithium-Polymer

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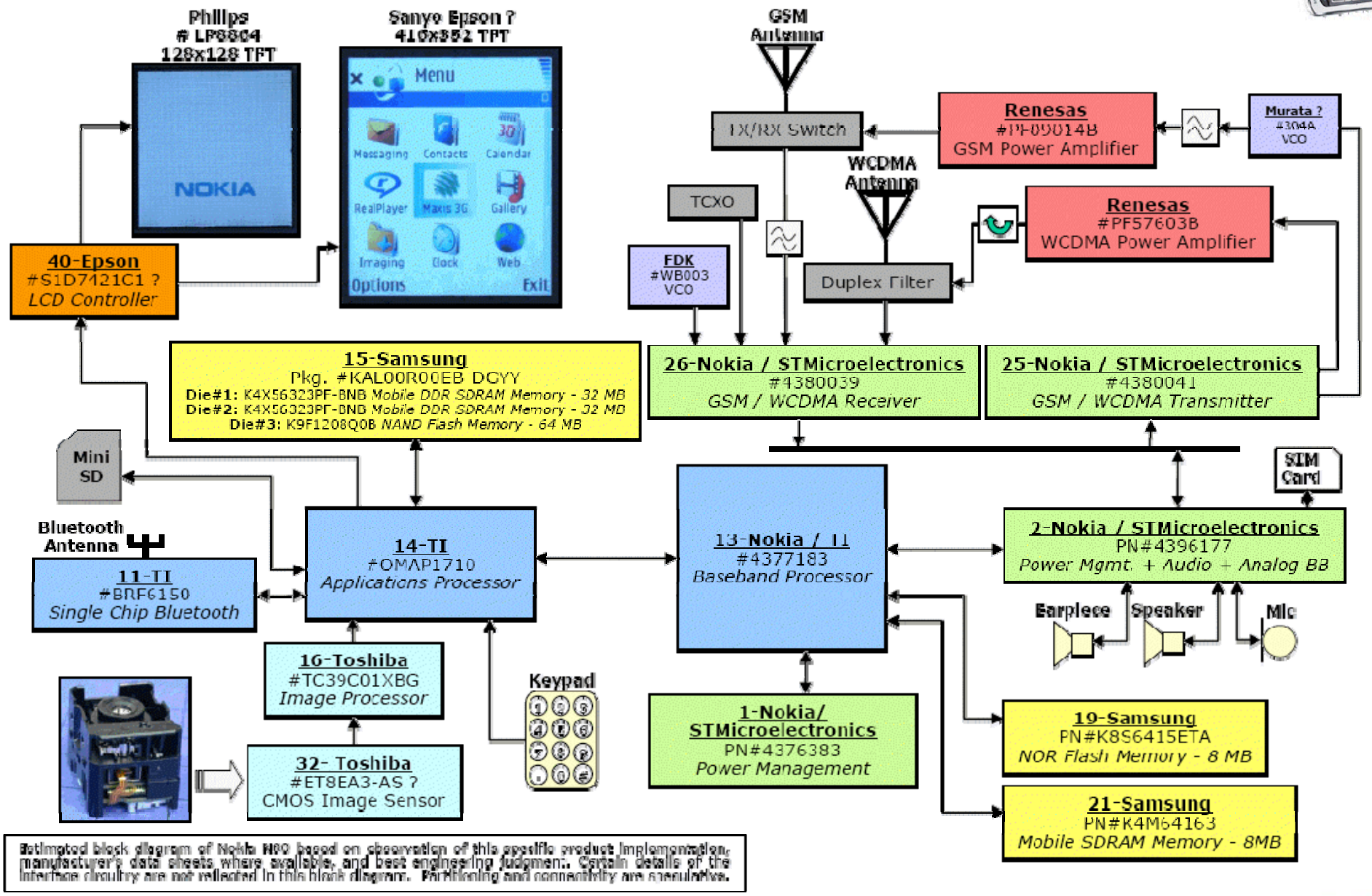
Source: Portelligent, Inc. (printed with permission)

Illustration: N90 Teardown



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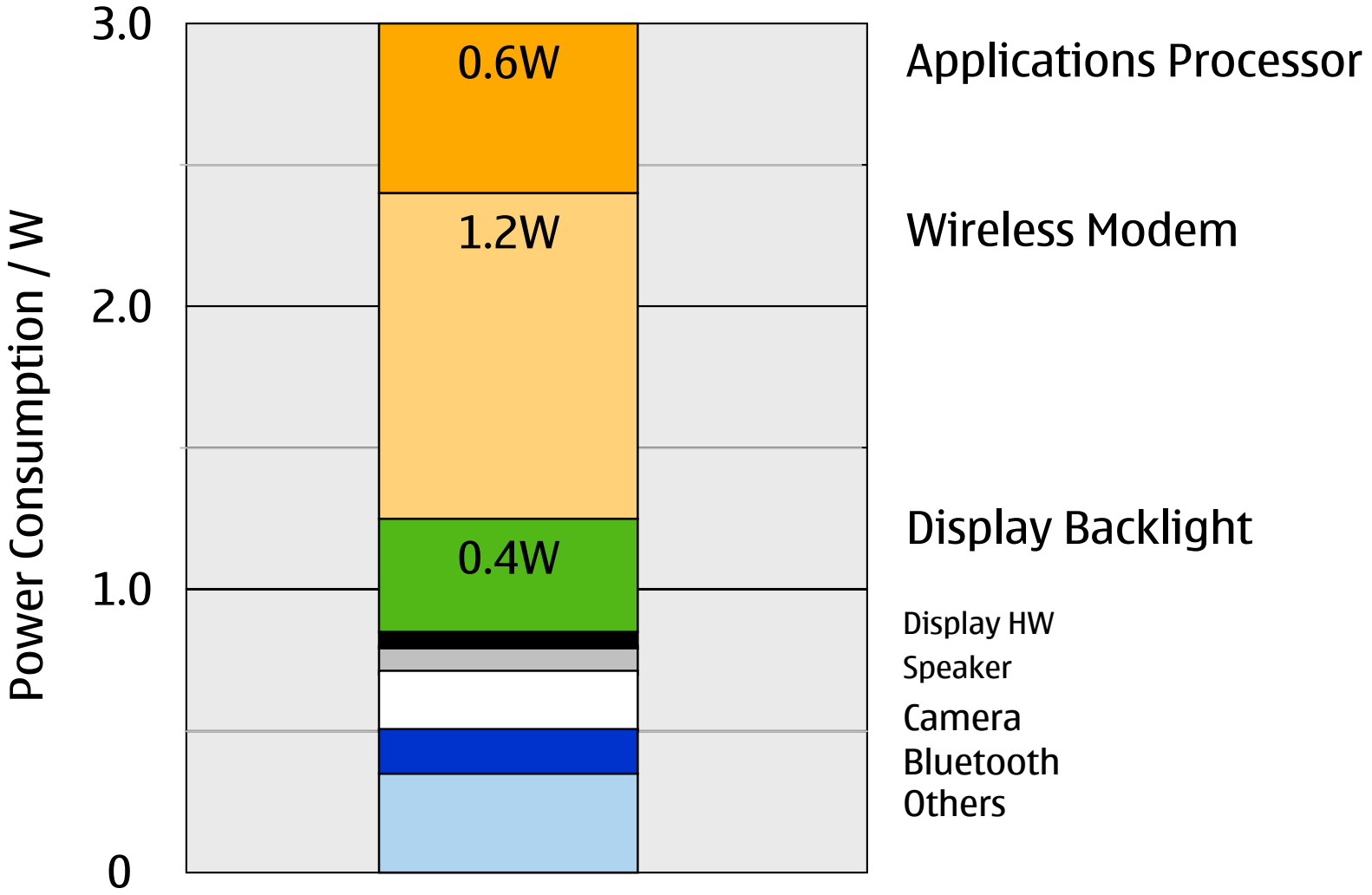
Power Consumption Breakdown: 2-Way Video Call



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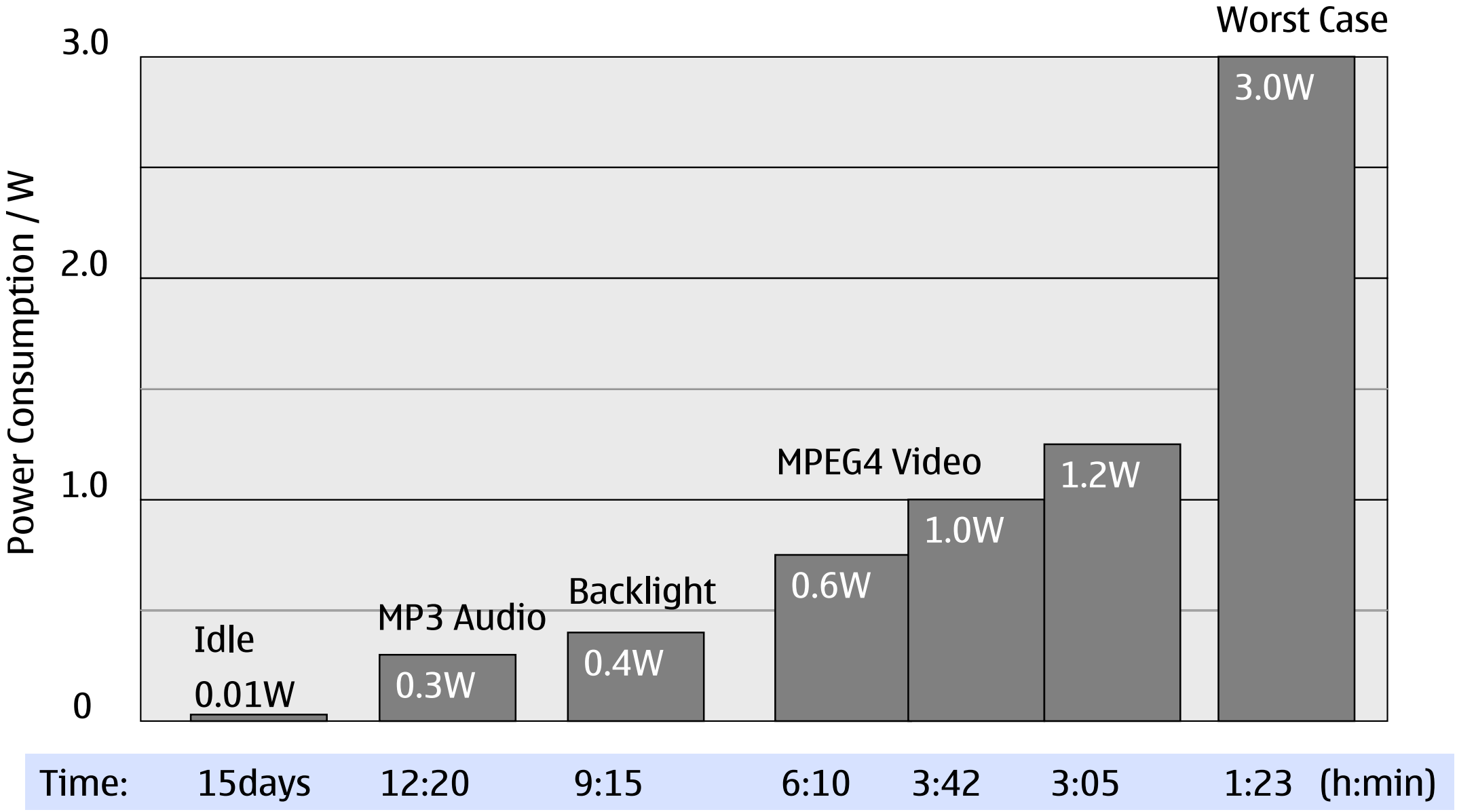
Battery: 1000mAh, 3.7Wh

MP3/MPEG4 File Playback Times



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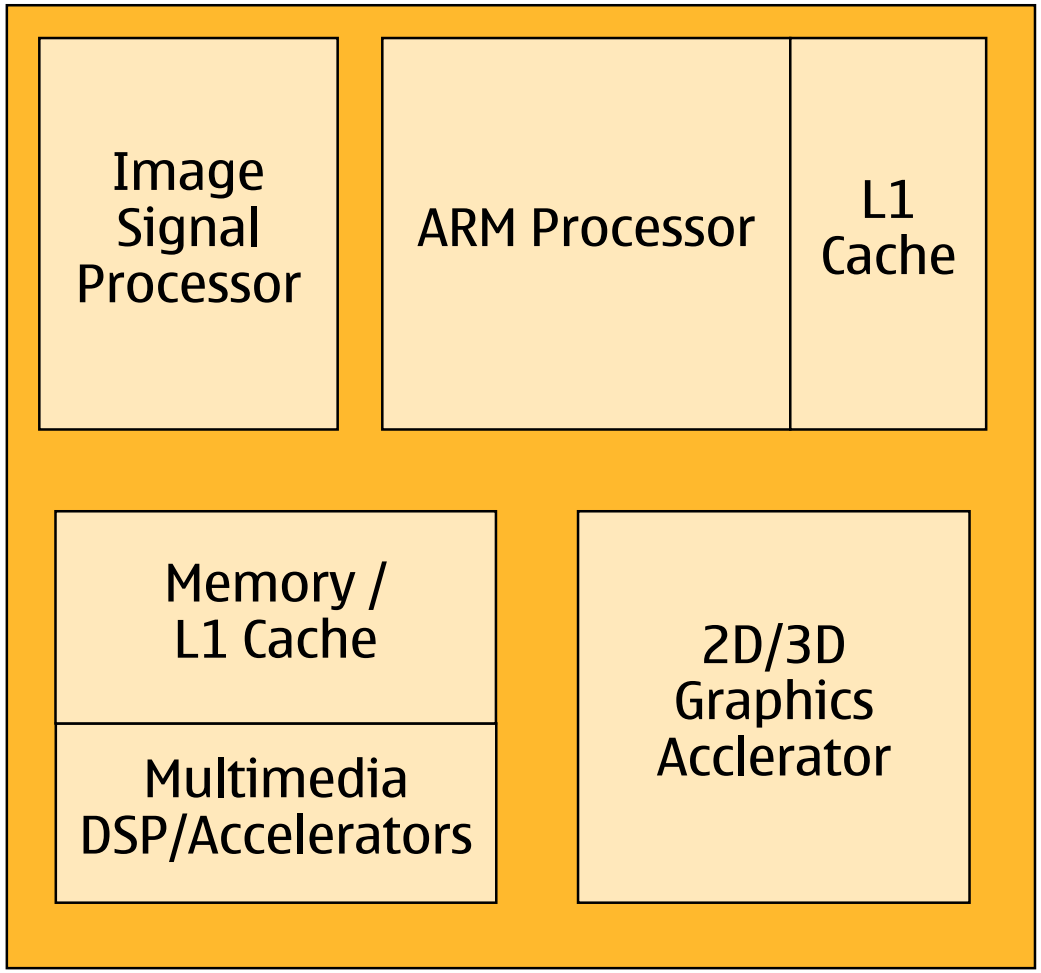
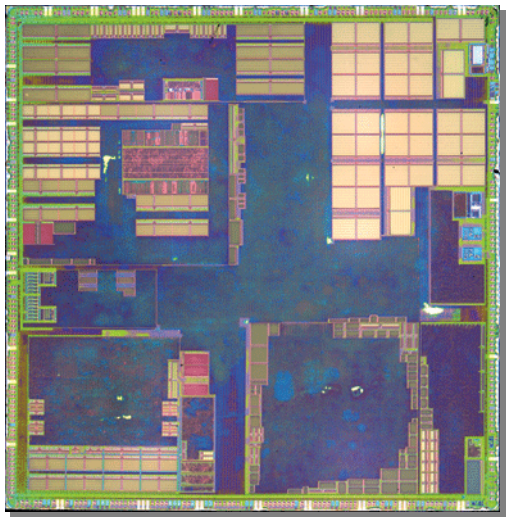
Multimedia Application Processor

- ARM processor
- Multimedia processing options:
  - Microcontroller + HW
  - DSP + HW
- 2D/3D: acceleration for rendering vector gfx, user interfaces, games.
- ISP: raw image enhancements for plain camera sensors (SMIA).
- Memory: 166MHz 32-bit Mobile DDR-SDRAM, NOR/NAND Flash.
- Peripherals: Display/TV-out, HS-USB (OTG), MMC, SDIO, I2C, SPI, UART.
- Die area: 40-60 mm^2
- Price: 5-15 USD (>10M units)
- 28M Smartphones shipped in 2005.



Sources: arm.convergencepromotions.com, www.intel.com, EETimes 11/05, ARM DevCon 04.

Application Processor vs. Mobile x86



Texas Instruments OMAP2420

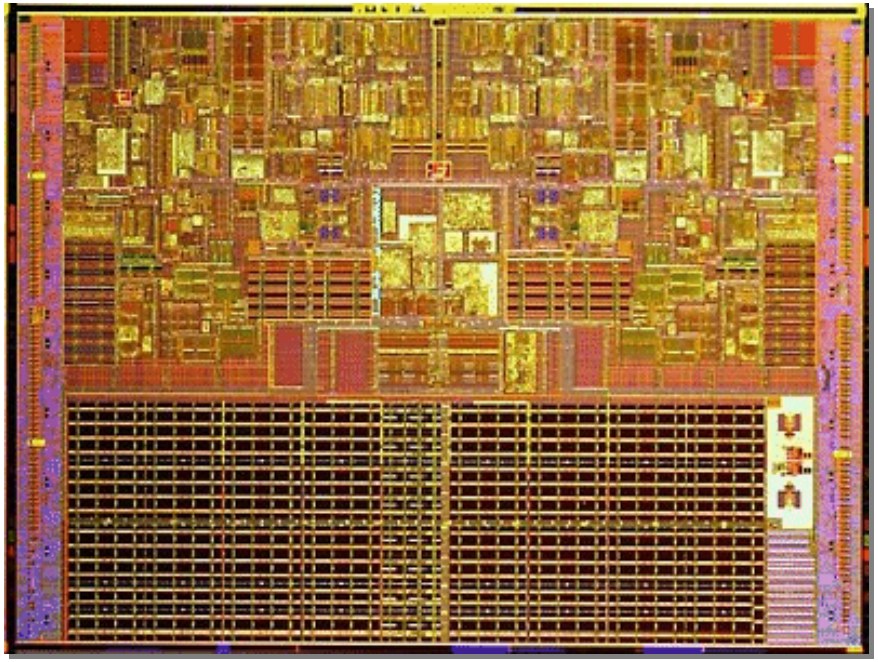
ARM1136JF 330MHz L1 32/32kB

C55 220MHz L1 16 4/4/64/96kB + IVA,

MBX/VGP 3D, 640kB SRAM

Power: 0.6W

Price: <20 USD



Intel L2300 Duo Core (Yonah)

2CPU x86 1.5 GHz, L1 32/32kB, L2 2MB

Area: 90.3 mm², 65nm

Power: 15W (TDP)

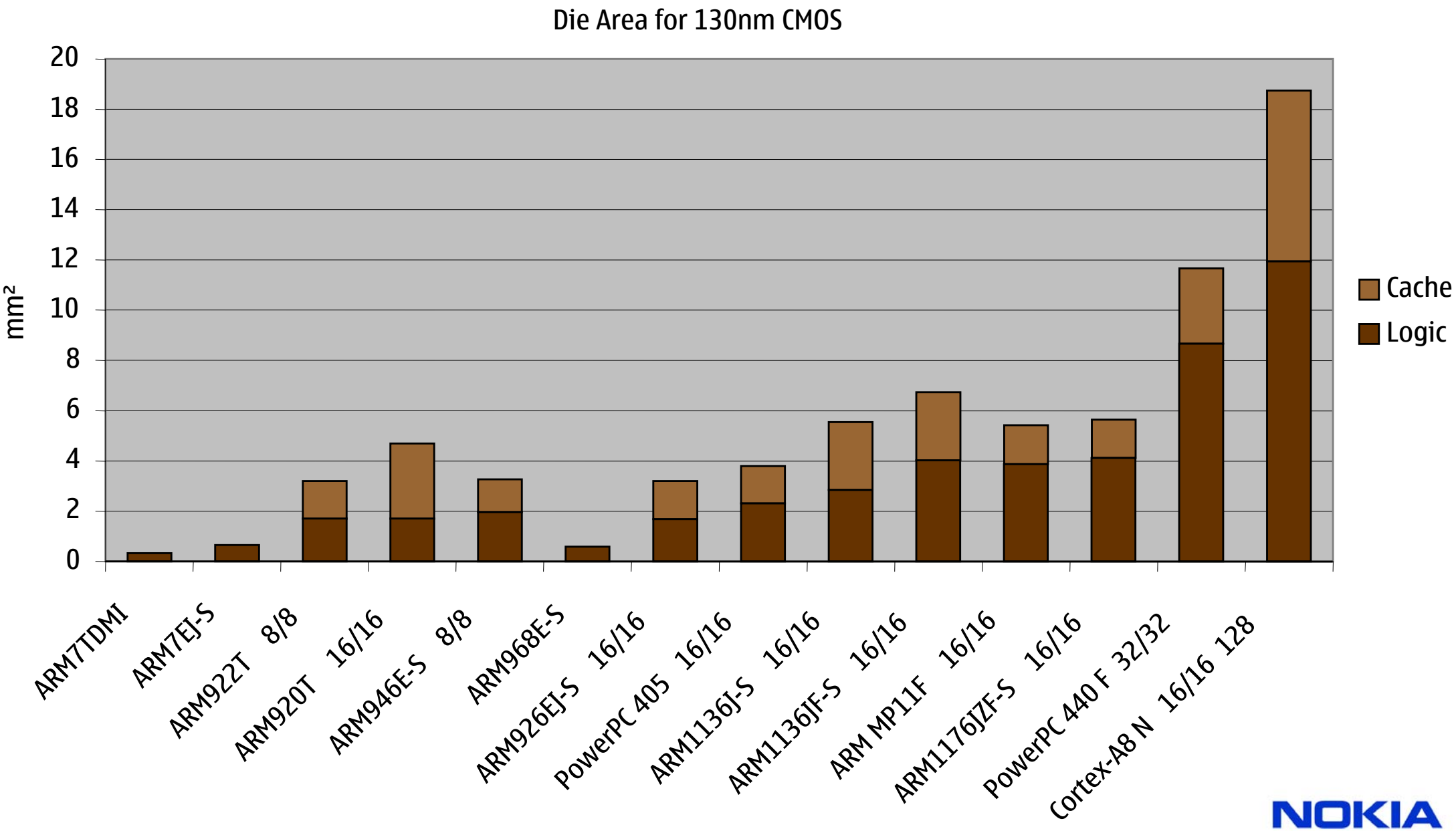
Price: 284 USD

General-Purpose Processors: ARM

- All Nokia terminals include one or more ARM processors:
  - ARM7TDMI (low-end), ARM926 (mid-end), ARM1136 (high-end).
  - Processors have MMU and L1. Lately L2-cached designs appearing in industry.
- Mobile phones are not sold by GHz-CPU arguments.
- ARM CPU power budget is 250mW.
- Cortex-A8 and ARM MPCore are next generation application CPUs.
- Implementation complexity and leakage/active power (45 nm) may limit reasonable CPU clock speeds around 800MHz.
- Simultaneous Multithreading (SMT): probably not a good idea, consider x86.
  - 10-15% increase in core logic area.
  - Cache trashing from 2+ threads.
- Symmetric Multiprocessing (SMP, Multicore): simpler CPU cores.
  - 100% increase in core/cache area.
  - 2x performance is possible.

Sources: www.ARM.com, www.IBM.com, Spring Processor Forum 06, ARM Devcon 05.
Cortex A8 area estimate: Cortex-R4 process scaling ratio 0.61 and cache areas.

General-Purpose Processor Area



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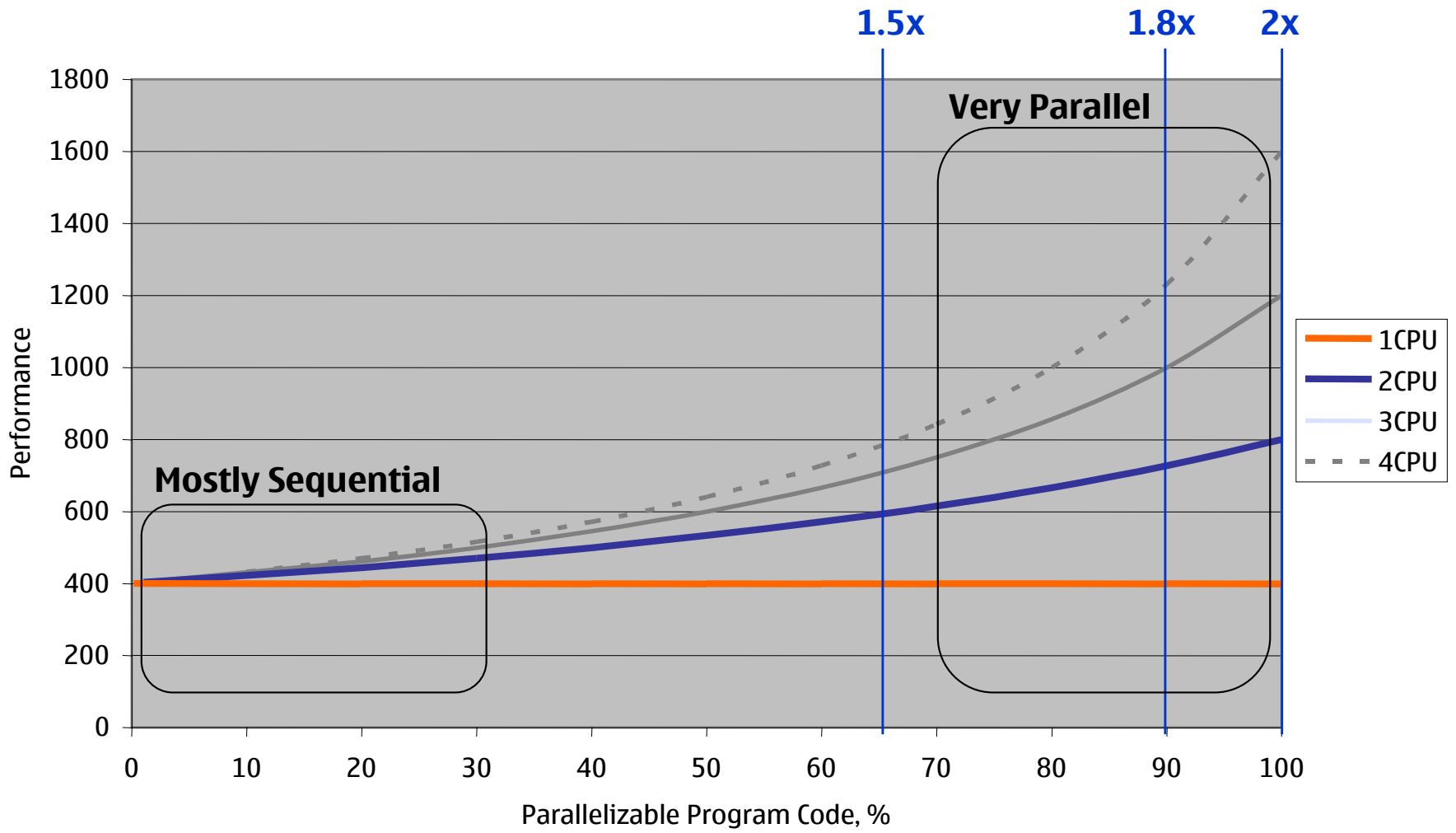
Multicore and SMT Considerations

- CPU pipeline length traditionally describes maturity of a processor microarchitecture.
- Desktop/mobile x86 CPUs today have pipeline length around 10-16 stages.
- Pipeline evolution in ARM processors:
  - ARM7 3
  - ARM9 5
  - ARM11 8
  - Cortex-A8 13
- Optimizing memory architecture for faster random-access and wider buses can bring significant performance increases.

Processor	Pipeline Stages
ARM7E	3
ARM926EJ	5
PowerPC 405	5
ARM1136JF	8
XScale (ARM) PXA27x	7
PowerPC 440	7
Pentium III	10
AMD Athlon 64	12
Pentium M (Yonah)	13*
Cortex-A8	13
PowerPC 970 (G3)	16
Pentium 4	20

Multicore Performance



Performance increase requires either: 1) multithreaded application or 2) parallel application usage scenario.

Example: Parallel Usage Scenario

”Advanced end-user Ari does multiple things at the same time.”

- Beginning:
  1. **Streaming audio** from XM Radio.
  2. **Browsing** website www.CNN.com (very tricky Java/tables/css).
  3. **Recording news video** received from DVB-H.
- Suddenly:
  4. **Push email** downloads 1MB JPEG image (background).
  5. **Voice call** comes in.
- At the same, time many OS features are used in parallel:

  VoIP stack, HTTP/TCP/IP stack, Bluetooth stack, WLAN driver, telephony, MP3 decode, RTP/UDP stack, Java virtual machine, window server, fileserver, etc.
- Requires high performance peak. Overload shows as bad user experience for the foreground application.
- Any system stutter or unresponsiveness considered harmful.

Multimedia Processors

- DSP and HW accelerator clock speeds are around 100-200MHz. Processors utilize DMA and large tightly-coupled memories. Typically there is no cache.
- Application-specific hardware units provide performance boost for time-consuming kernels mostly found in video/imaging.
- Three main processor subsystems for multimedia:
  - Video/audio processing
  - Camera post-processing
  - 2D/3D graphics acceleration
- Fast camera serial-shooting sets very high peak-processing requirements for JPEG encoders: 20-40Mpxl/second for 5 images/second at 4-8MP resolution.
- Mobile 3D graphics: OpenGL ES 2.0 will provide improved look of surface using programmable pixel/vertex shaders.
- HW design cycles are long. Programmable DSP/SIMD processors are preferred for implementing new codecs and other unpredicted product features.

MPEG4 AVC (H.264) Processing

Decoding

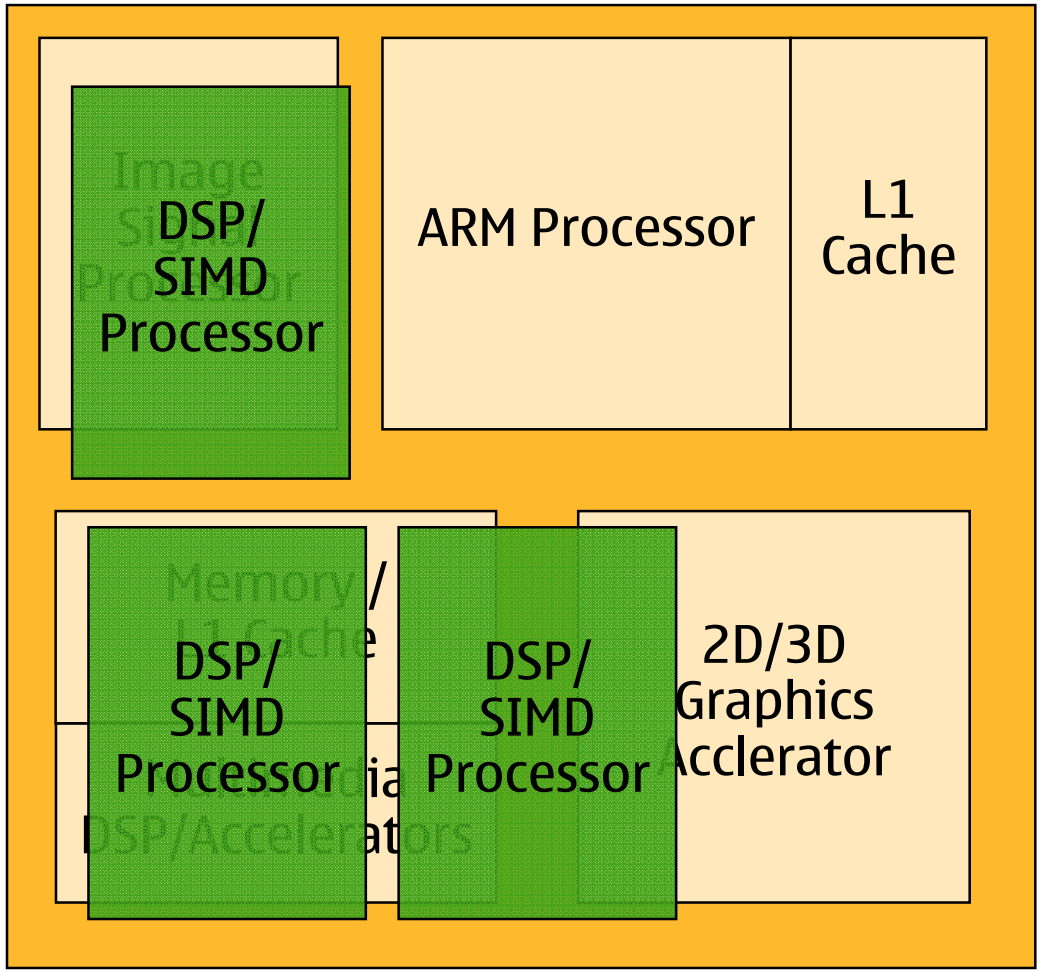
- MPEG4 Advanced Video Codec (AVC or H.264) decoder provides excellent quality for low bit rates, but requires 2-3x more processing than Simple Profile (H.263).
- All-ARM11 SW implementation of CIF (352x288) and D1 (720x576) 30fps decoding requires approximately 400 and 1400 MHz (3.5x expected).

Encoding

- MPEG4 AVC video encoding is roughly 4x more complex as decoding.
- Using decoder estimates, CIF and D1 30fps encoding would require 1.6GHz and 5.6GHz ARM11.
- MPEG4 AVC (H.264) codecs supporting D1 30fps need hardware acceleration.
- Coarse comparison: an MPEG4 Advanced Simple Profile (ASP) implementation reports CIF encoding at 35fps with 1.66GHz Athlon CPU. D1 35fps encoding would require 6GHz.

Related Topics

- Open interface standards from MIPI alliance: apps processor-modem, display/camera serial interface, high-speed serial (SLVS), UniPro.
- Advanced multi-die packaging for digital ASICs: Product size reduction and performance improvements.
- Standard DSP/SIMD-processor concept:
  - Enable reusing optimized software
  - Maximize silicon utilization
  - Instruction set architecture for BB/camera/imaging/video
  - Specify only ISA, implement a family of processors or one processor (IP)



Six Key Messages

- Wireless multimedia computers are extremely power and heat limited gadgets. Fundamentally this limits amount of processing power integrated into device.
- Power constrained CPUs are mandatory, but the most exciting features require system-level SW optimization. ARM Dhrystone_2.1 power budget is 250mW.
- General-purpose processors will evolve to multicore due to increasing architecture/implementation complexity in the most advanced CPUs.
- We will not get performance increase as ”a free lunch” anymore in multicore/SMT because applications need multithreading or parallel use case.
- MIPI: key venue for specifying open, license-free mobile chipset interfaces.
- Mobile industry could benefit from a standard, licensable multicore processor that is architected for video/imaging and baseband DSP processing.