An H.264/AVC Main Profile Video Decoder Accelerator in a Multimedia SOC Platform

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THEDA.DESIGN.
Tsing Hua Electronic Design Automation & IC Design

IC Design Tecnology

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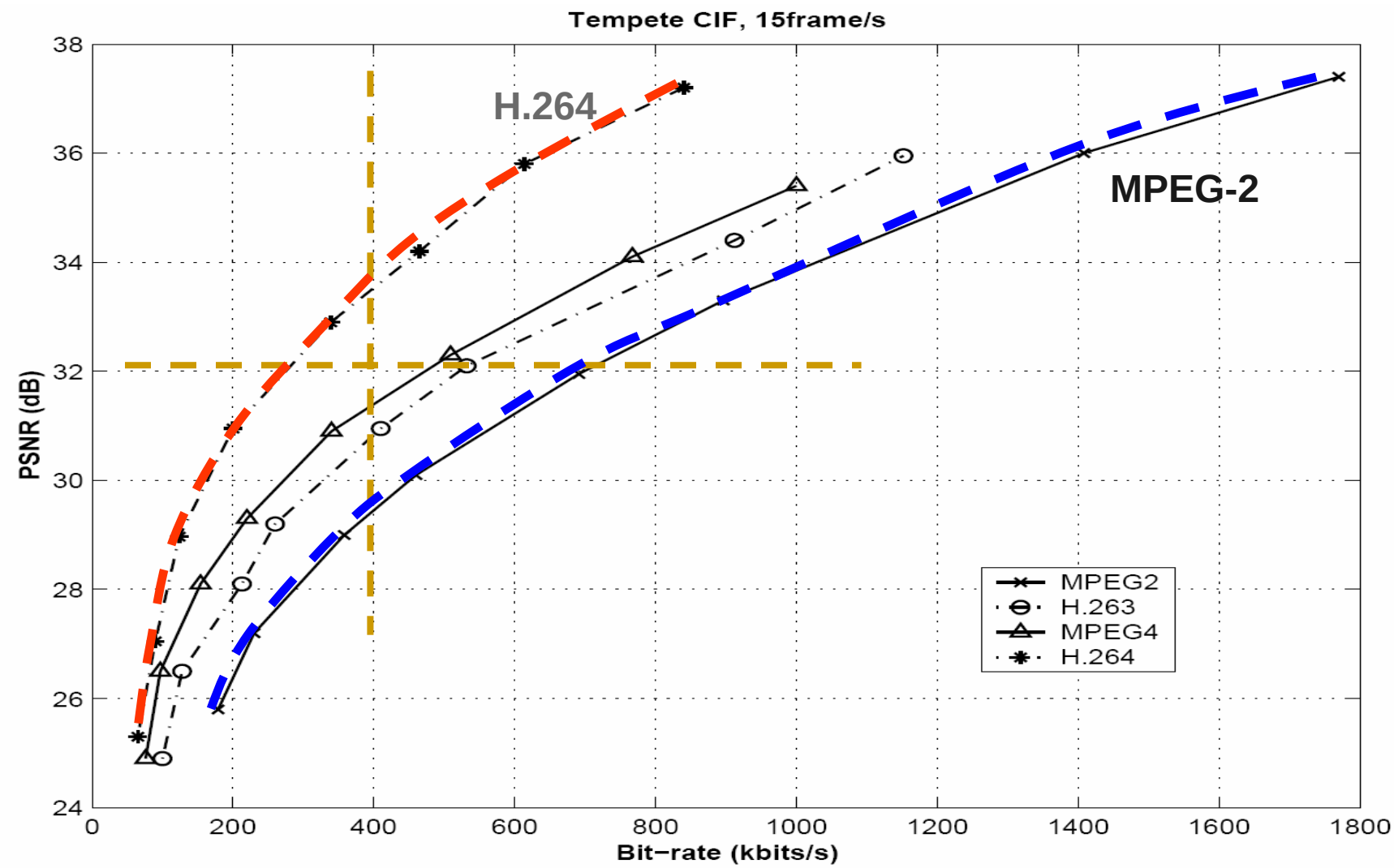
Main Points

- Hardwired design has excellent area, performance, power advantages
- If it is to be used by 1B people everyday, every bit and every cycle count
- It is not difficult
  - 15 CS student-years, no background in video nor HDL-based design; neither is the professor
  - RTL design is the easy part;
  - Understanding algorithm and designing architecture are most critical

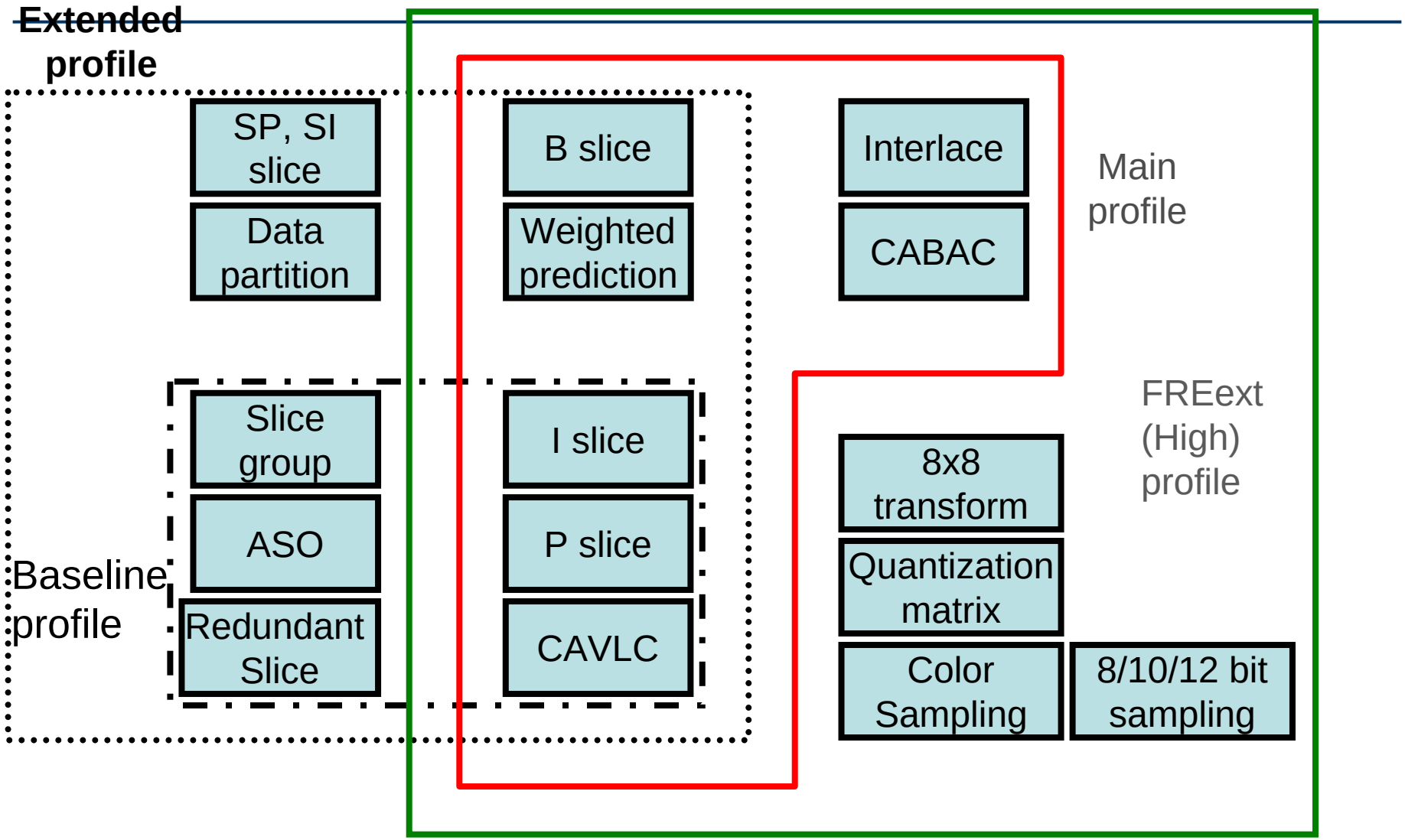
Video Coding Standards

Standard	MPEG-1	MPEG-2	MPEG-4	H.264
MB size	16*16	16*16(frame)	16*16	16*16
Block size	8*8	8*8	16*16, 8*8	16*16, 16*8, 8*16, 8*8, 8*4, 4*8, 4*4
Transform	DCT	DCT	DCT/ Wavelet	4*4 int transform
Entropy coding	VLC	VLC	VLC	VLC, CAVLC and CABAC
ME, MC	Yes	Yes	Yes	41 MVs per MB
Pixel accuracy	½ pel	½ pel	¼ pel	¼ pel
Reference frames	One frame	One frame	One frame	Multiple (5) frames
Picture type	I, P, B	I, P, B	I, P, B	I, P, B
Transmission rate	Up to 1.5 Mbps	2-15 Mbps	64kbps~2Mbps	64kbps ~ 150Mbps

Get More for Less



H.264/AVC Profiles



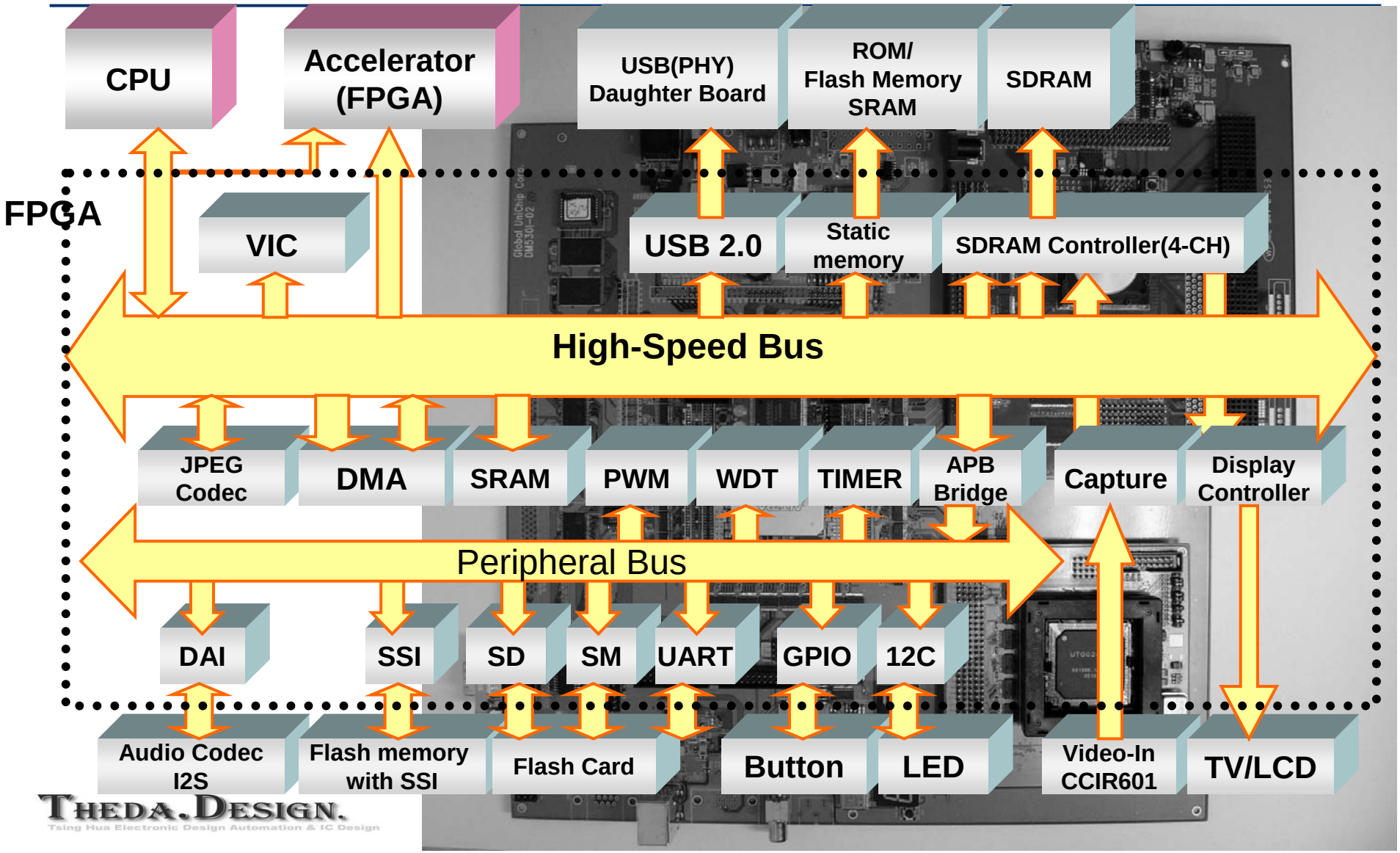
NTHU H.264/AVC Main Profile Video Decoder Prototype

Multimedia SOC Platform

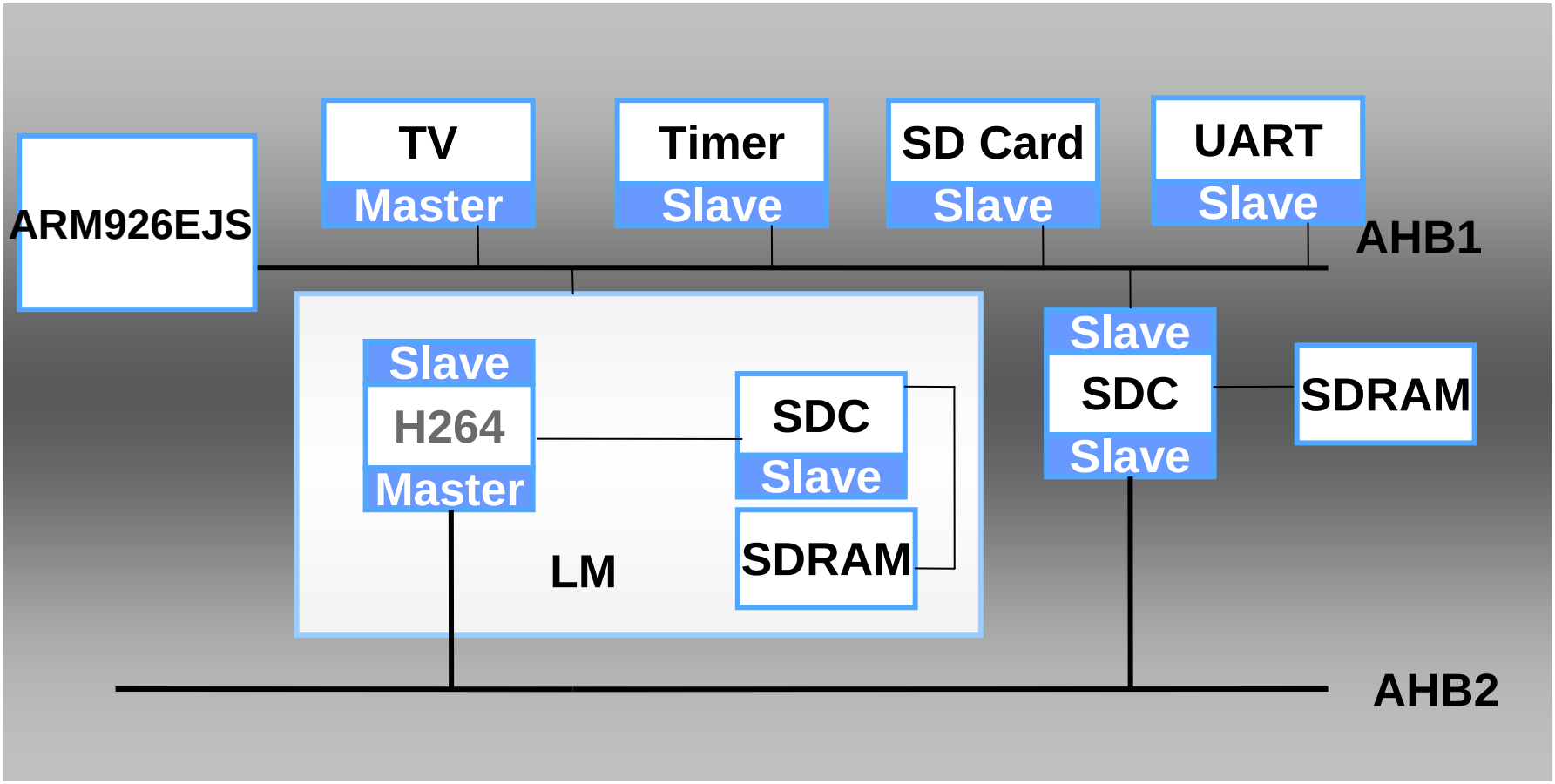
FPGA @ 10MHz
Main Profile
CIF(352x288)@ 30 fps

FPGA @ 24MHz
Main Profile
D1 (720x480)@30fps

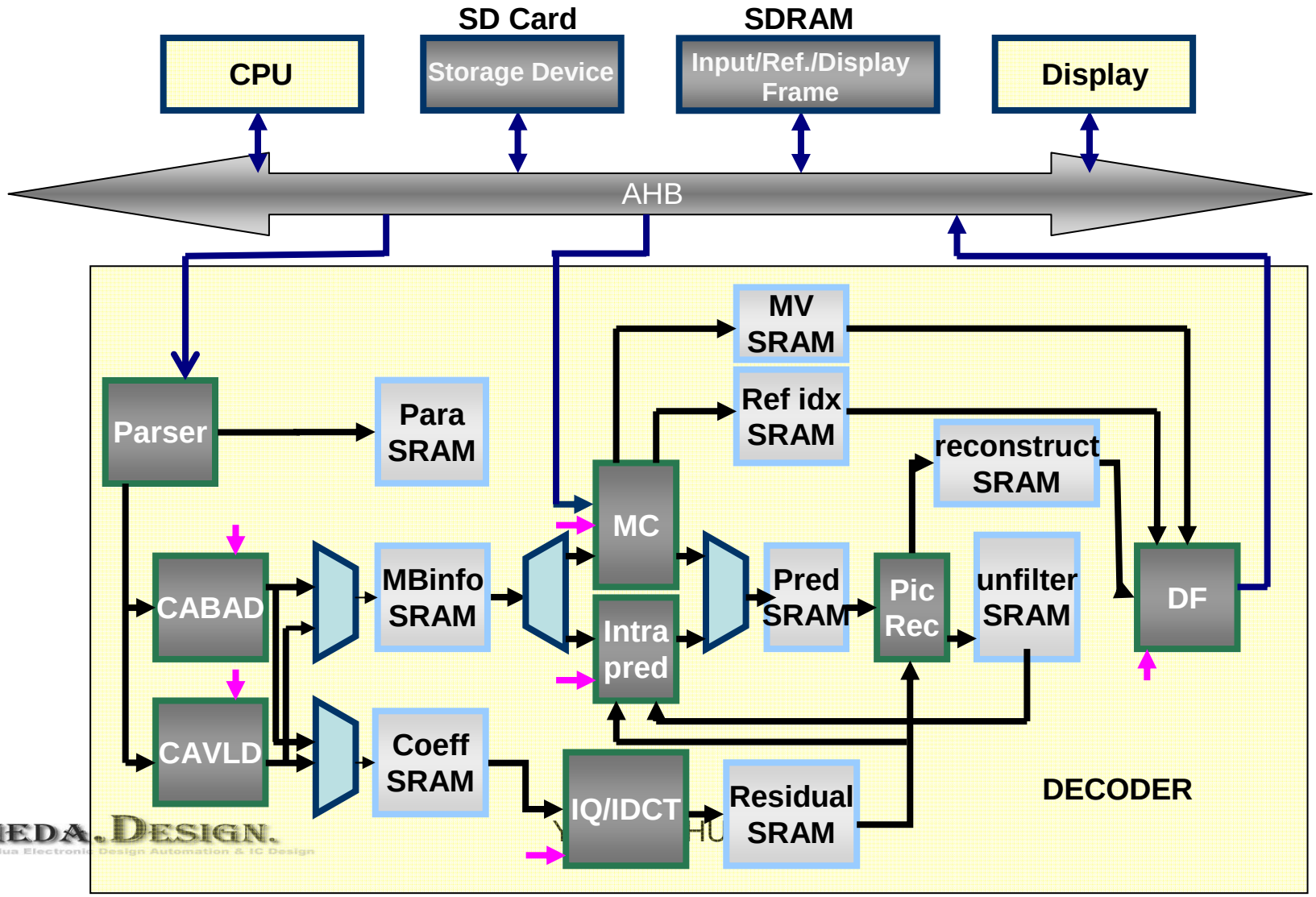
A Multimedia SOC Platform



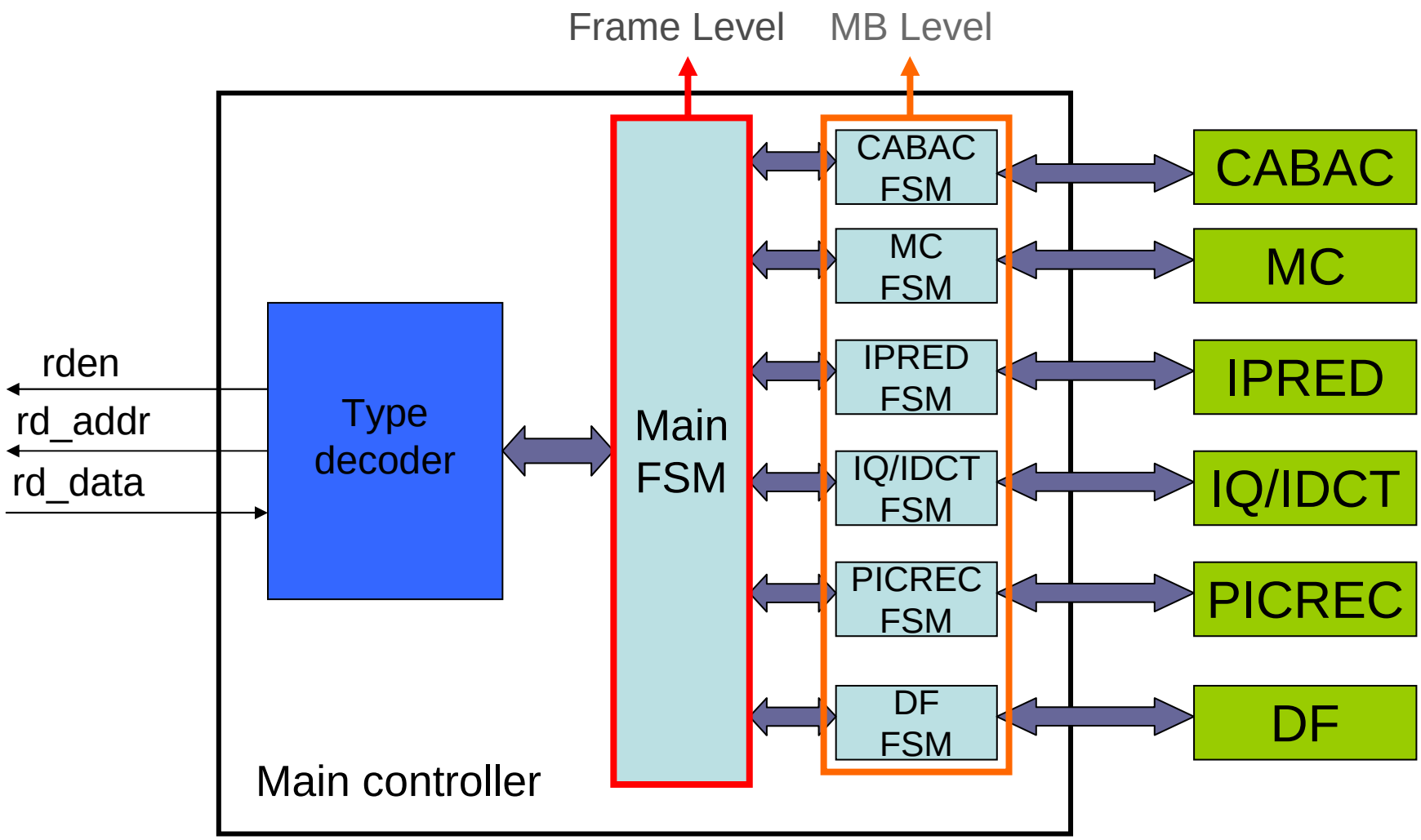
H.264/AVC Decoder System Diagram



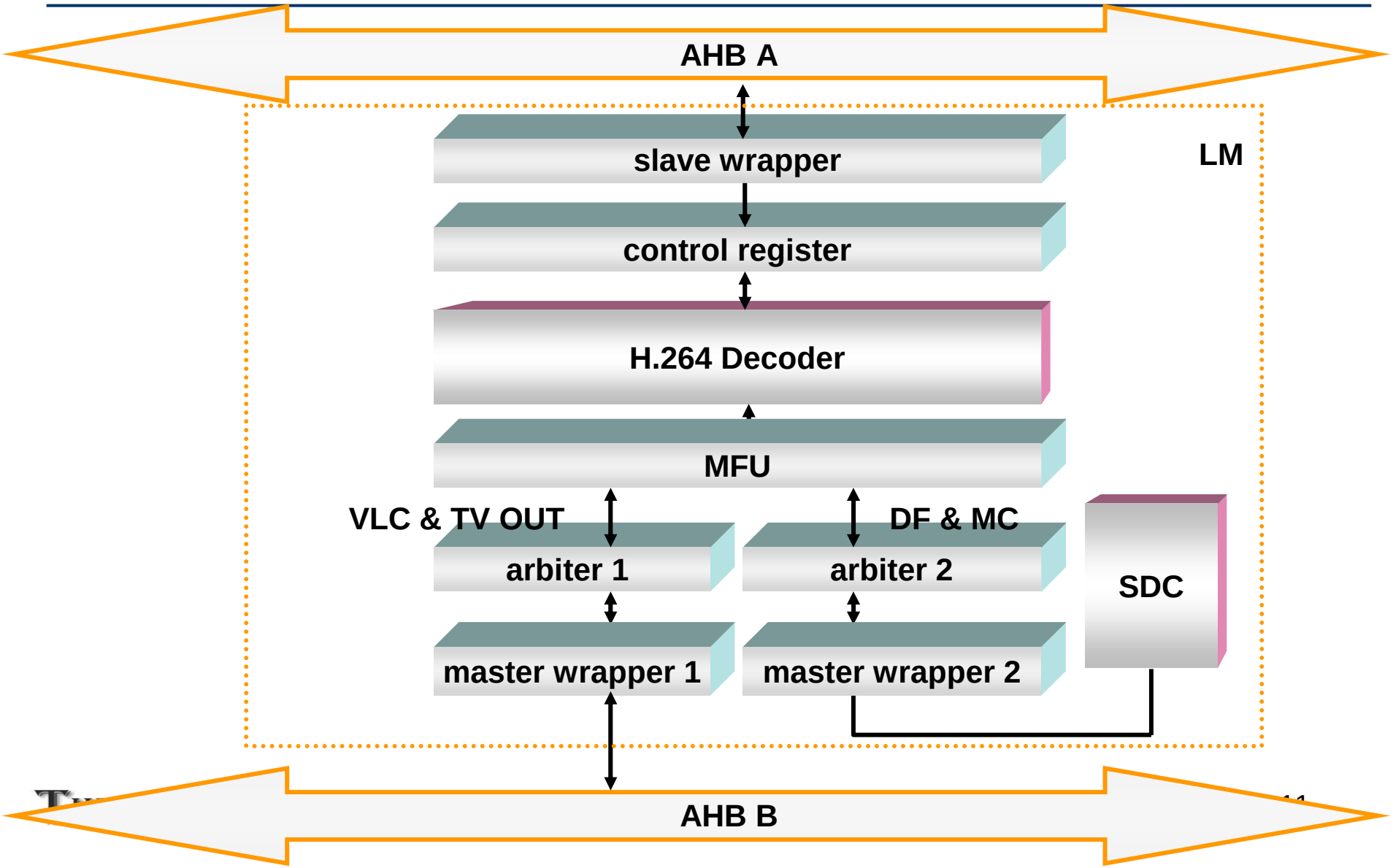
H.264/AVC Decoder Architecture



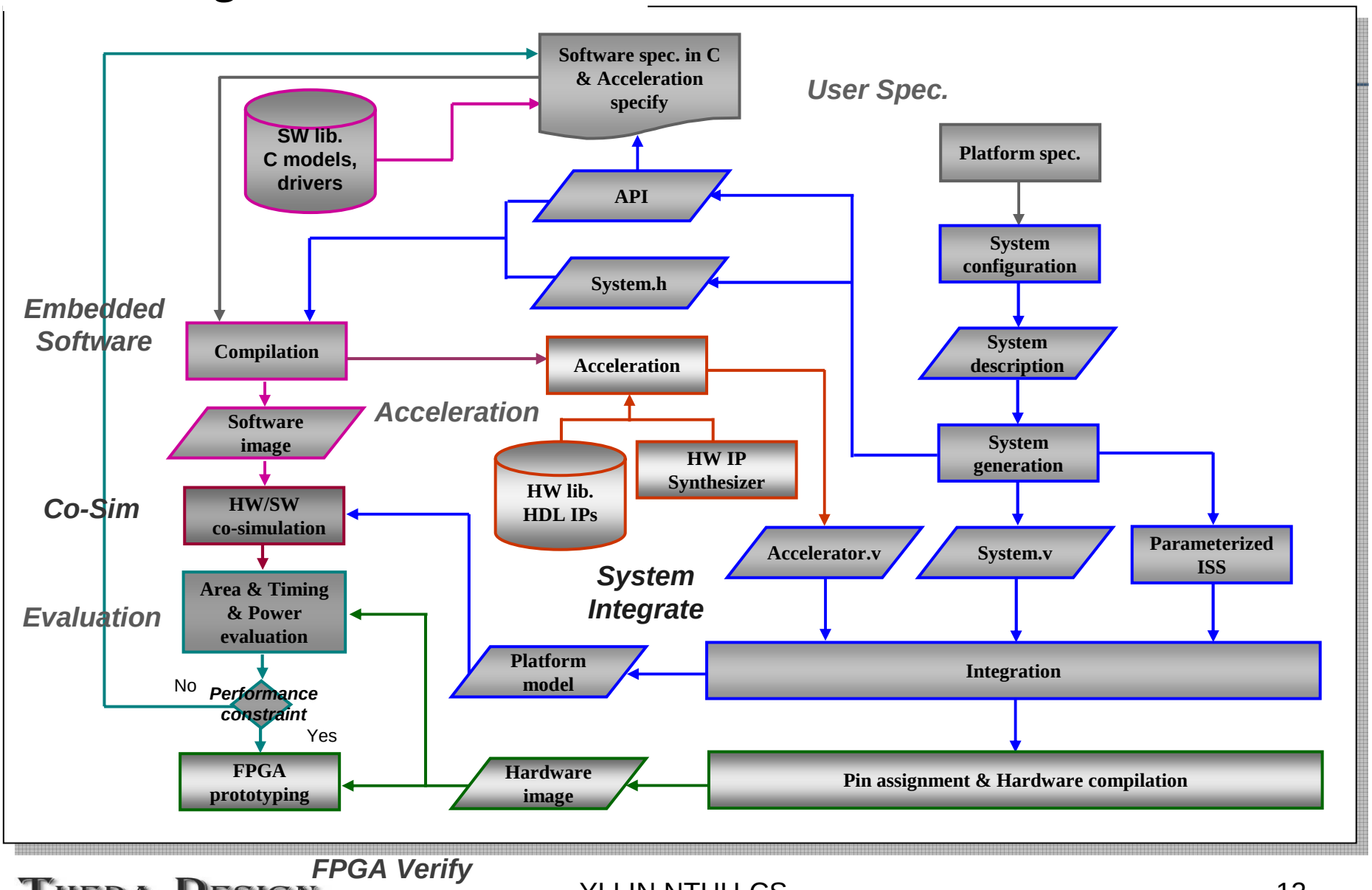
Hierarchical FSM in Main Controller



AMBA interface



Our Design Flow

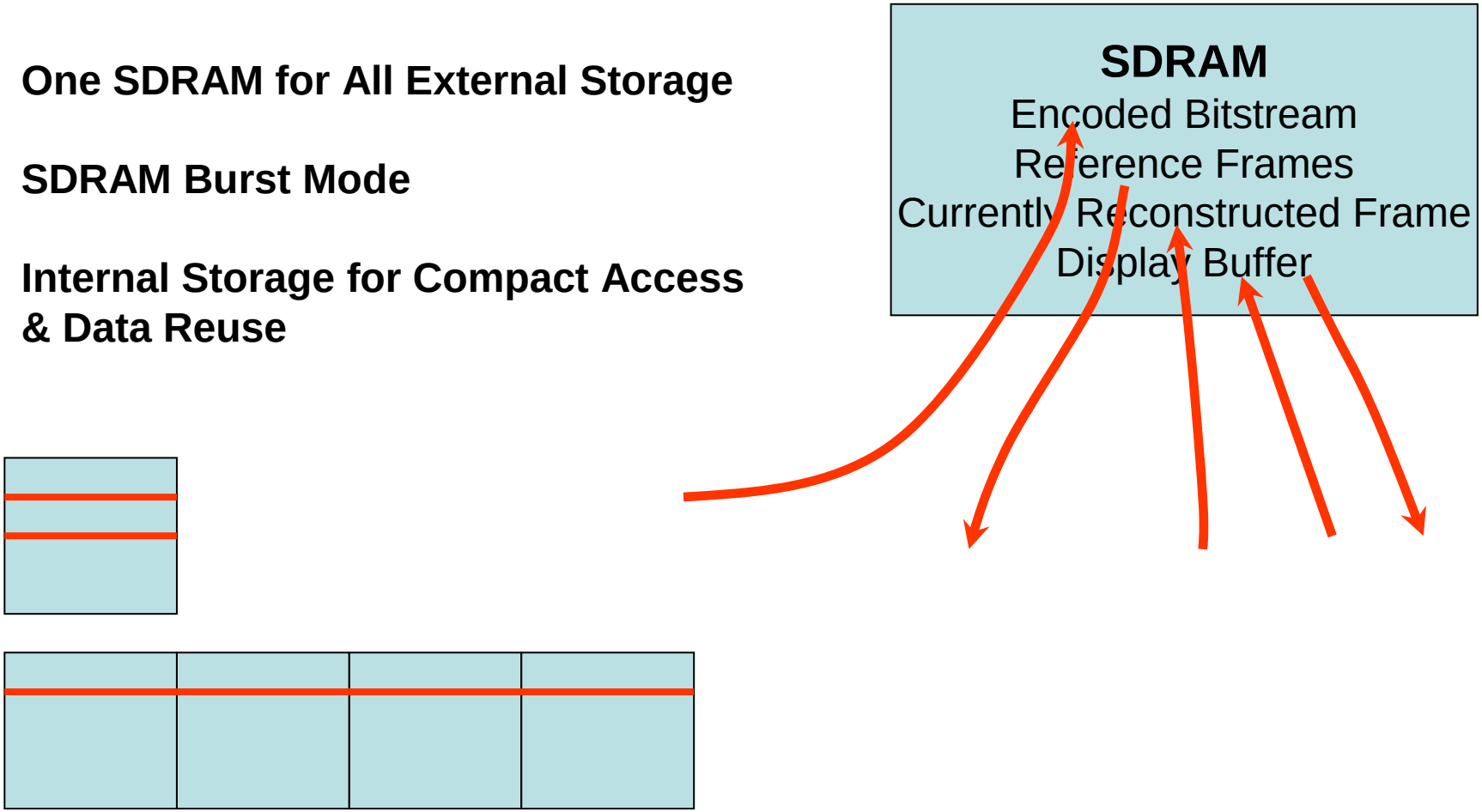


Memory Traffic Consideration

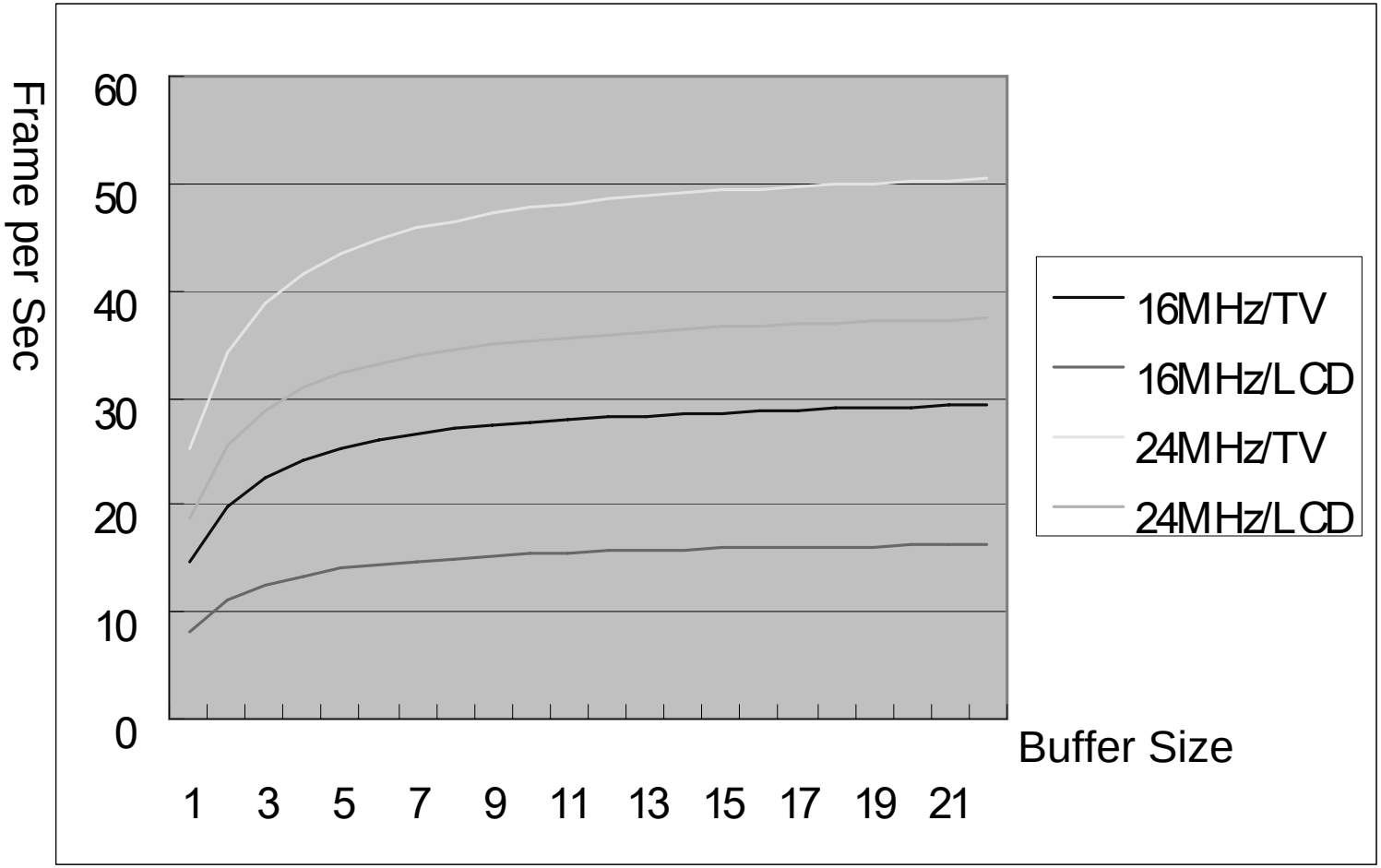
One SDRAM for All External Storage

SDRAM Burst Mode

Internal Storage for Compact Access & Data Reuse



Buffer Size vs Bus Traffic



Performance Comparison

	DSP Core	HW Accelerated	
Gate Count	230K	180K	180K
MHz	200	10	24
Profile	Baseline	Main	Main
Resolution	QCIF (176x144)	CIF (352x288)	D1 (720x480)
Frame Rate	15	30	30

Summary

- An H.264/AVC main profile decoder on an ad hoc multimedia SOC platform
- Hardware-accelerated approach is high-performance and energy-efficient
- Memory traffic has major impact on performance
- It is not as difficult as you may think; algorithm and architecture are critical; writing Verilog is no difference from writing C
- Do not try to parallelize Reference Software; it is just proof of concept; not an implementation

Demo Video