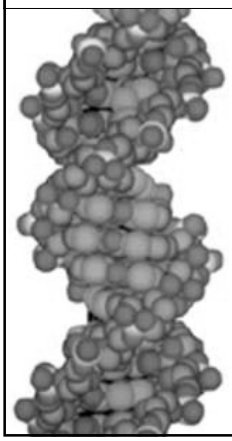
Evolving MPSoC Solutions



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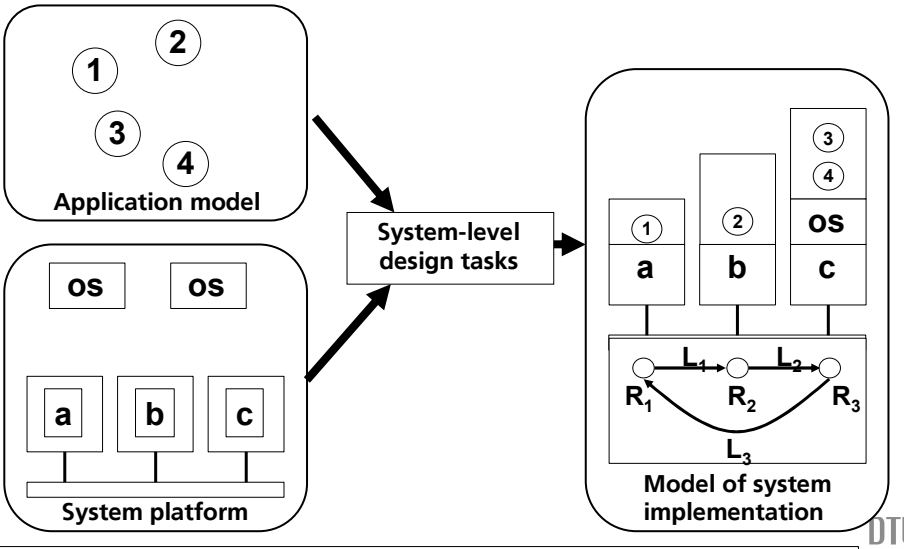
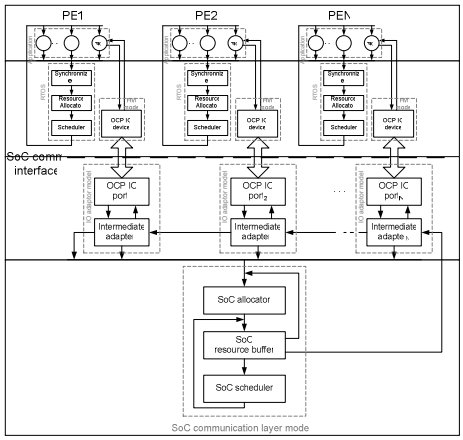
MPSoC 2006

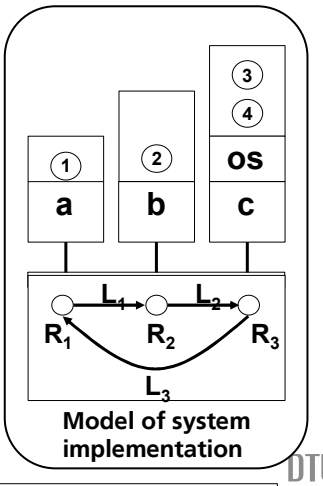
Motivation



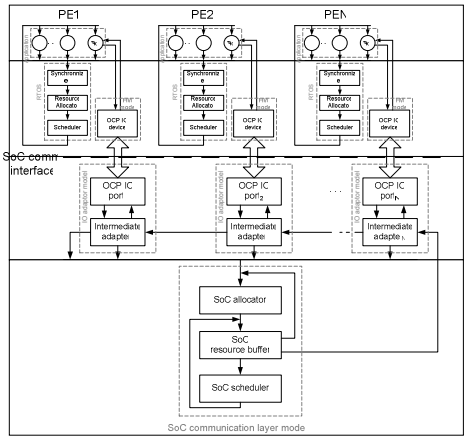
MPSoC 2005: ARTS model

ARTS model in SystemC





MPSoC 2005: ARTS model

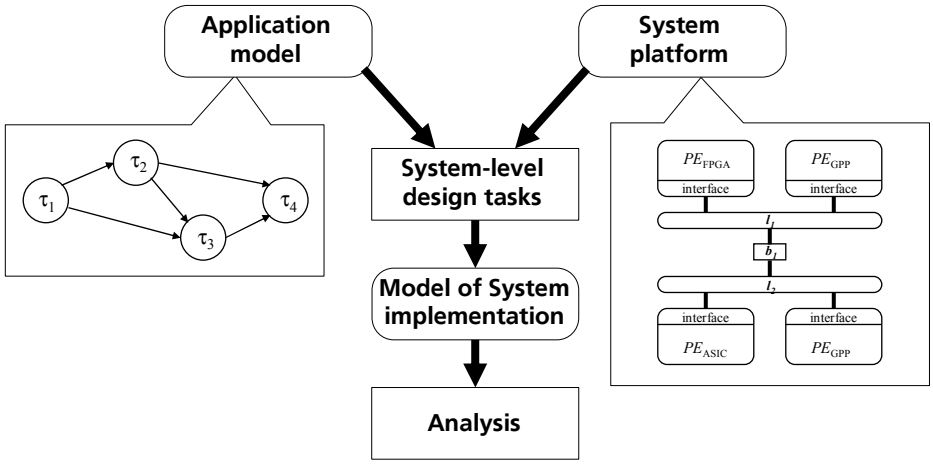


- **ARTS** Simulation framework based on SystemC
- **ARTS** PE module:
  - Application
  - OS
  - IO ports (OCP 2.0 interface)
  - IO device drivers
- **ARTS** Communication module:
  - Network topology and protocol
  - Network adapters
  - IO ports (OCP 2.0 interface)
- **ARTS Simulation traces**:
  - Deadlines
  - PE and Communication utilization
  - Memory profiles
  - Power profiles

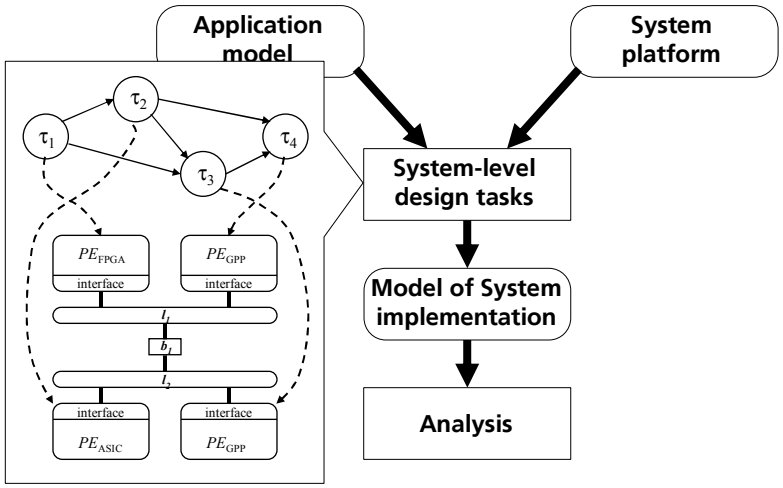
Outline

- Design space exploration
  - Exploration flow
  - Exploration scenarios
- Evolutionary algorithms
  - Problem encoding
  - Solution evaluation
- Case study: Smart Phone application

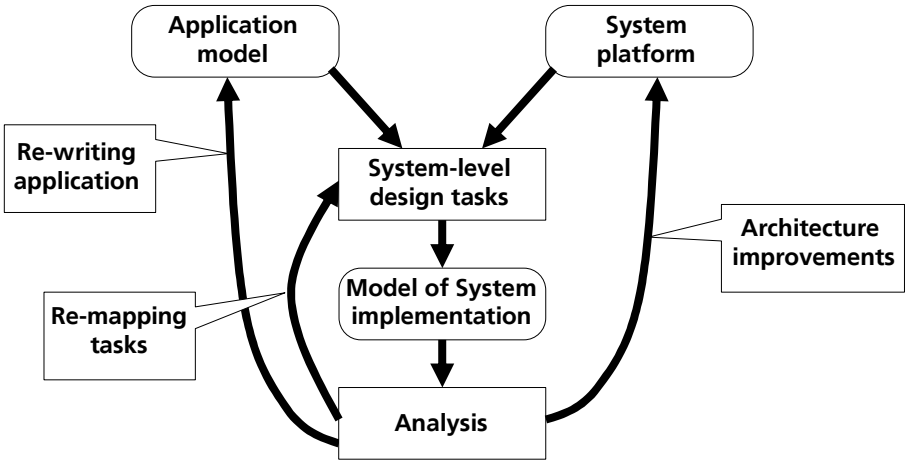
Design space exploration



Design space exploration



Design space exploration



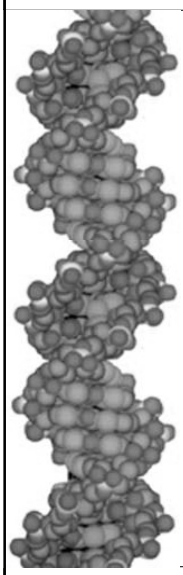
Exploration scenarios

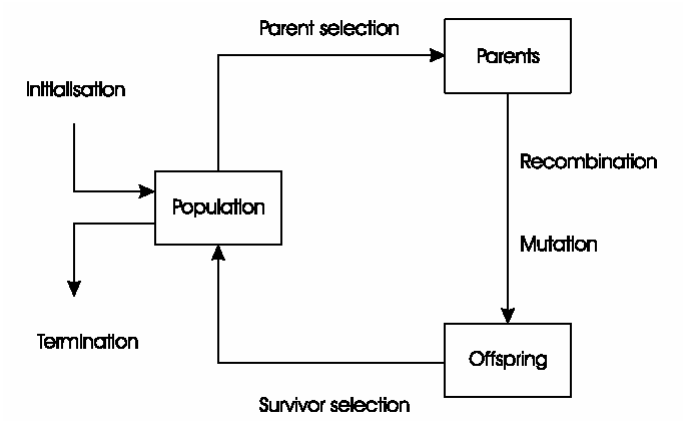
- Assumption:
  - Static scheduling, i.e. no dynamic OS
- Explore task mappings
  - No change in architecture
- Explore task mappings and architecture improvements
  - Number and types of cores, buses and bus bridges

Design space exploration

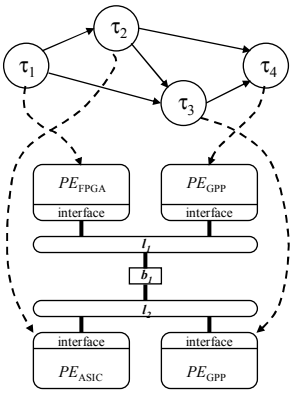
- Automatic exploration
- Multiple objectives:
  - Meet deadlines
  - Minimize power consumption
  - Stay within memory bounds
  - Minimize communication buffers
  - Minimize component cost
- Based on an Evolutionary Algorithm (EA)
  - PISA framework from ETH Zurich (SPEA2)

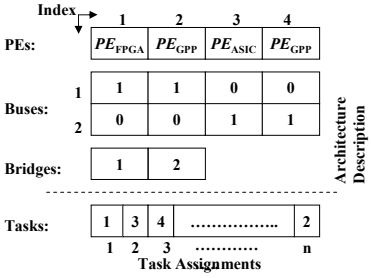
General Scheme of EAs





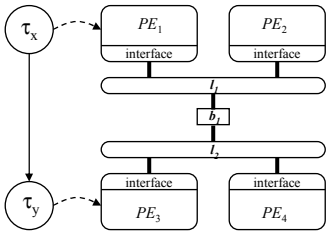
Problem encoding in EA

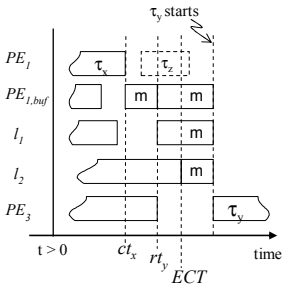




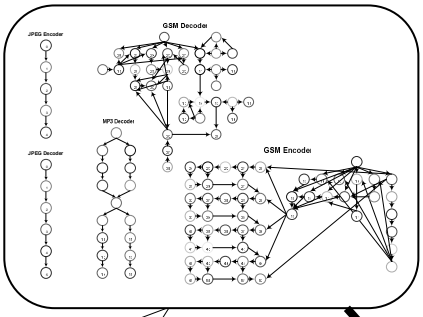
Fitness evaluation

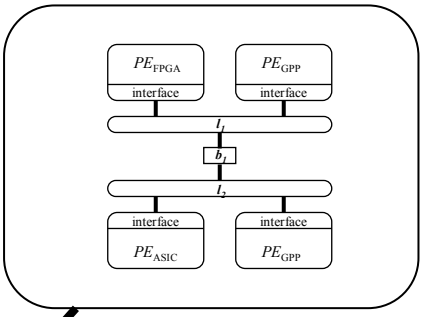
- List-based scheduling





Case study





- Hyper period
- Total number of tasks **530**

System-level design tasks

- Meet deadlines
- Min. power
- Min. buffer sizes
- Component cost

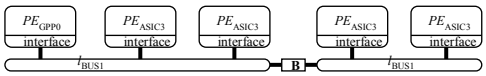
Characterization of components

PE type	freq. (MHz)	cost ($)	Mem/chip size (Bytes)/(μ^2 or TLBs)	static power (μW)	comm. power (μW)
General Purpose Processors (ARM Family):					
PE_{GPP0}	25.0	100	1024000 Bytes	800	2000
PE_{GPP1}	10.0	50	1024000 Bytes	800	2000
PE_{GPP2}	6.6	50	1024000 Bytes	800	18000
PE_{GPP3}	10.0	50	1024000 Bytes	880	2000
ASIC (0.35μ):					
PE_{ASIC0}	2.5	400	18374 μ^2	10	21
PE_{ASIC1}	2.5	300	50000 μ^2	18	37
PE_{ASIC2}	2.5	500	24274 μ^2	10	21
PE_{ASIC3}	2.5	300	50000 μ^2	20	37
FPGA (Xilinx Family)					
PE_{FPGA}	2.5	250	1220 TLBs	127	42.79
Communication links (buses)					
l_{BUS0}	66.0	65	NA	775	4881.648
l_{BUS1}	33.0	48	NA	941	4781.648

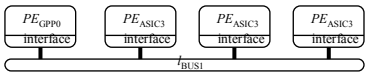
Exploration results

id	cost($)	Energy (J)	Memory violation (Bytes)
166	1396	22.0	1344
171	1048	29.0	0
184	1396	24.6	0
187	1596	22.0	612

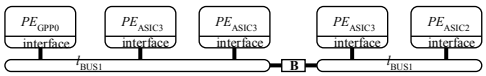
Architecture: id 166, id 184



Architecture: id 171



Architecture: id 187



Acknowledgements

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  - Thomas Stidsen (Assistant Professor)