RENESAS
Everywhere you imagine.

A New Business Model to Face the Challenges in the Ubiquitous Era

Renesas Technology Corp.

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LSI Product Technology Unit
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August 18, 2006

MPSoC '06

Outline

1. Introduction of Renesas
2. Technology and Market Trends
3. Key Issue: Design Cost Reduction
4. Renesas Business Model
5. Conclusion

Company Profile

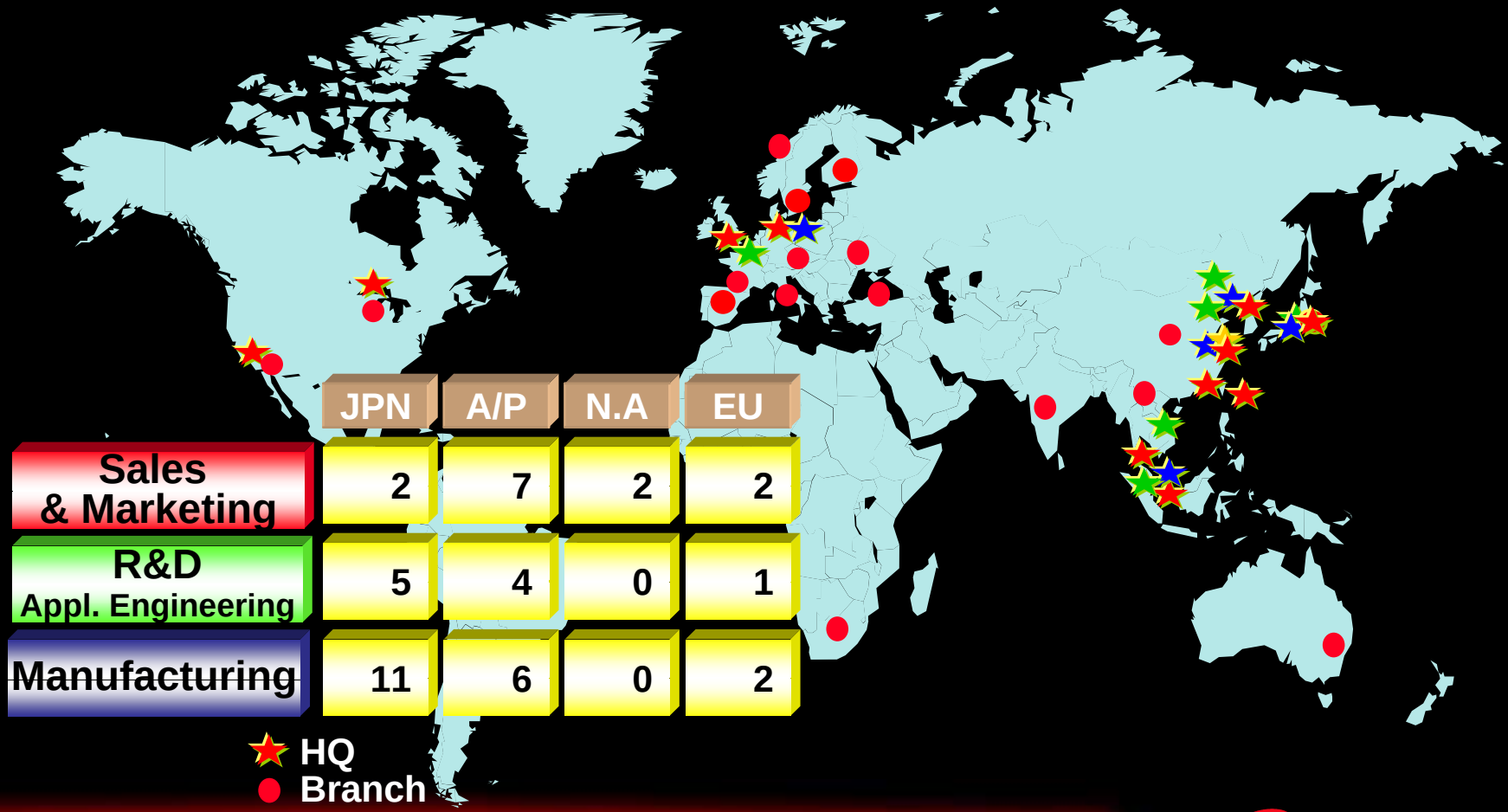
- **Renesas Technology Corp.**
  Renaissance Semiconductor for Advanced Solutions

RENESAS
Everywhere you imagine.

- **Joint venture between Hitachi and Mitsubishi Electric**
  Established on April 1, 2003
- **FY2005 Revenue: 906B¥ (approximately 7.7B$ (117¥/$))**
- **Employee : 26,000 (consolidated as of March 31,2006)**

Renesas Group W/W Network

- Worldwide locations optimized for resources, logistics and markets.
- Shift to Asia for assembly/test and design/development.

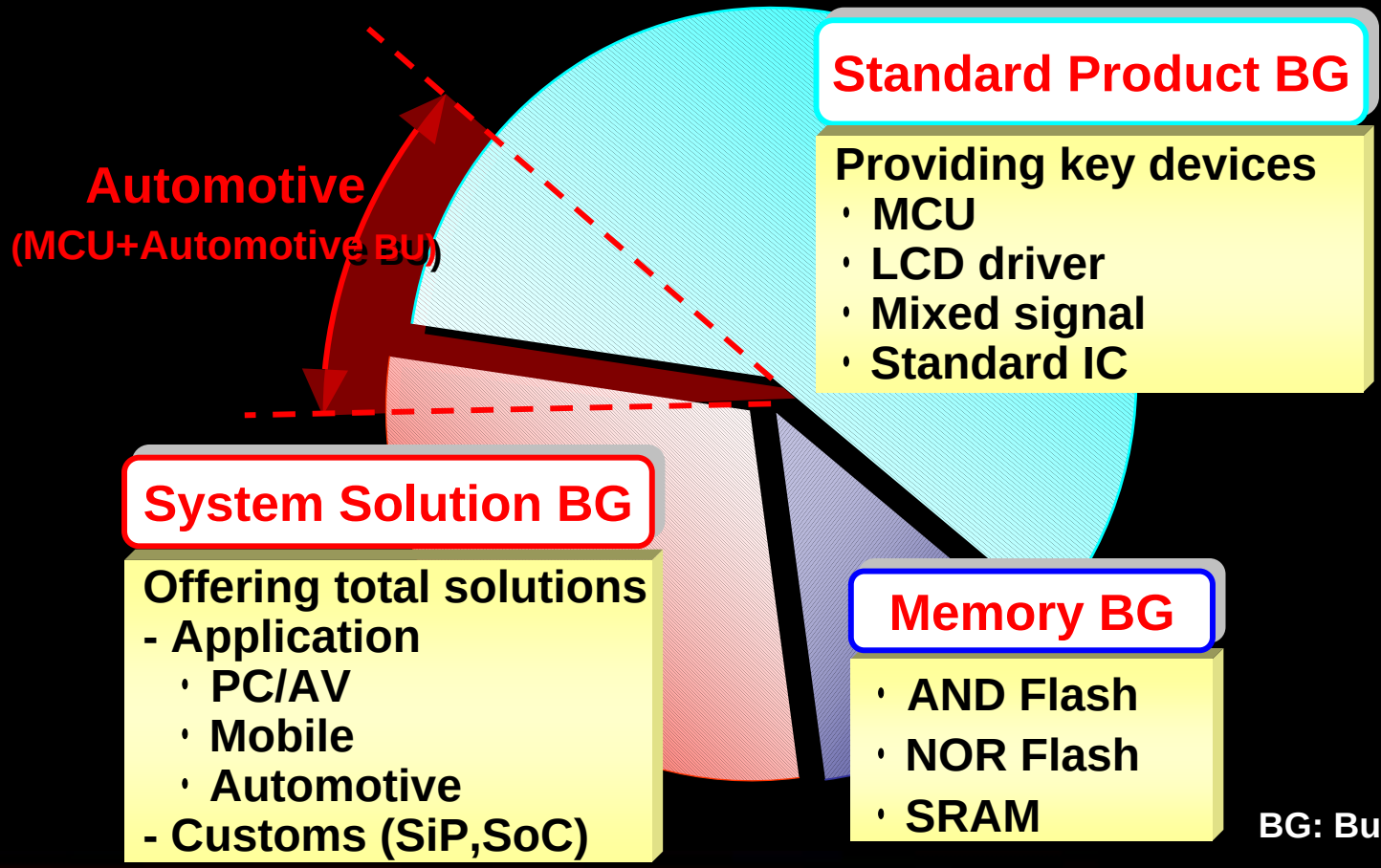


	JPN	A/P	N.A	EU
Sales & Marketing	2	7	2	2
R&D Appl. Engineering	5	4	0	1
Manufacturing	11	6	0	2

HQ
Branch

Renesas Business Structure

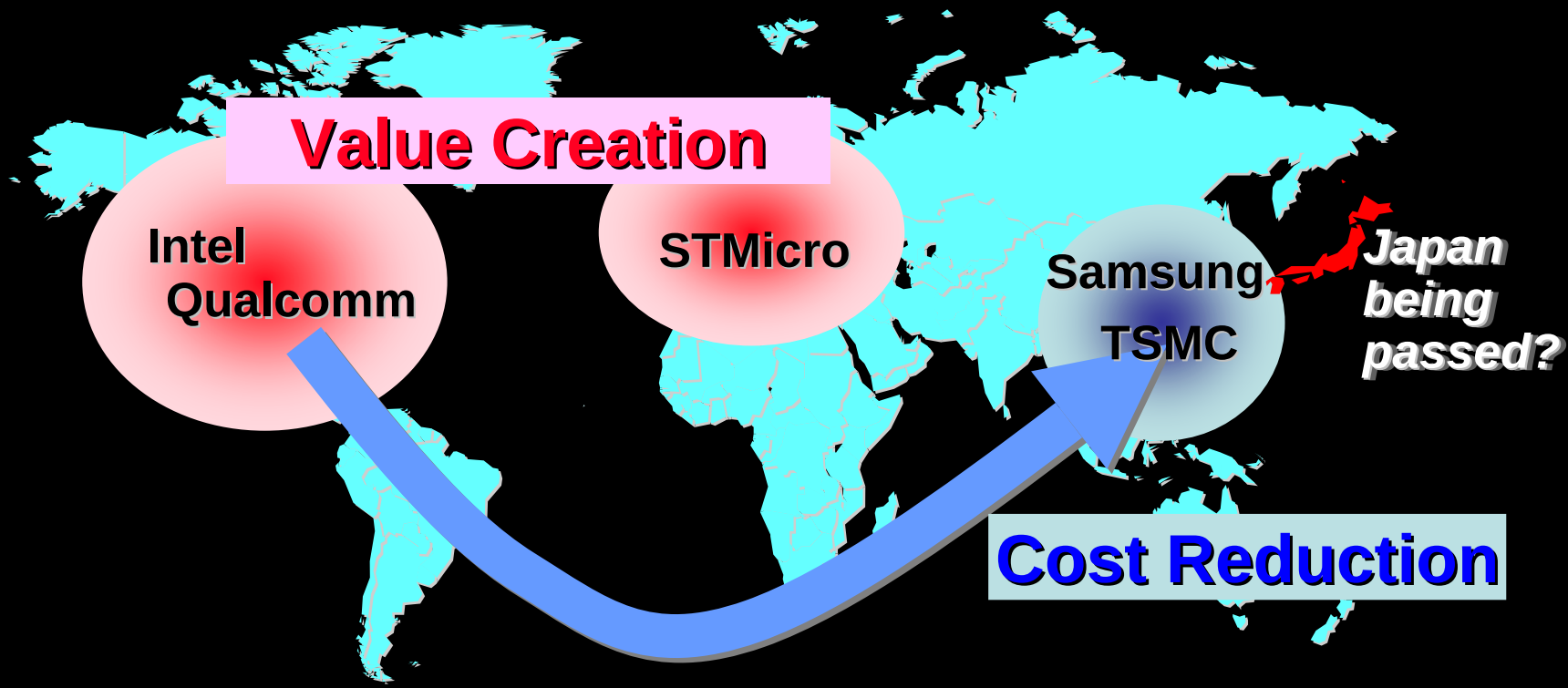
- Two-prong business structure based on the “advanced technology driver” System Solution Business and “fundamental” Standard Product Business.



BG: Business Group

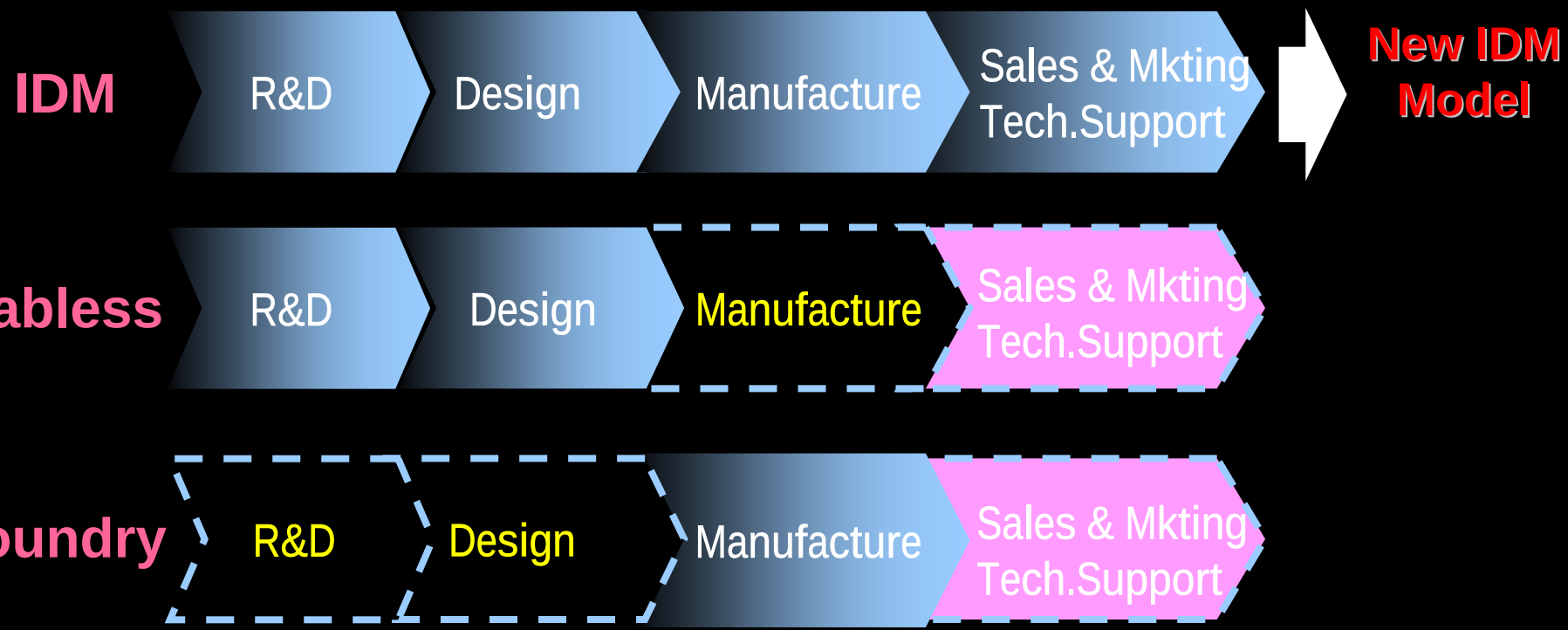
Present Status

- Success of US, Europe, Korea, and Taiwan manufacturers establishing their own business models.
- Japan caught between concepts of "Value Creation" and "Cost Reduction" with no clear business model.



Semiconductor Industrial Business Models

- Value creation has shifted from
  「Silicon」→「Product」→「System」→「Value Chain」
- Traditional IDM model is not suited to the value shift. A new business model is necessary.



*IDM:Integrated Device Manufacturer

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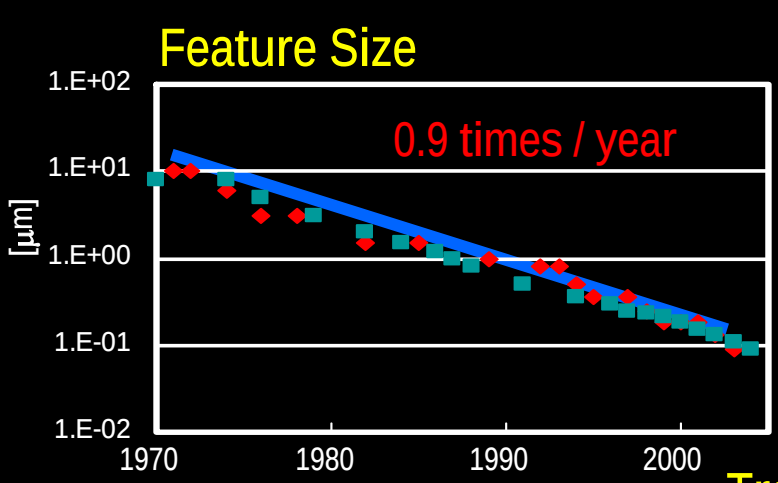
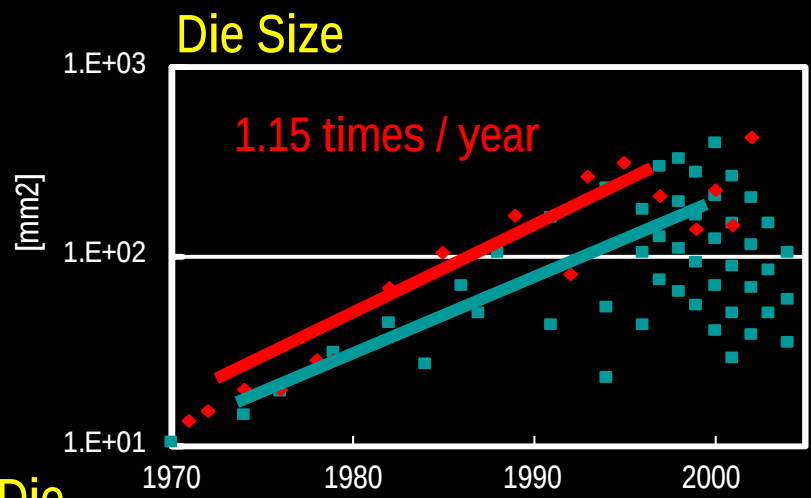
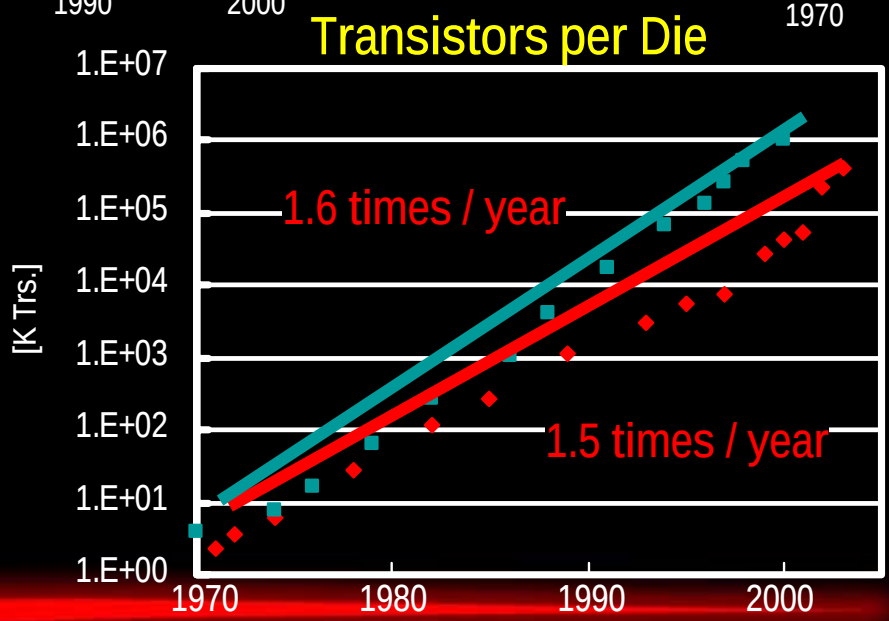
Integration Trends

- "Moore's Law" driven by both "Feature Size" reduction and "Die Size" enlargement.



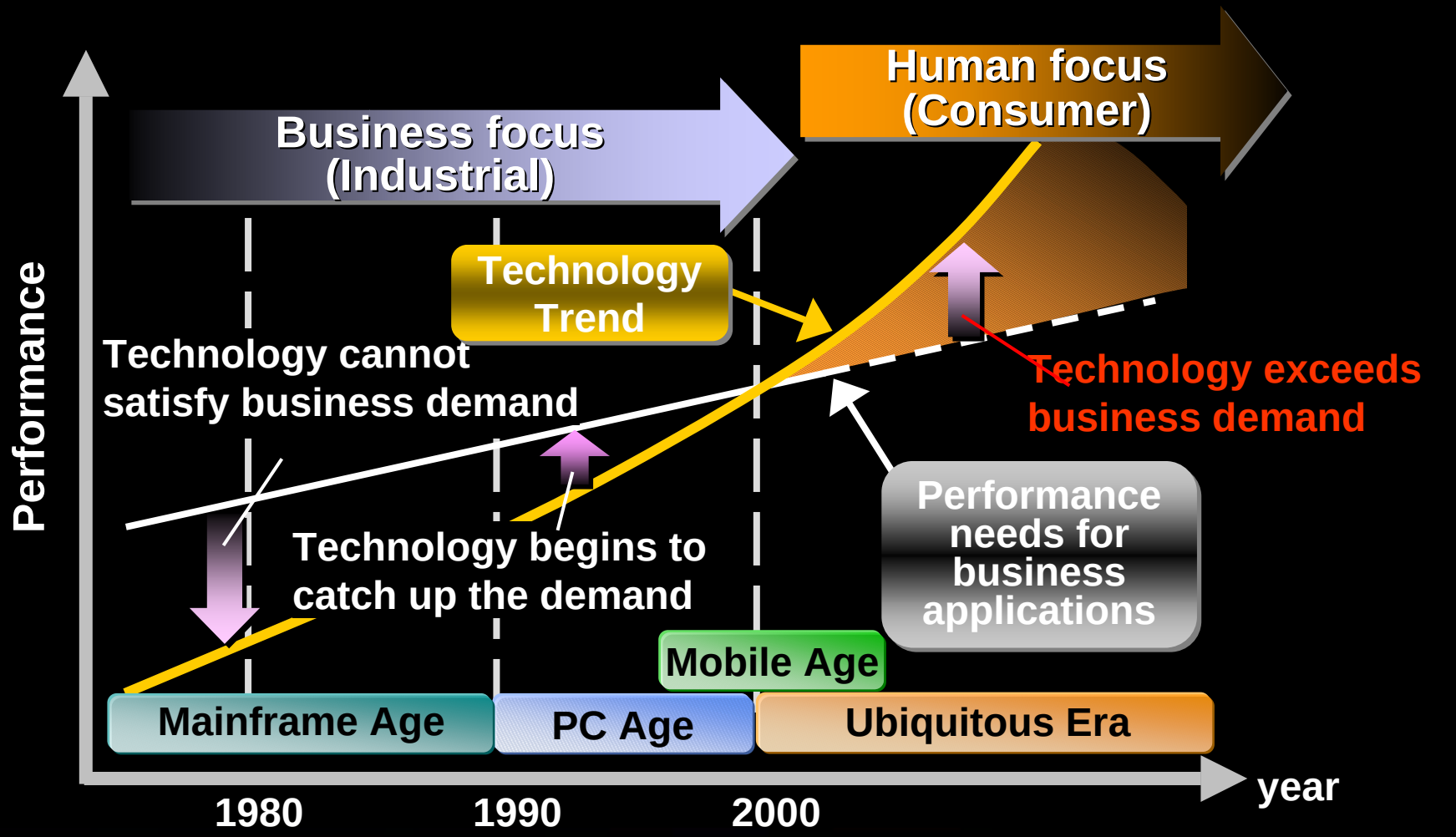




■ : DRAM
◆ : Intel MPU

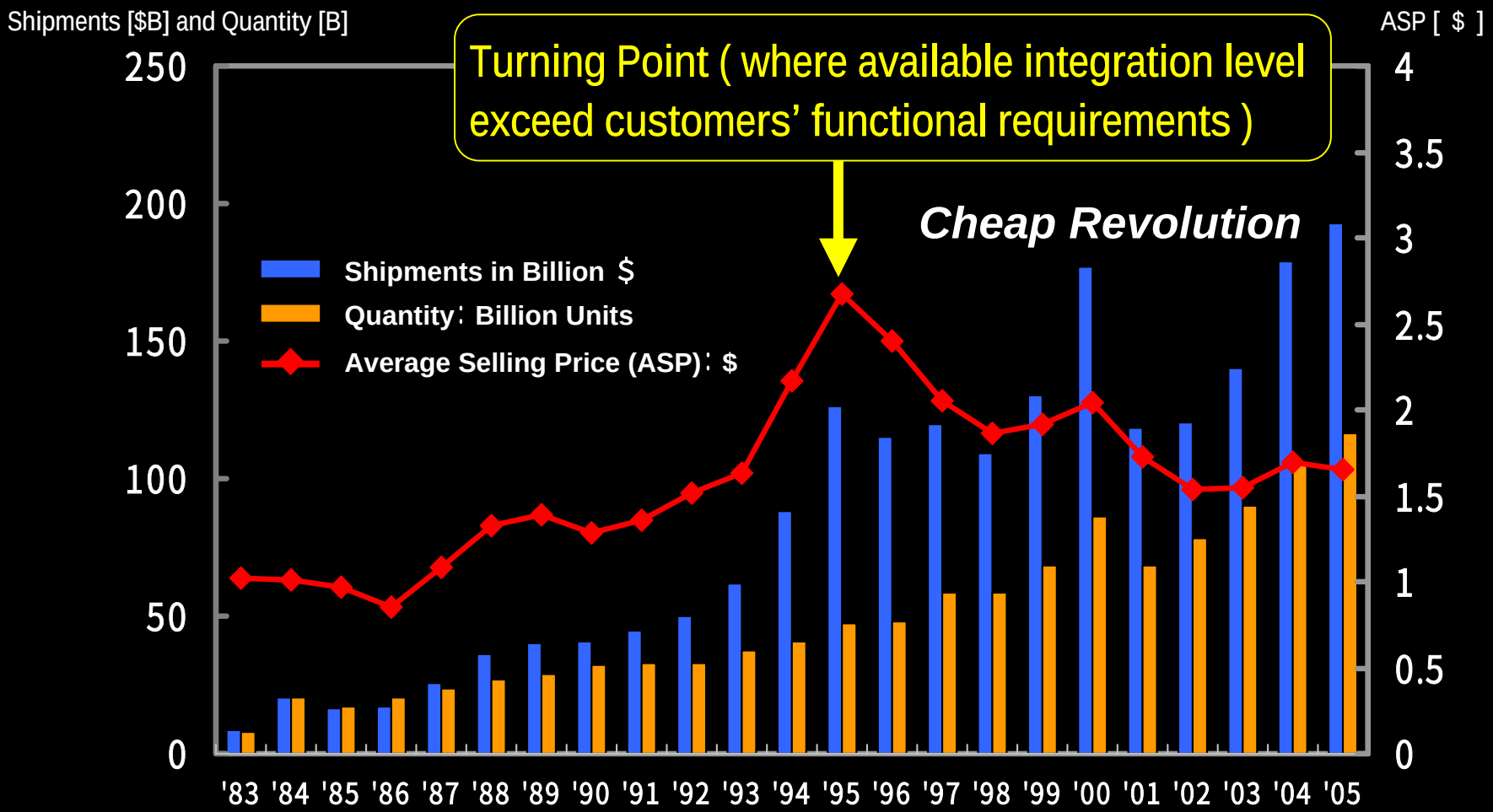
Shifting from Business Focus to Human Focus

- Shifting from performance-oriented business markets to satisfaction-oriented consumer markets



Worldwide IC Shipment & ASP

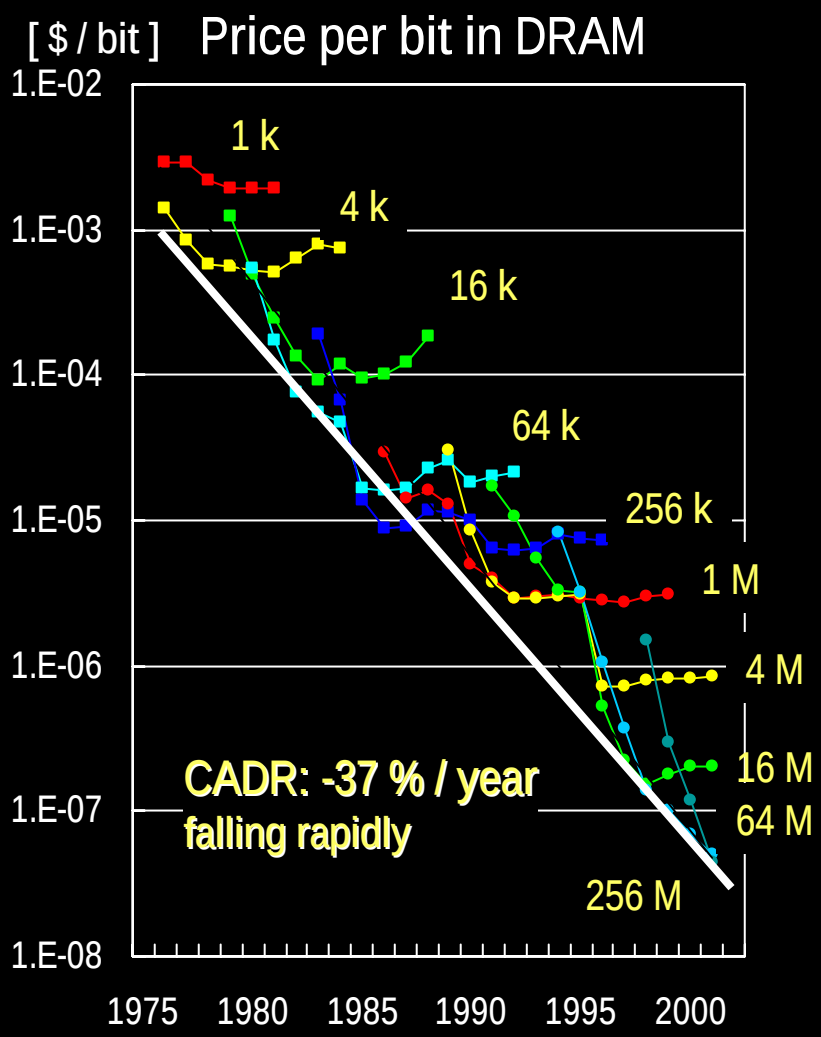
- Market transformed from PC-centric DRAM's and MPU's to widespread IC application.

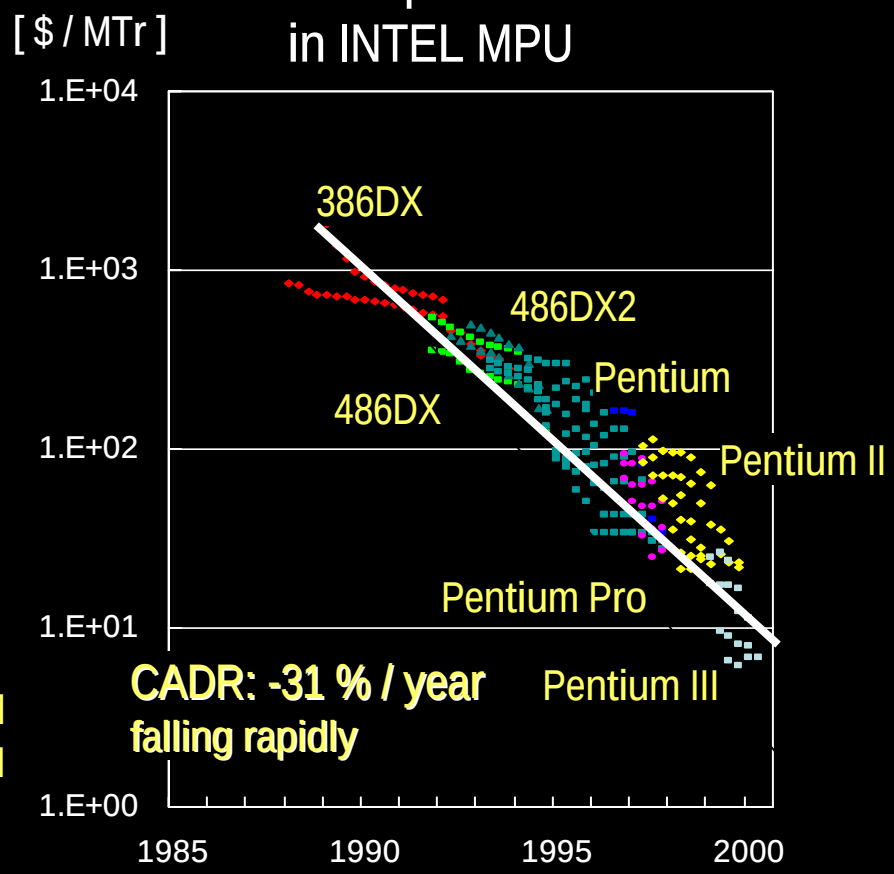


Source: WSTS, SIA

Price per bit, transistor

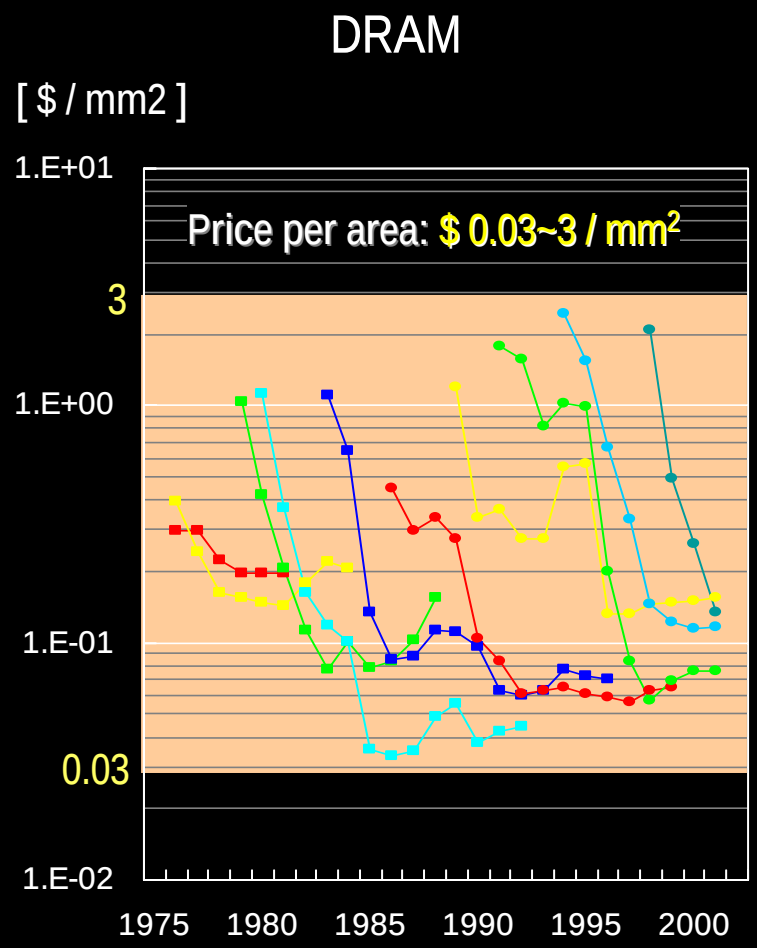
- Price per function has continuously decreased at a constant rate.

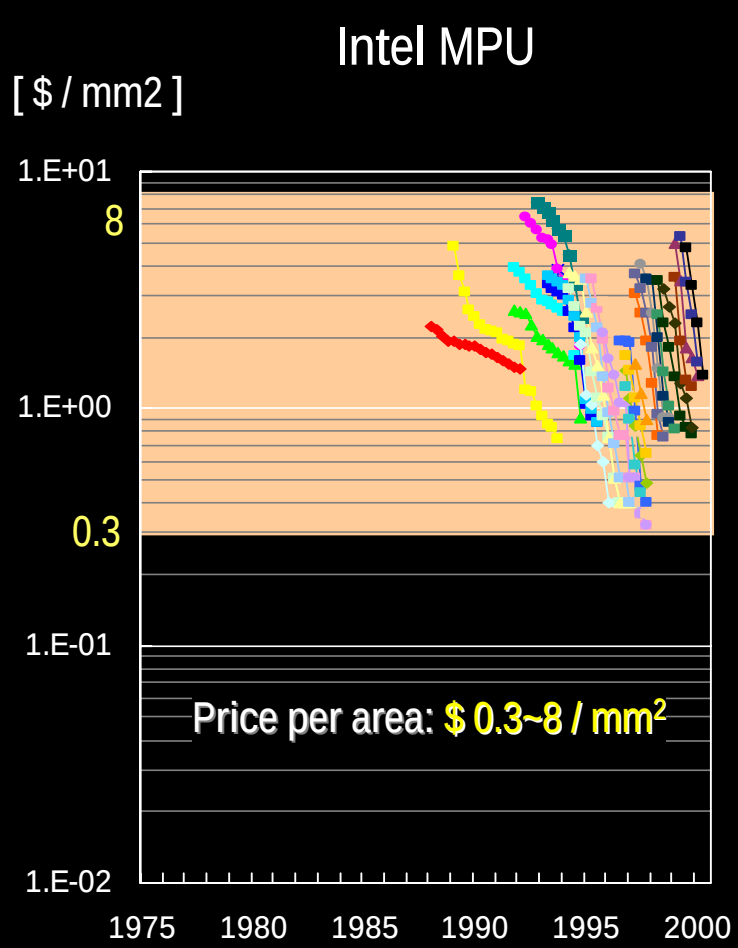




Price per Area

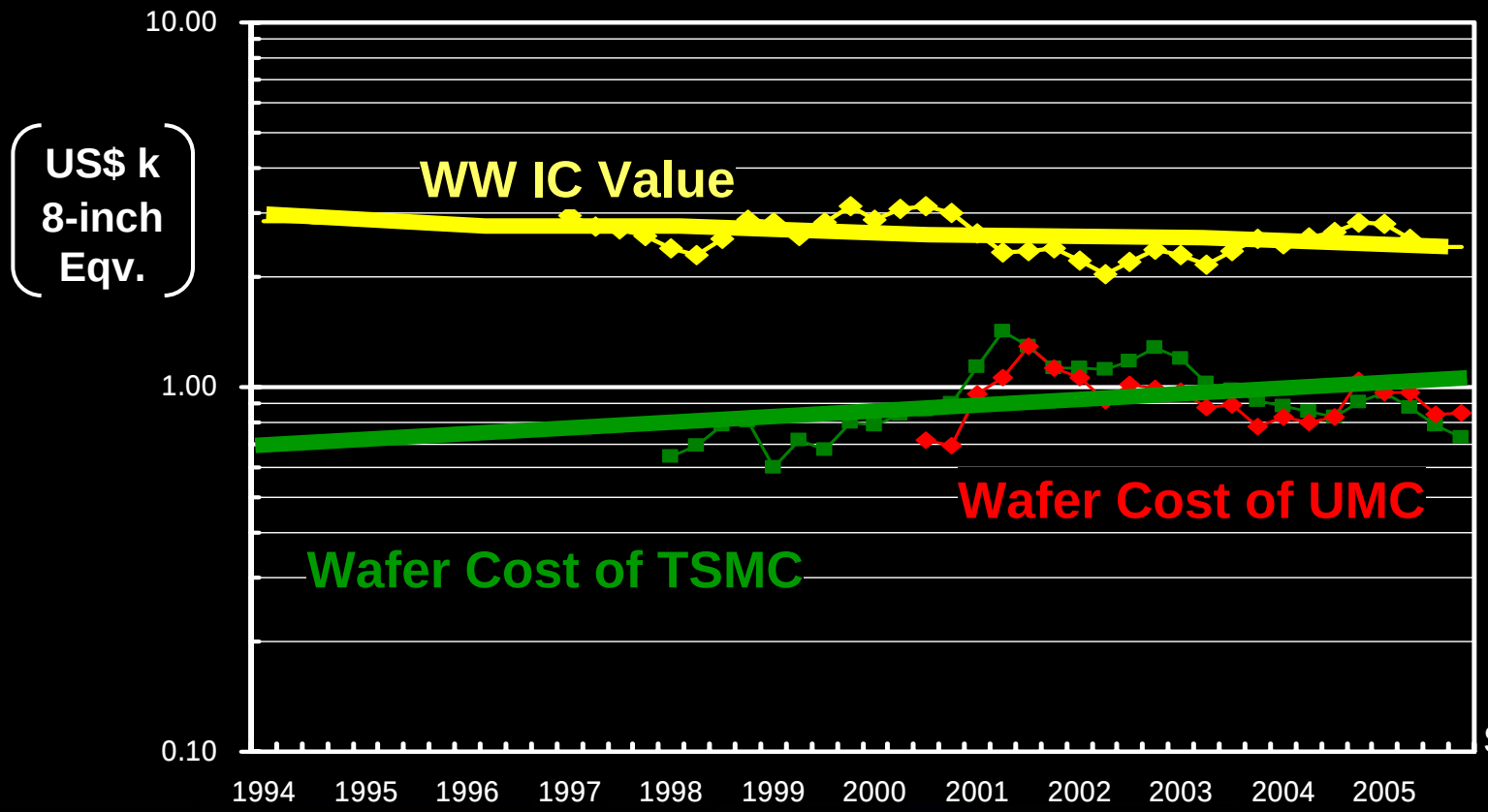
- Price per area has basically settled within a constant range.





Value and Cost Per Wafer (1)

- As a result, value (price) per wafer has remained constant. Processed wafer cost is also generally constant.
- Increase in wafer value is unlikely, and thus there is increasing pressure to reduce design costs.



Source: SIA, TSMC, UMC Web Site

Value and Cost Per Wafer (2)

- For sustainable business, both value and cost per wafer are important issues.

Key Factors Affecting Value Per Wafer

↑ Sophisticated Design Technology

Raise Functionality per Transistor ➡ Increase Product Price

↑ Advanced Process Technology

Reduce Die Size ➡ Increase Gross Number of Dies

↑ Design for Manufacturability

Raise Yield ➡ Increase Good Dies

↓ Price Lowering Pressure from Customers

Key Factors Affecting Cost Per Wafer

↑ Fab Line Investment

↓ Volume Production

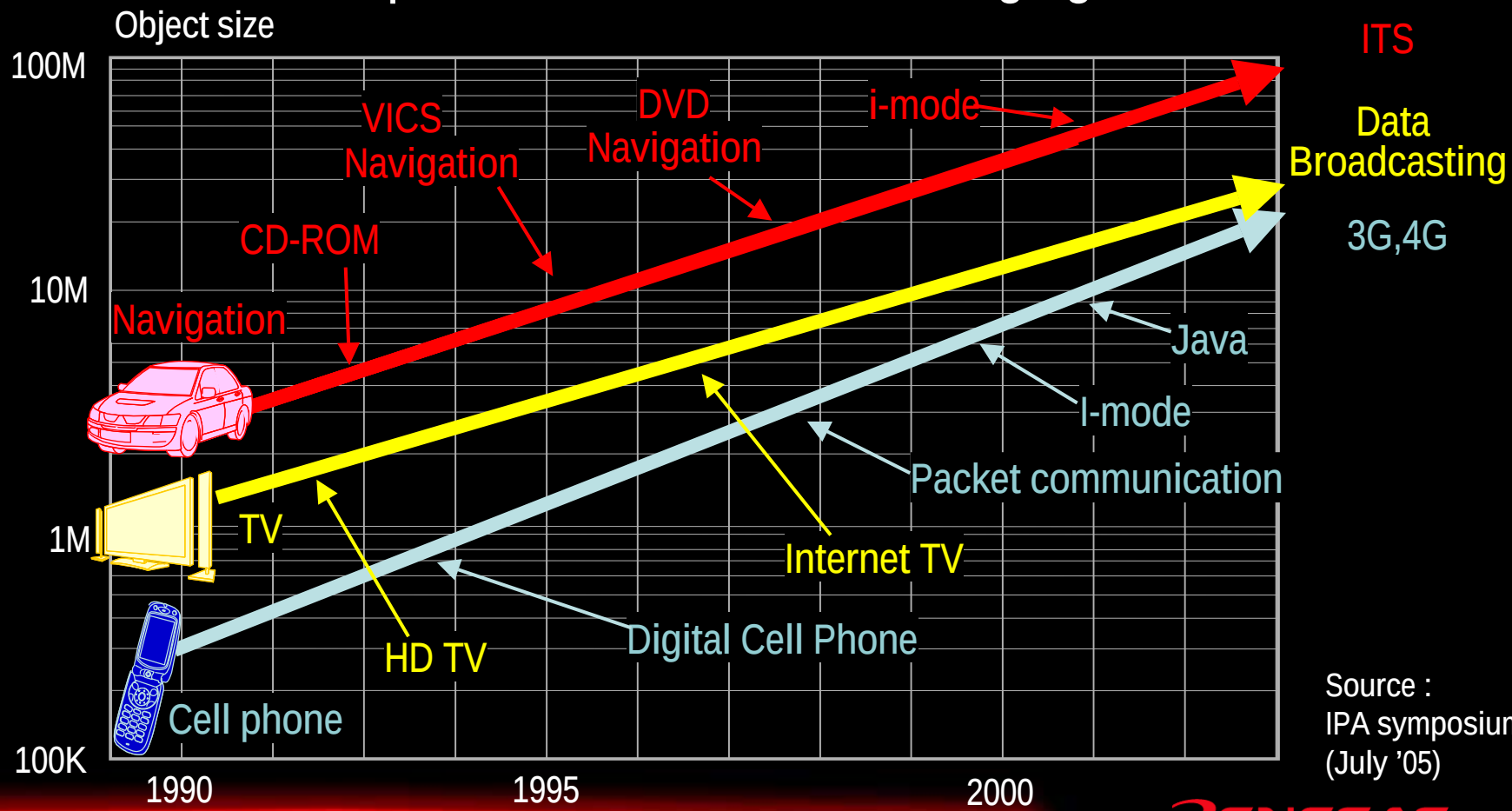
Diversity of Applications but Convergence of Technologies

- In the ubiquitous era, diversity of applications is growing rapidly.
- In contrast, technologies are converging – the same technology is used for a variety of applications.

Multimedia processing
- **High speed Graphics**
- **MPEG, etc.**

Software Development Faces Big Challenges in the Ubiquitous Era

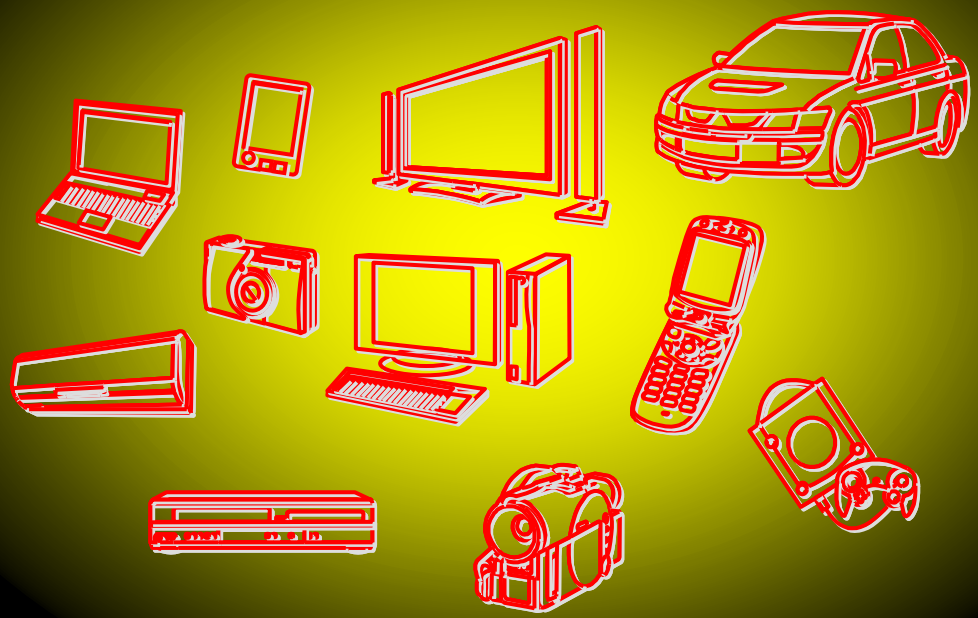
- Applications in the ubiquitous era require a huge volume of software.
- The software explosion will be more challenging than ever.



Source :
IPA symposium
(July '05)

Main Issues Facing The Semiconductor Industry in the Next Decade

Ubiquitous applications



Issues = Needs

- Diversity of Applications
- Convergence of Technologies
- Explosion of Software

And in addition,

- Shortened TTM

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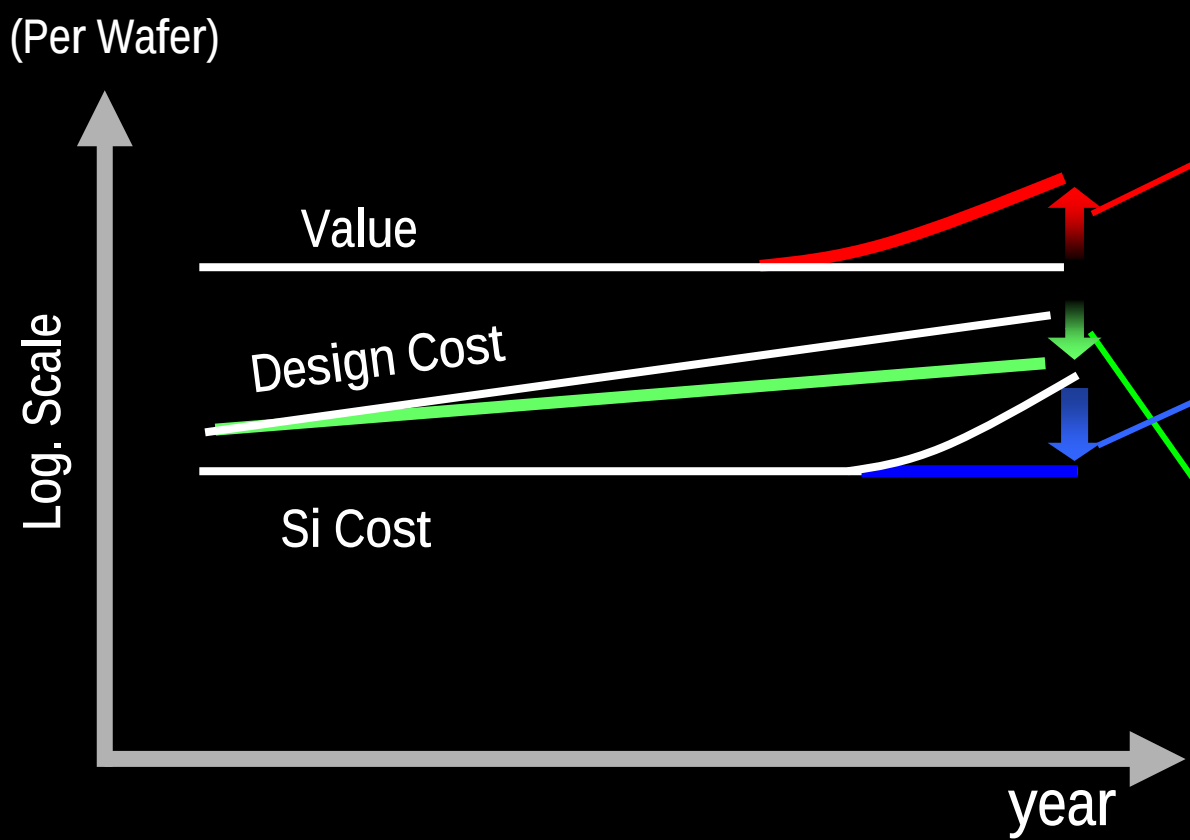
Three Challenges



Challenge 1

To raise value per wafer

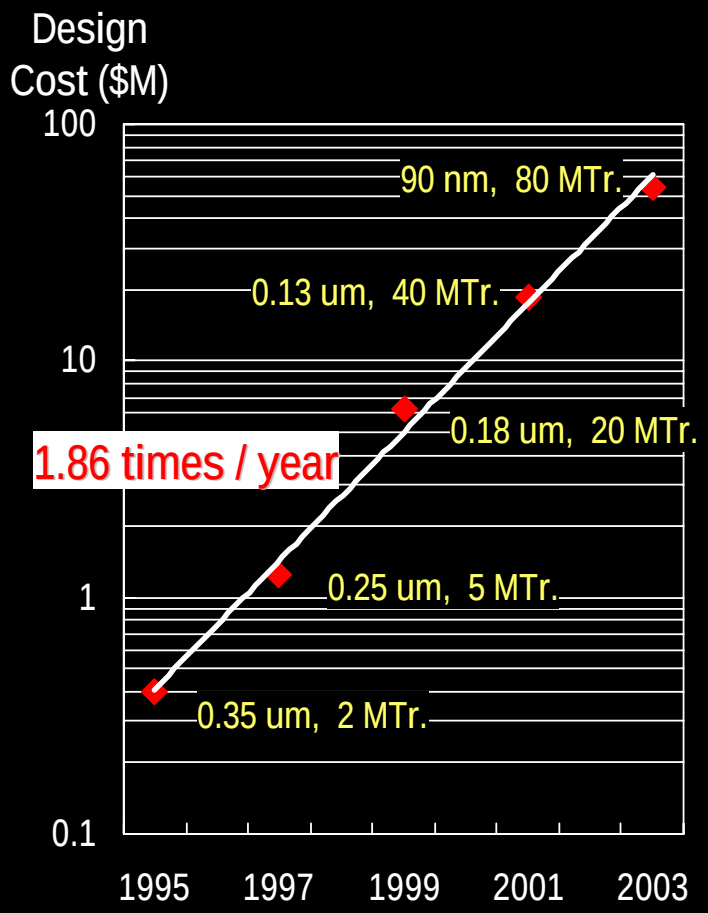
Challenge 2

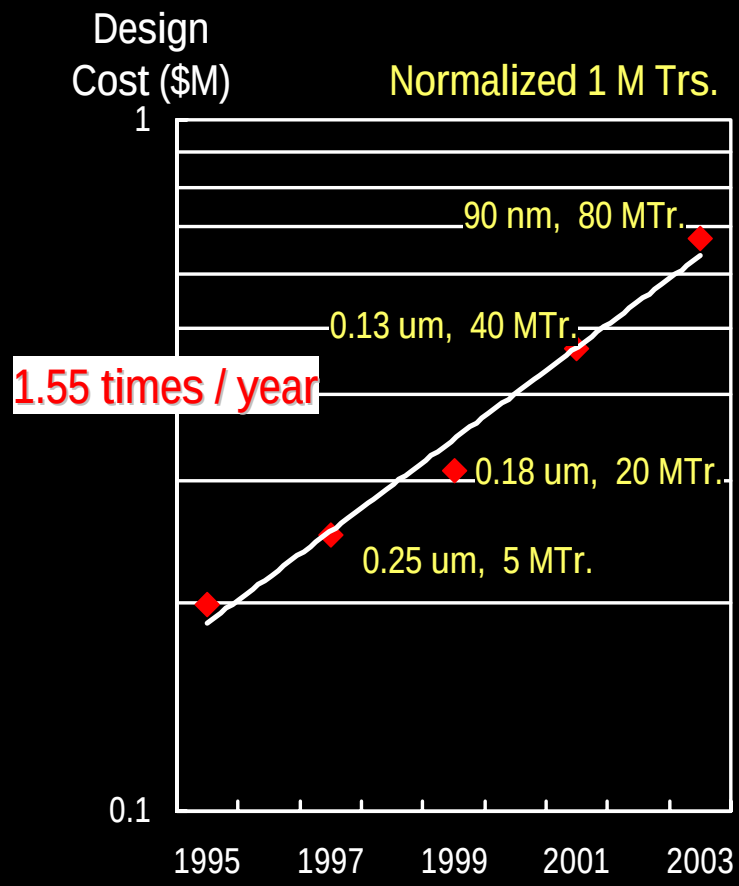
To reduce cost of silicon

Challenge 3

To reduce design cost

Design Cost Trends

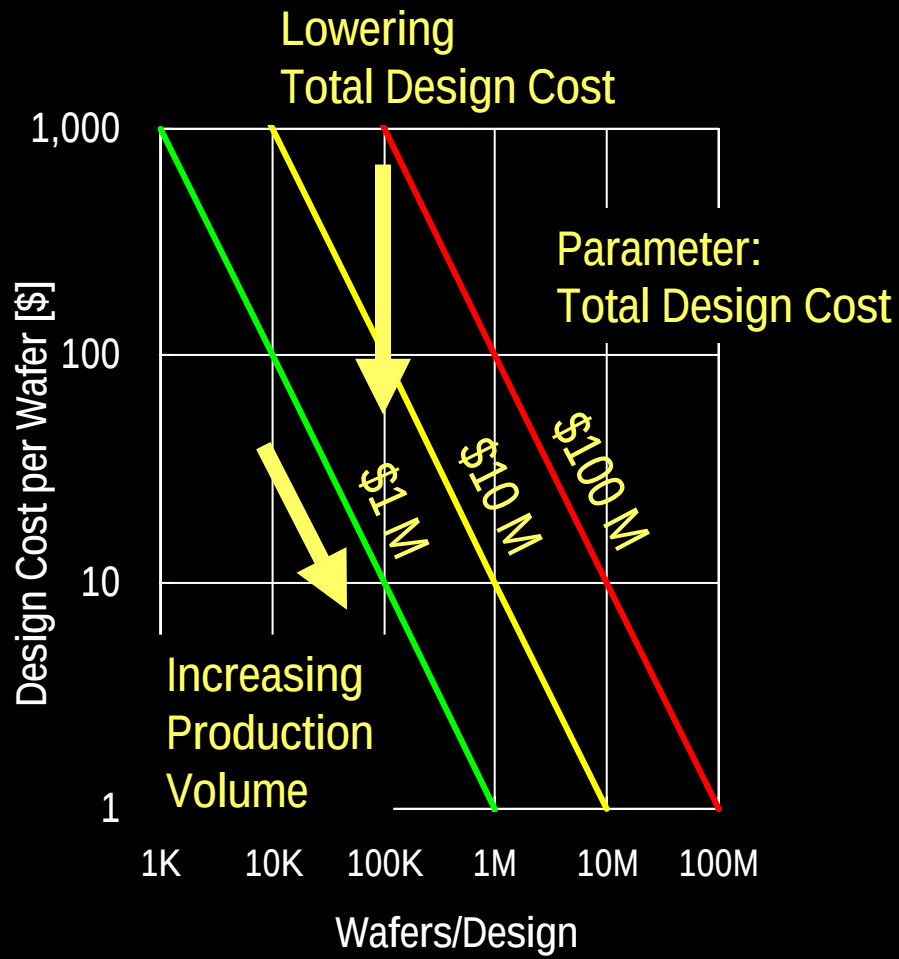




Source : IBS 2003

Design Cost per Wafer

- Design cost per wafer decreases with increase in number of produced wafers.
- Total design cost increases with design scale increase and usage of advanced process technologies
- Total design cost must be lowered to retain profitability at lower production levels.



Challenges for Design Cost Reduction

Challenges	Renesas Countermeasures
Increasing Revenue per Design	■ System Level Platform EXREAL Platform for H/W and S/W design (EXcellent Reliability Efficiency Agility Link platform)
	■ Re-Configurable Devices
Lowering Cost per Design	■ Design Environment / EDA Tools REAP (REnesas Advanced design Platform) : for SoC / MCU design ARES (Advanced REnesas mixed signal design System) for mixed signal LSI design
	■ Engineering Resources Open global design centers Increase skill of design engineers

Platform and Re-configurables increase Revenue per Design

Diversity of Application

- Reduction of development time
- Squeeze development cost

Application Oriented Platform

- Easily customized hardware and software
- Effective utilization of design assets

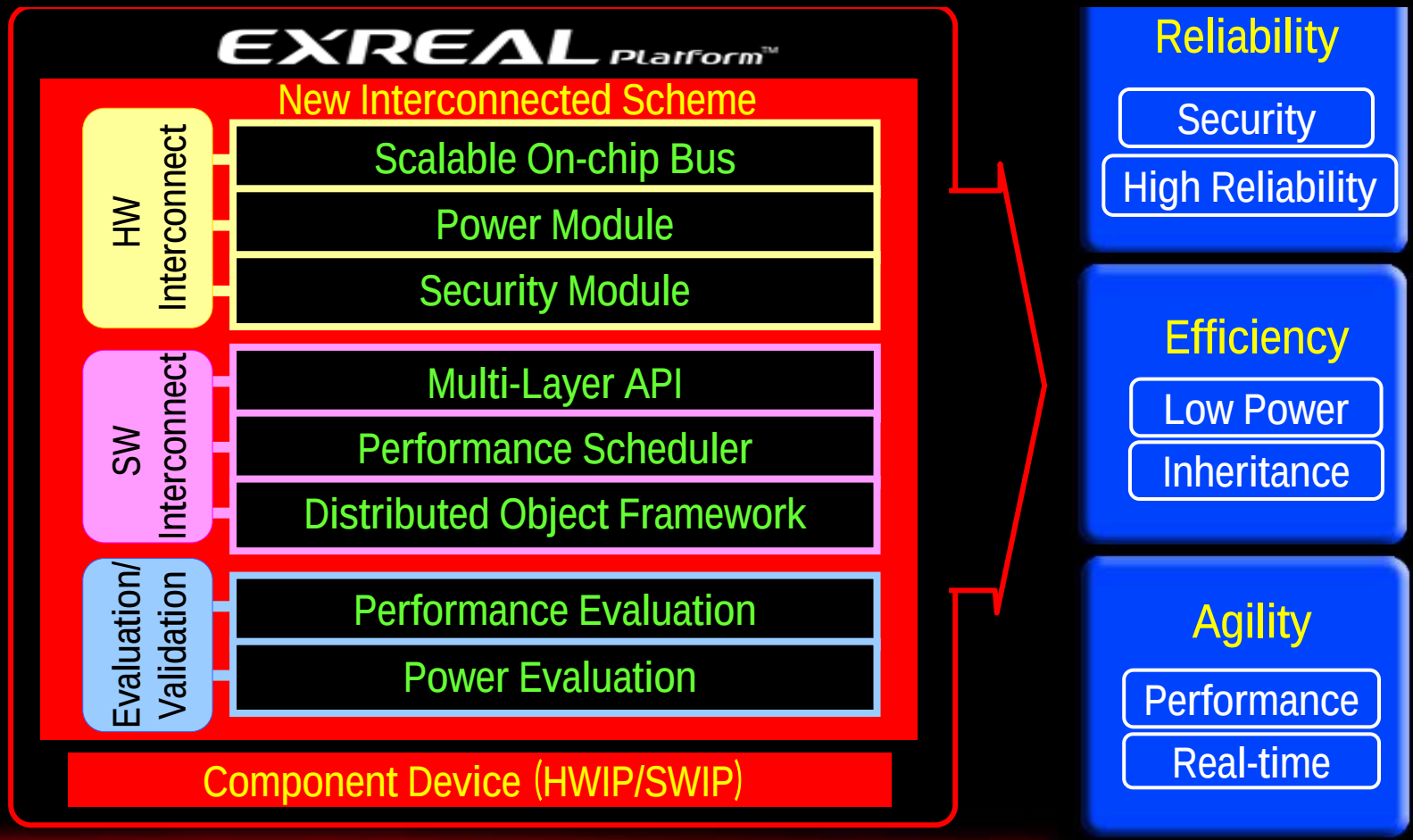
Reconfigurable Devices

- Capability of hardware swap after device mounting
- One device covers multiple designs

EXREAL Platform ™

EXREAL: EXcellent Reliability Efficiency Agility Link platform

- Dramatically reduced development time and increased software development efficiency
- High performance and usability with a new interconnected scheme



Innovation in the EXREAL Platform ™

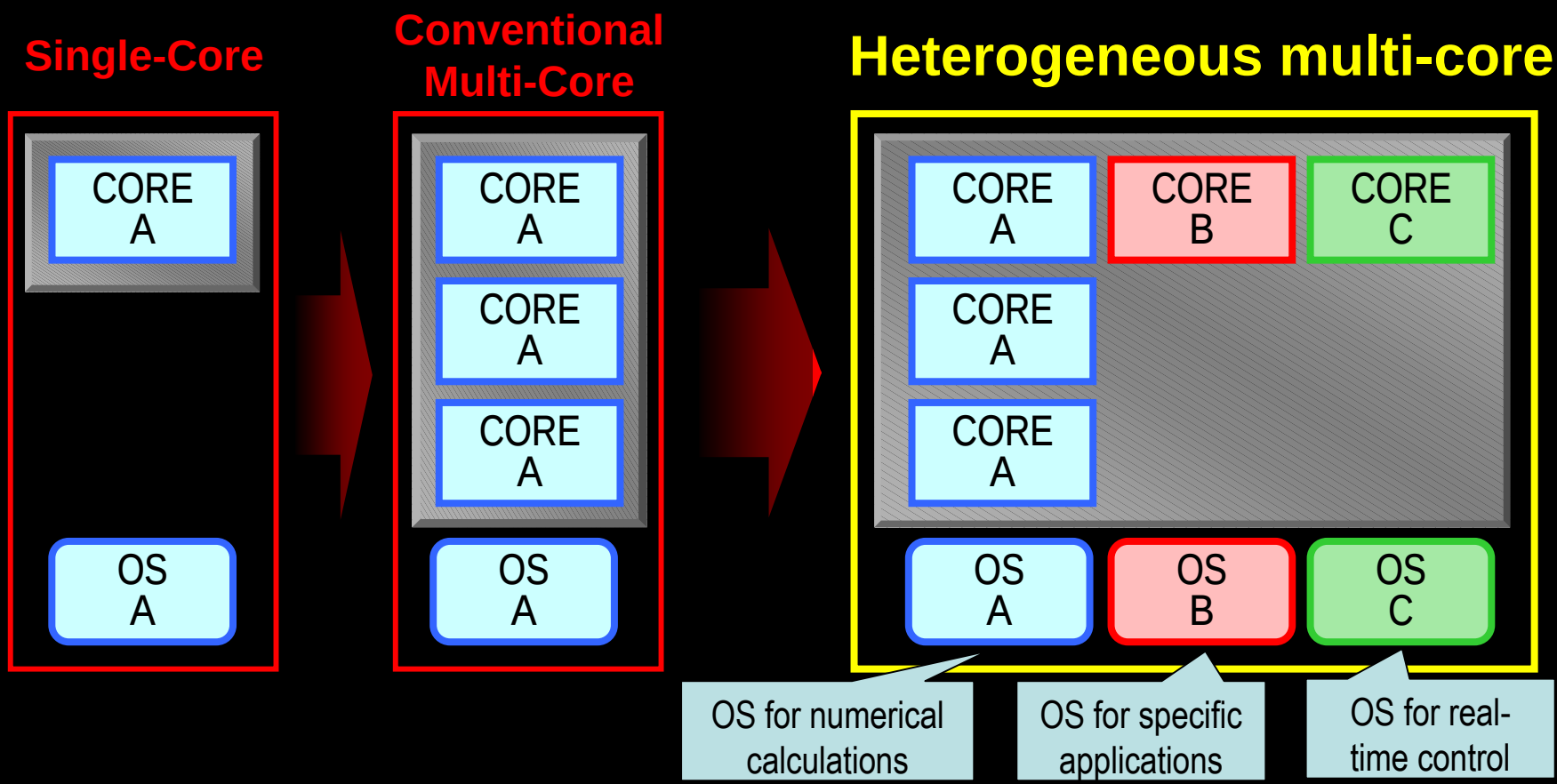
- In response to application diversity, there are four innovative features in the EXREAL platform:

Inheritance and High Portability	●Availability of past assets of software and hardware ●High portability of existing assets and hardware IP
Flexible Scalability	●Improvement of performance using scalable CPU/IP and reliability ●Reduction of power
Heterogeneous Architecture	●Optimized performance, cost, flexibility and development period by heterogeneous configuration with diverse cores
Convergence	●Reuse of modules between platforms

Shorten development time of new LSI's and
realize dramatic improvement in development efficiency

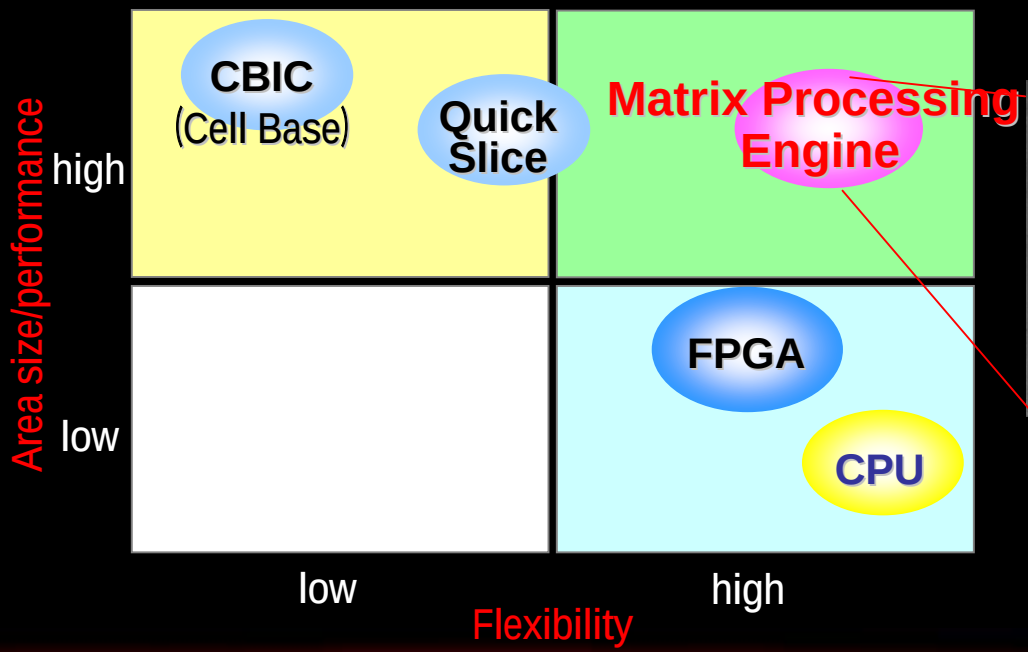
EXREAL Platform™ Design Example:
Heterogeneous Multi-Core Concept

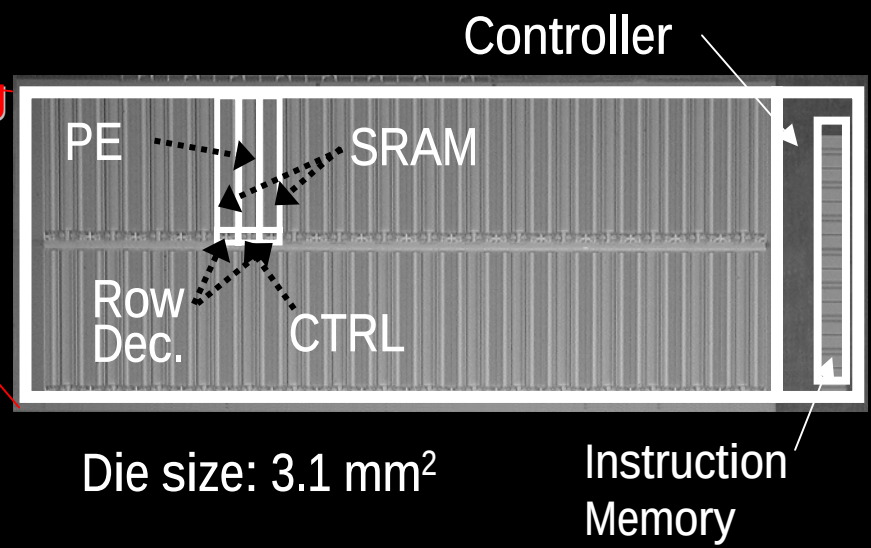
- Heterogeneous multi-cores offer higher performance with optimized core and OS implementation



Reconfigurable Device Example

- New Renesas reconfigurable device concept: Reconfigurable processor core
- Massively parallel processor based on a matrix configuration
  - Configurable PE (Processing Elements) which meet various "Multimedia data standards"
  - 160 GOPS/W (40 GOPS at 250mW) performance achieved



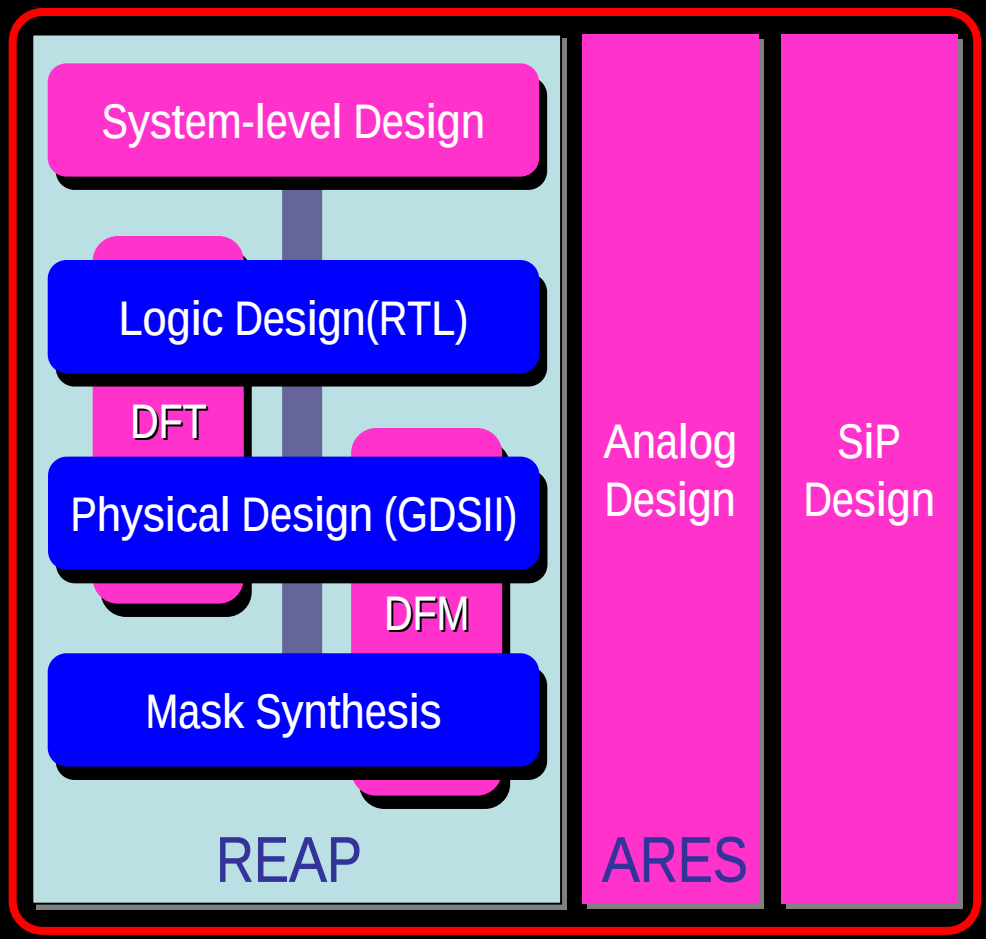


Die size: 3.1 mm^2

Source: 2006 ISSCC 22.5

Unified Design Environment / EDA Tools

- Renesas developed a unified design environment from separate Hitachi and Mitsubishi environments in one year.



Design Cost Reduction

- System-level Design
- Analog Design
- SiP (System in Package) Design

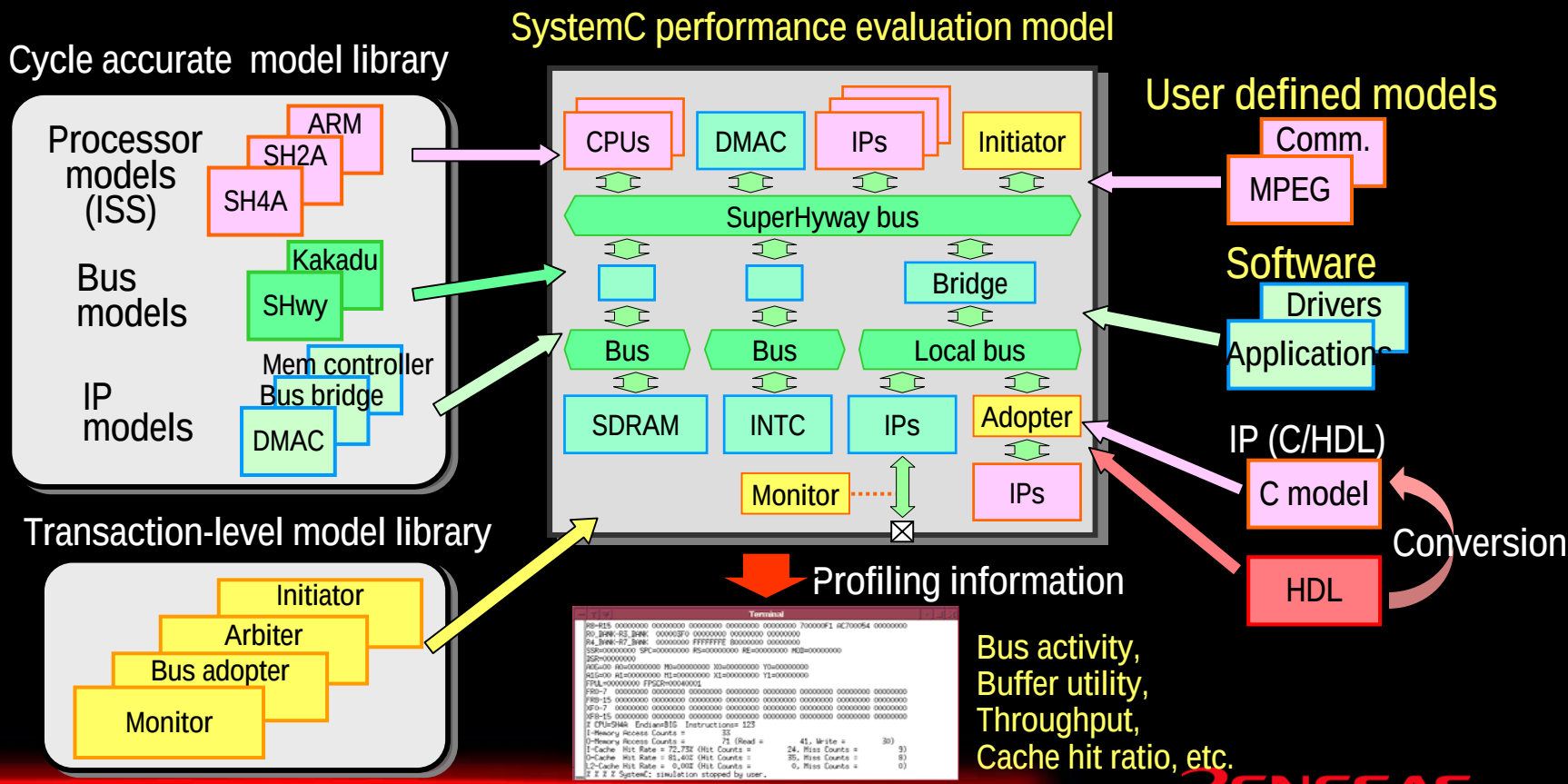
Silicon Cost Reduction

- DFM (Design For Manufacturability)
- DFT (Design For Test)

REAP (REnesas Advanced design Platform) : for SoC / MCU
ARES (Advanced REnesas mixed signal design System) : for mixed signal LSI

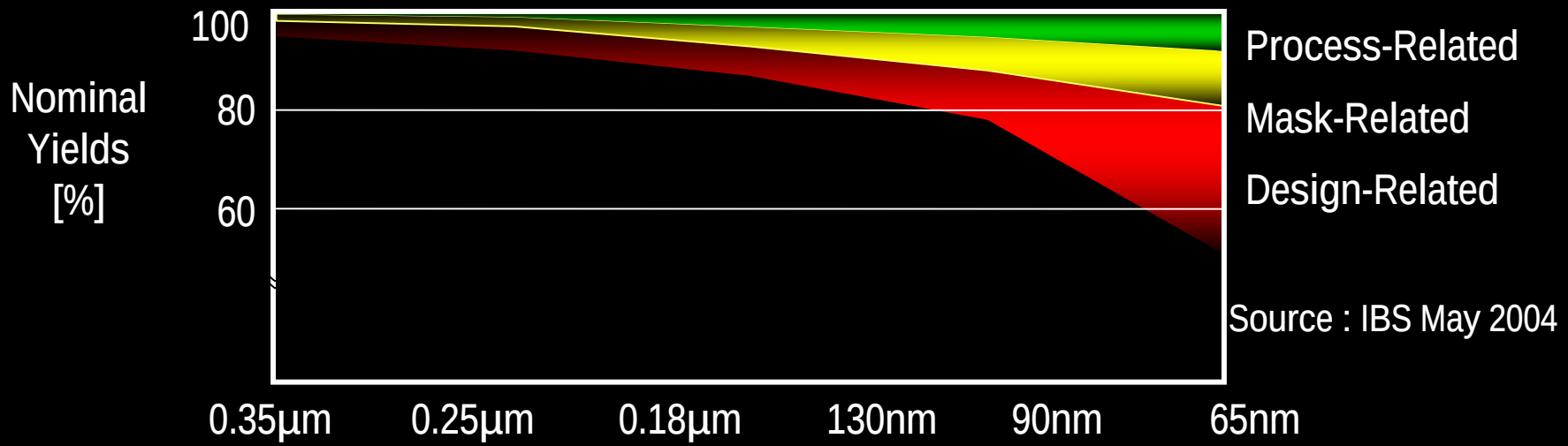
System Level Design

- SoC's have become more and more complex. Multiple CPUs, legacy or 3rd-party IP's, etc., all integrated on one chip.
- Accuracy and short turn-around-time is required for performance evaluation and power estimation during architecture exploration.



DFM (Design For Manufacturability)

- DFM is crucial to prevent yield decrease due to miniaturization



Process Technology

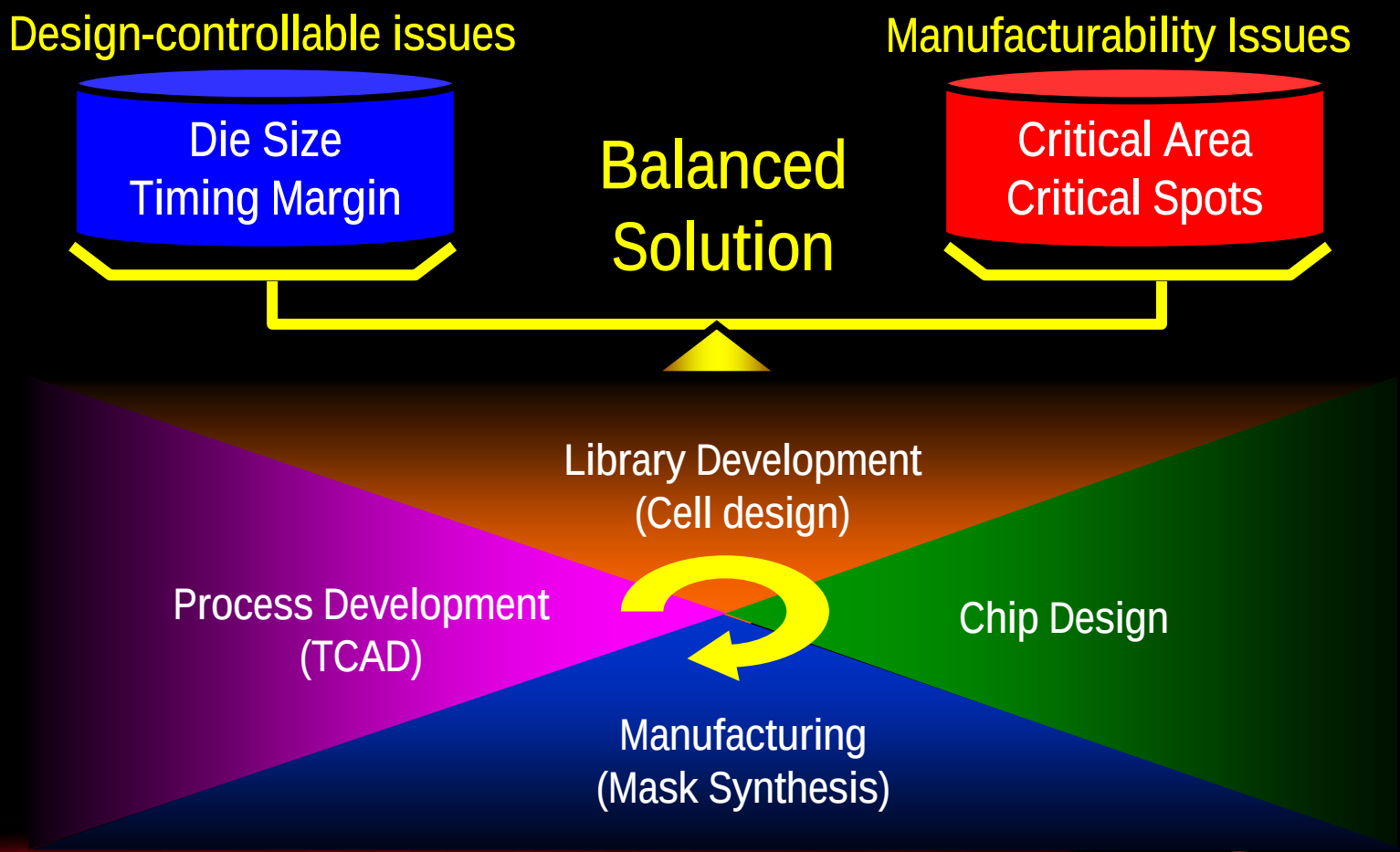
CMP(Chemical Mechanical Polishing) for Multi-level Interconnect

OPC(Optical Proximity Correction) for Design Rule < Wave Length

DFM

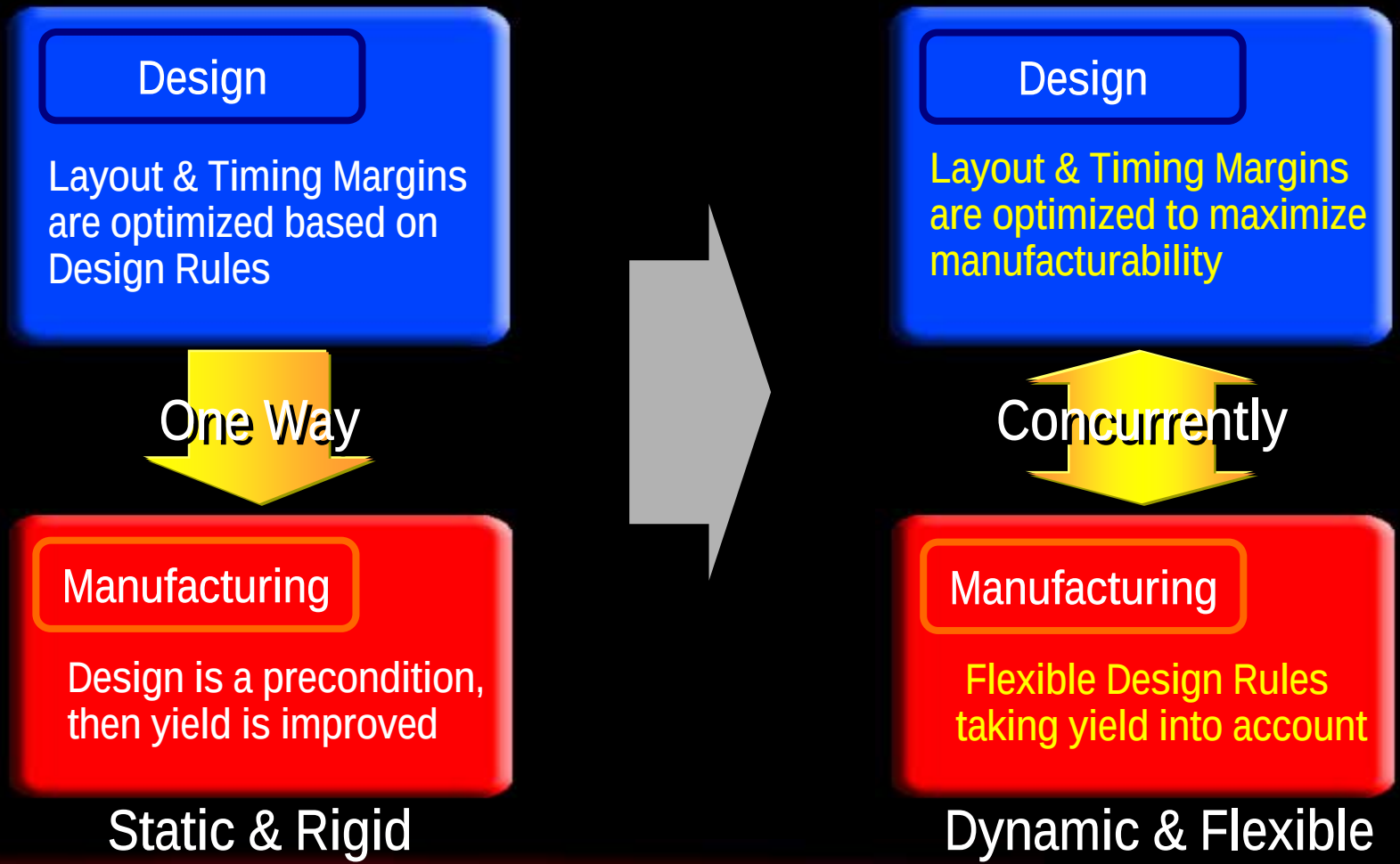
DFM (Design For Manufacturability)

- Design-controllable issues (Die Size, etc.) and manufacturability are trade-offs.
- Balanced solution maximizes wafer value.



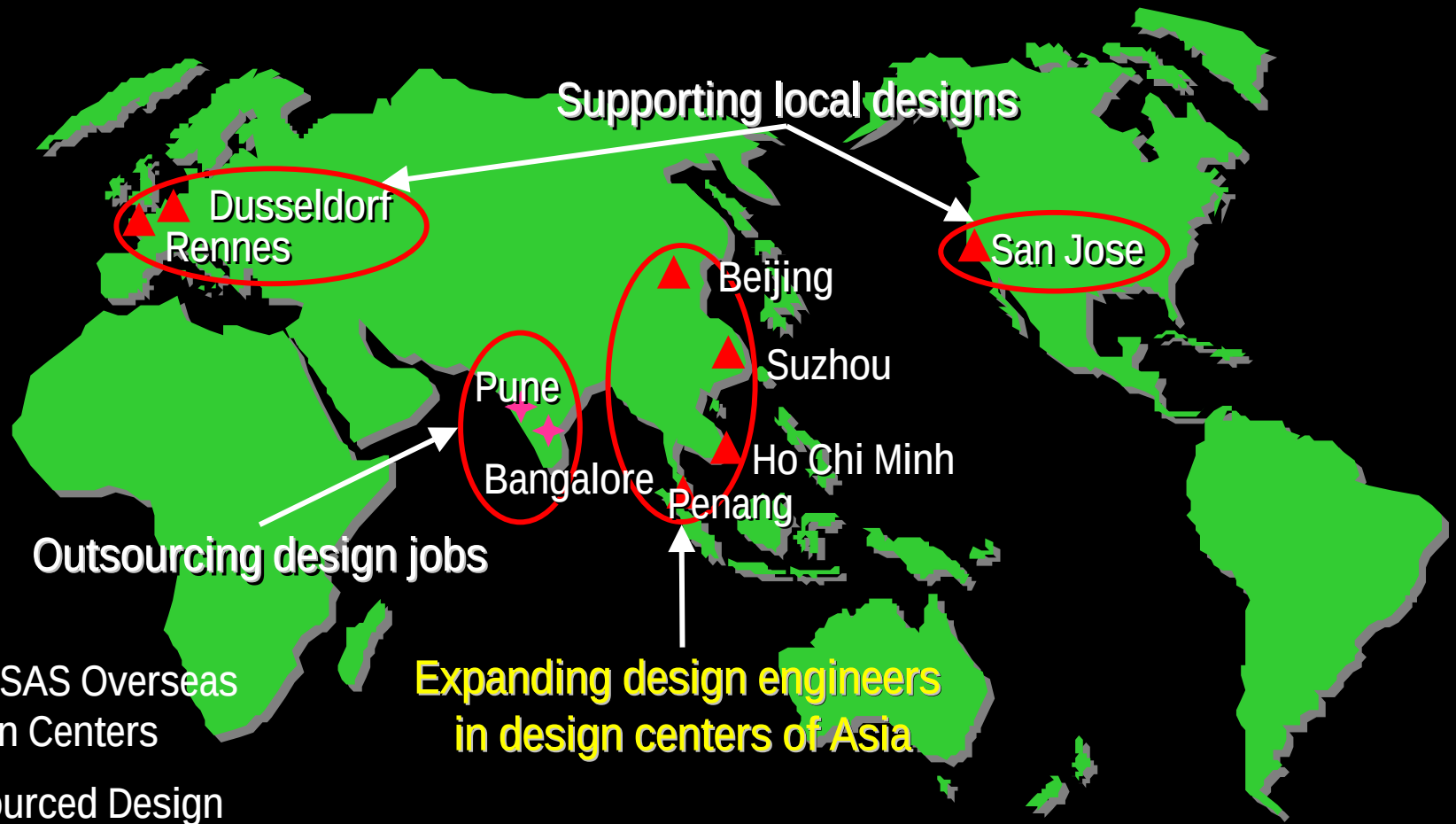
Designer Collaboration is the Key for Advanced Technologies

- Design & Manufacturing Scheme shifting from “Static & Rigid” to “Dynamic & Flexible”



RENESAS Overseas Design Centers

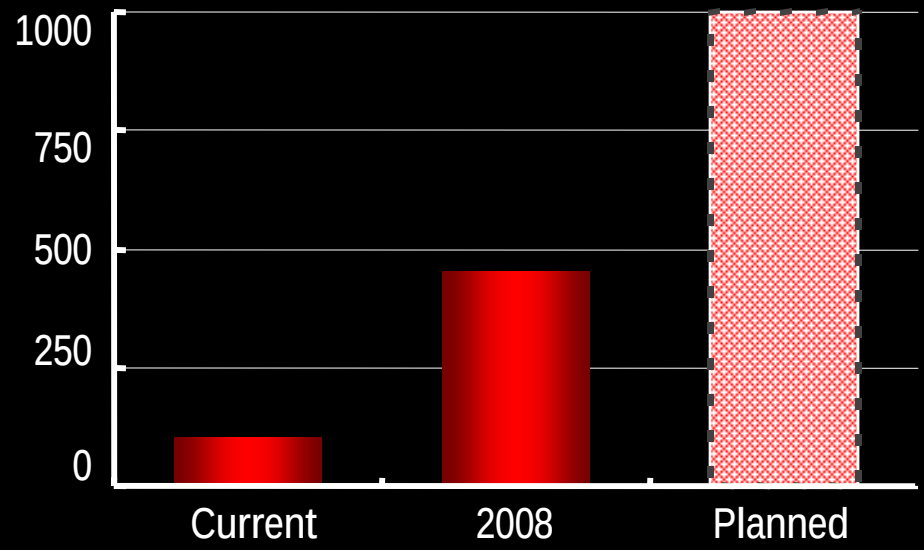
- Due to EDA tool advancement and proliferation, close links between global design centers possible.



Renesas Design Vietnam

- The first LSI design center in Vietnam
- One of the best locations for LSI design
- Networking & EDA enabling optimized design environment

New Building
under Construction



No. of Designers

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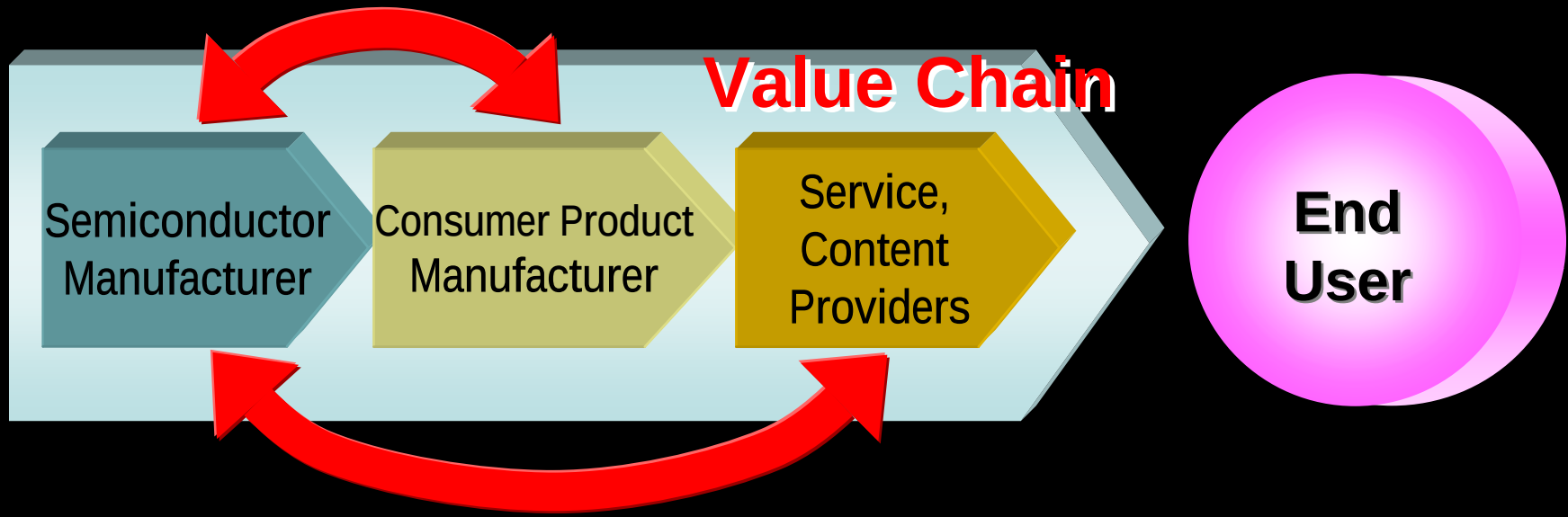
Renesas System Solutions Business Strategy

- Close cooperation not only with consumer product manufacturers but beyond (Service,Content Providers) is the Key



Automotive

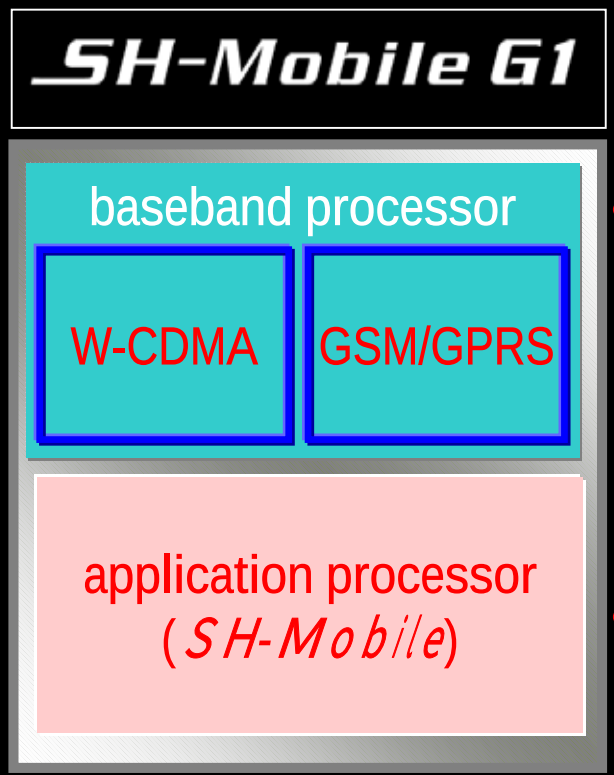
Close relationships with Toyota, Nissan, and other automotive companies. Involvement in consortiums (AUTOSAR,JASPER).

Cellular

Cooperation with carrier design service infrastructure. Setting up SH-Mobile and other consortiums.

SH-Mobile G1: Mass Production in Q1/FY06

- Jointly developed with NTT DoCoMo and realized an highly-integrated LSI by using the EXREAL Platform™
- To be used in FOMA handsets from Fujitsu, Mitsubishi Electric, and Sharp



- Integrated 2 baseband processors and an application processor
  - 90nm node
  - Operating frequency: 312MHz
- Highly integrated LSI chip of 180M transistors

Handset Makers

Fujitsu

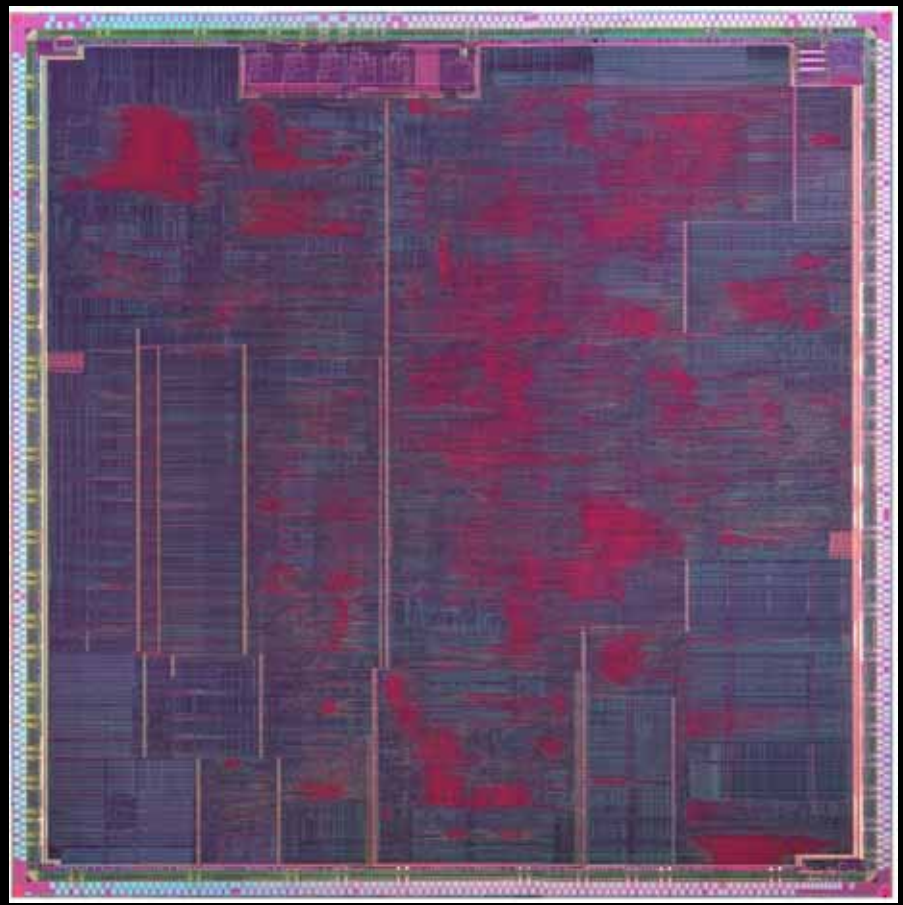
Mitsubishi Elec.

Sharp

SH-Mobile (G1) Chip Photo

SH-Mobile G1

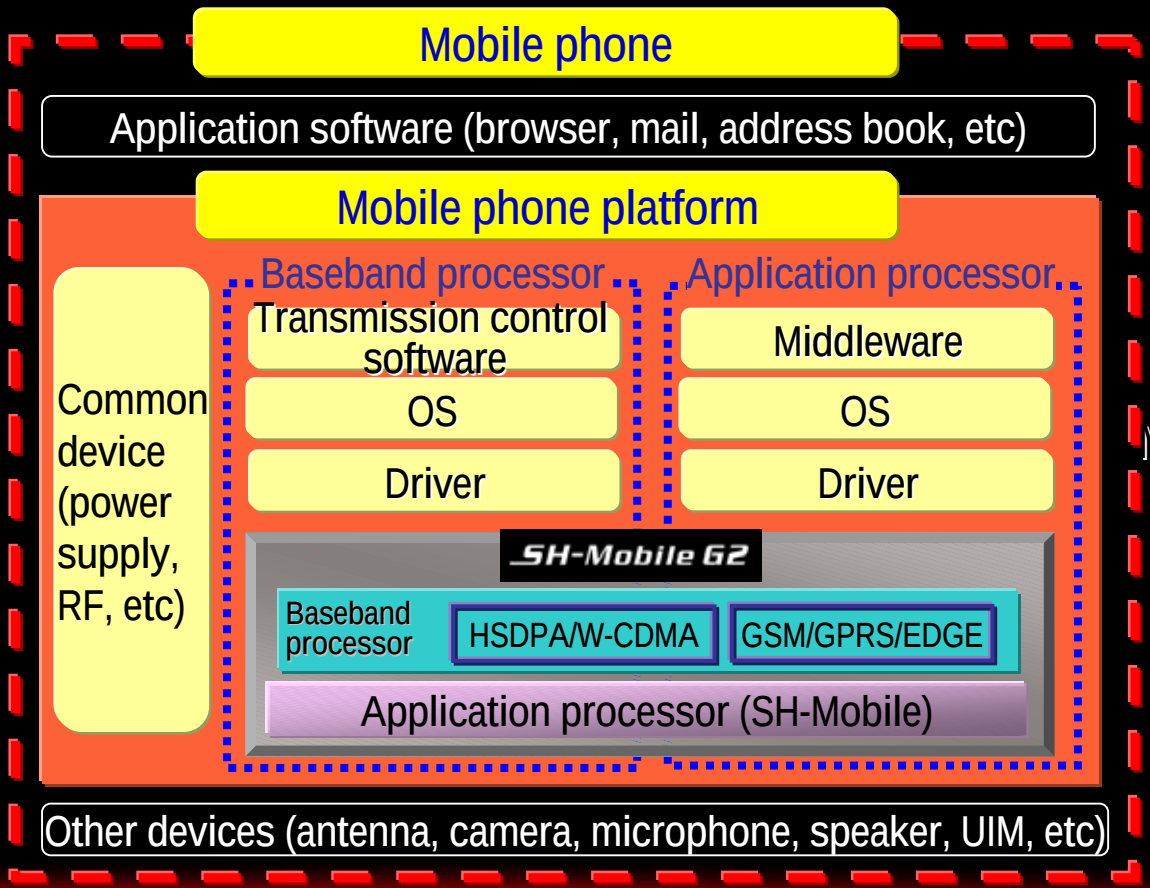
- Though highly integrated, we achieved 1st Silicon success
- Development period reduced to two-thirds (18 to 12 months)

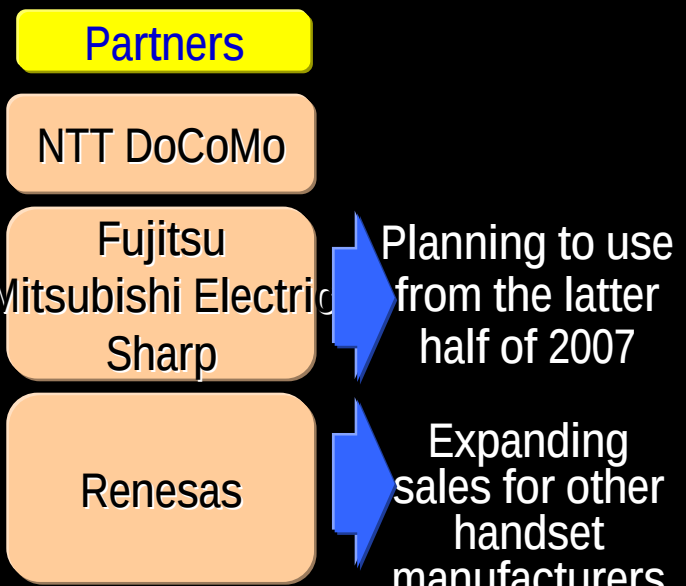


- Die size : 11.15mm x 11.15mm
- # of TRs : 181M TRs
  (13.5M gates, 20Mbit memories)
- Process: 90nm LP

2nd Phase Development: Mobile Phone Platform

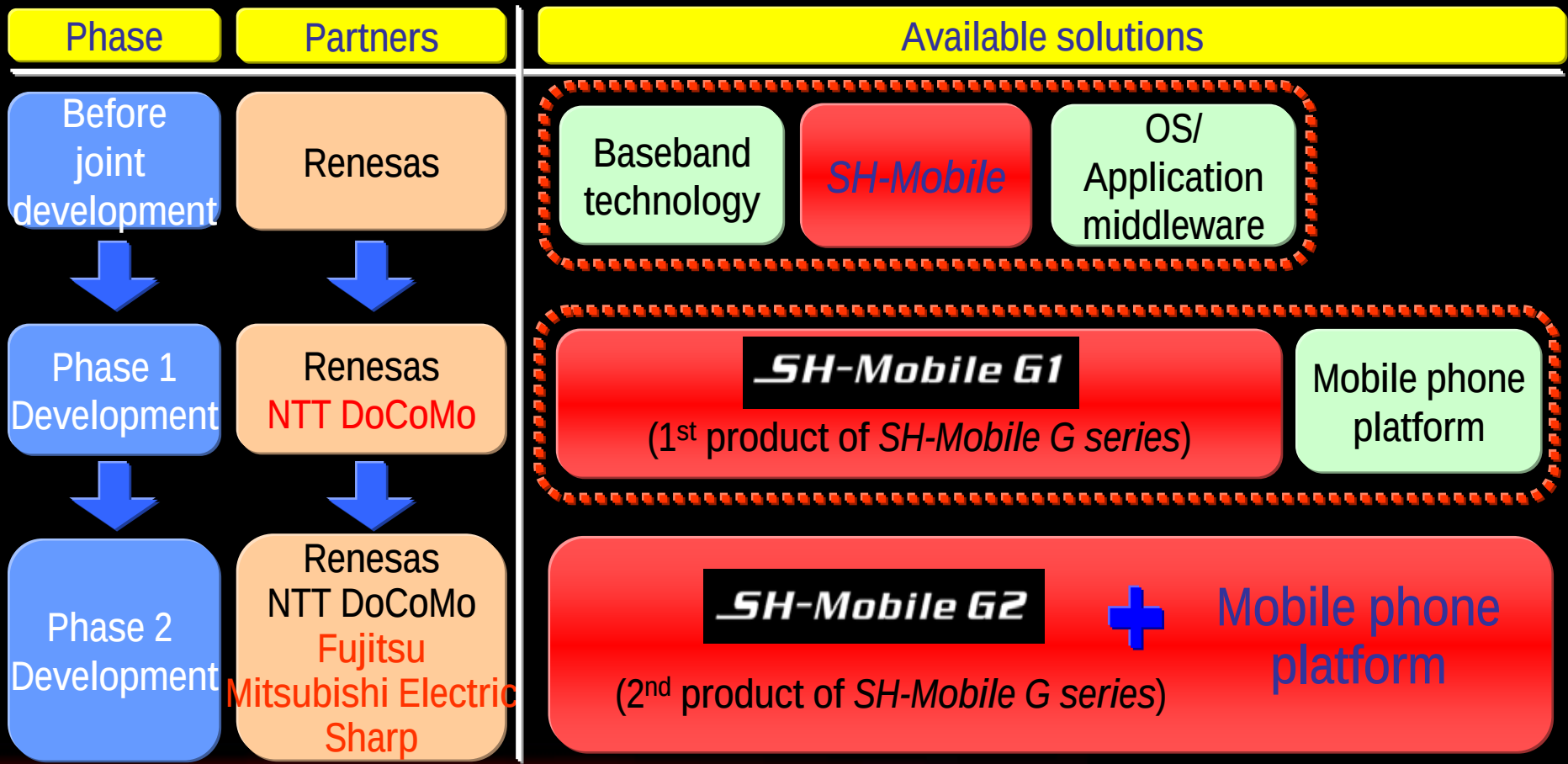
- *SH-Mobile G series*: Reduced the time/cost of development, collaborating with NTT DoCoMo and 3 handset manufacturers
- Fujitsu, Mitsubishi Electric, and Sharp will use it in FOMA handsets





Expanding available 3G solutions from Renesas

- Expanding Renesas 3G solutions from providing a single-chip LSI to a mobile phone platform, realized by phase 2 development with handset manufacturers



What was proven by the SH-Mobile G series

- Best Practices are integrated in the SH-Mobile G series

Leading Edge Process

- 90nm/65nm production capability utilizing 300mm wafer fab
- Process developed cooperating with Panasonic

EXREAL Platfrom™

- Tight relationship with EDA vendors
- Sophisticated functions such as Multi-core integration, with 1st silicon success
- TTM shorten from 18 to 12 months

Partnership Value Chain

- Jointly developed not only with handset makers but also with NTT Docomo
- SH-Mobile consortiums (220 partners)

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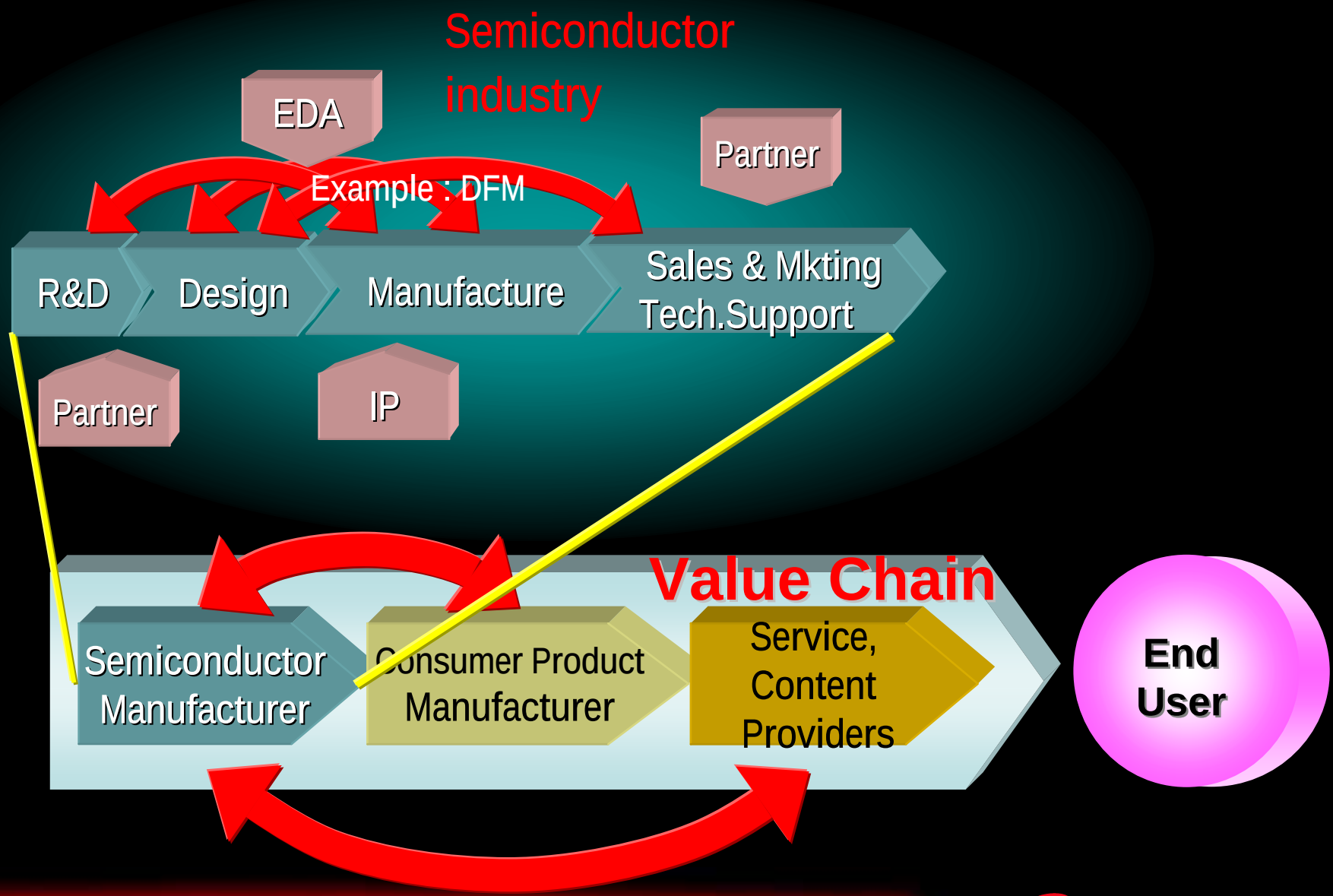
Renesas IDM model: Beyond conventional



Conclusion

- **Maintaining Moore's Law (Performance, Cost)**
  - Not an easy challenge, but need to do it
- **Tight Collaboration among Silicon Society Residents**
  - Wafer process technology developers, Chip designers, EDA vendors, Equipment vendors, …
- **Value Chain**
  - To collaborate Beyond the Silicon Society
- **What's Next**
  - Demand Creation
  - New Chip Design Architecture

References

(1) RENESAS: http://www.renesas.com

(2) SIA: http://www.sia-online.org/pre_statistics.cfm

(3) WSTS: http://www.wsts.org/

(4) Cheap Revolution by Rich Karlgaard (Editor of Forbes): http://www.forbes.com/

(5) TSMC: http://www.tsmc.com/english/default.htm

(6) UMC: http://www.umc.com/

(7) EXREAL: http://resources.renesas.com/lib/eng/edge/12/index.html/

(8) Re-configuration: "A 40 GOPS 250 mw Massively Parallel Processor Based on Matrix Architecture," in Proceeding ISSCC 2006 Session 22.5, pp.410-412

(9) SH-Mobile G1; "Hierarchical Power Distribution with 20 Power Domains in 90 nm Low-Power Multi-CPU Processor," in Proceedings ISSCC 2006 Session 29.4 and "A Power Management Scheme Controlling 20 Power Domains for a Single-Chip Mobile Processor," in Proceeding ISSCC 2006 Session 29.5 .

Cautionary Statement

Certain "forward-looking statements" are based upon current assumptions of future events which may not prove to be accurate. Undue reliance should not be placed on "forward-looking statements," as such statements speak only as of the date of this document.