Optical NoC Evaluation in a System-Level MP-SoC Platform

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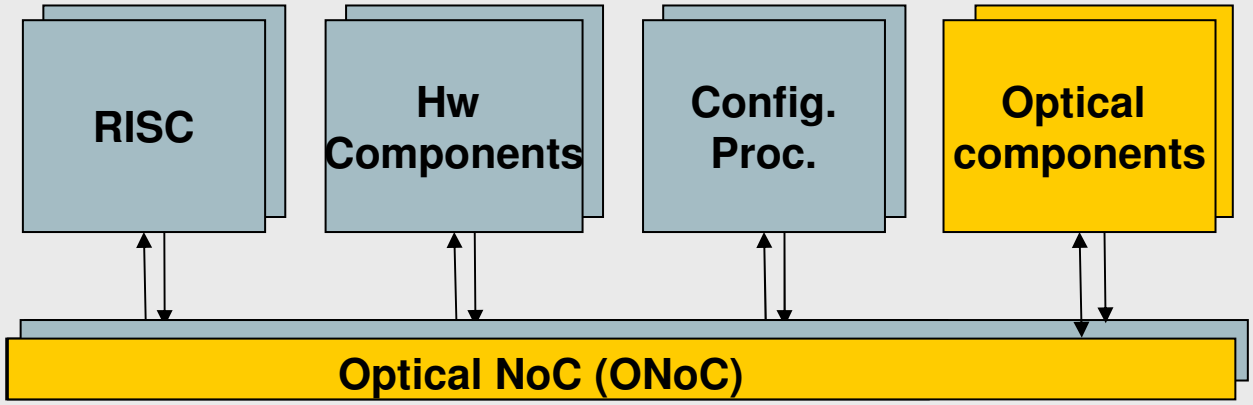
Heterogeneous SoC



- MPSoC architectures with large scale parallelism
- Optical NoC integration to overcome interconnect challenges

Optical NoC: Current R&D

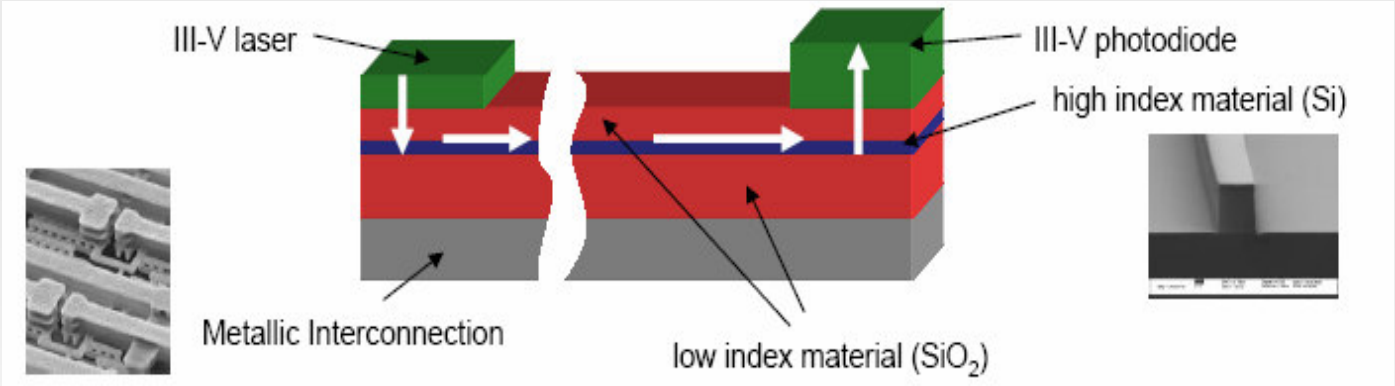
- Research is technology-dominated
  - Physical level research
  - New devices and architectures are defined
- System-level vision not considered yet
- Cooperation between system-level and physical-level designers is required

Overview

- Optical NoC – General view
- Optical NoC evaluation in System-Level platform
- Results
  - MPEG-4 application
    - Optical NoC vs. STBus: 2X speedup
    - Optical NoC vs. XBar: 3.5X speedup
  - Cavity detection application
    - Reducing programming effort

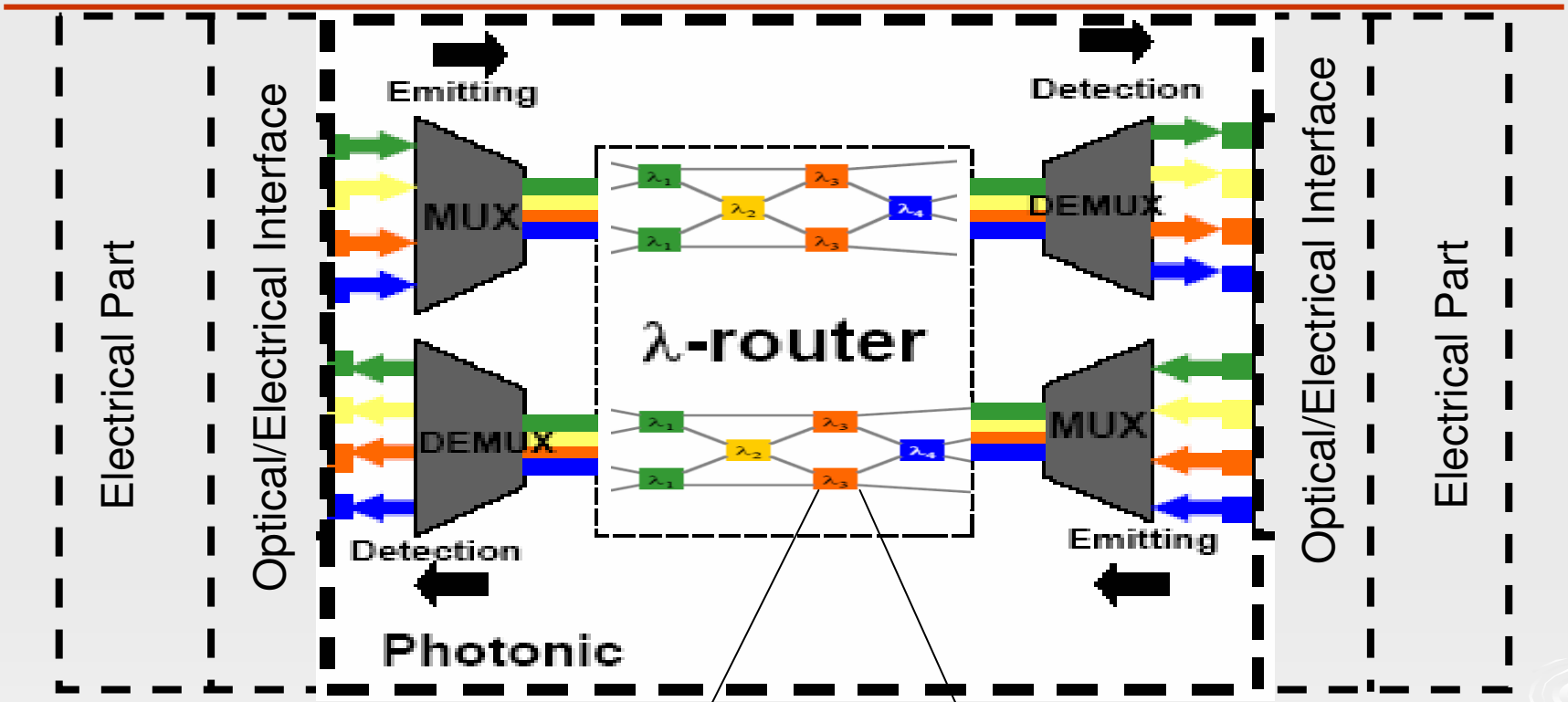
Technological solution

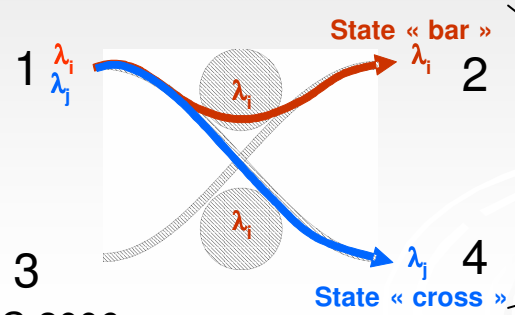
- Optical devices (passives and actives) above the classical integrated circuits
- Compatible with CMOS technology

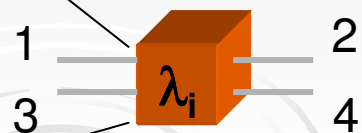


Source: I. O'Connor, Ecole Centrale Lyon

Optical NoC Architecture



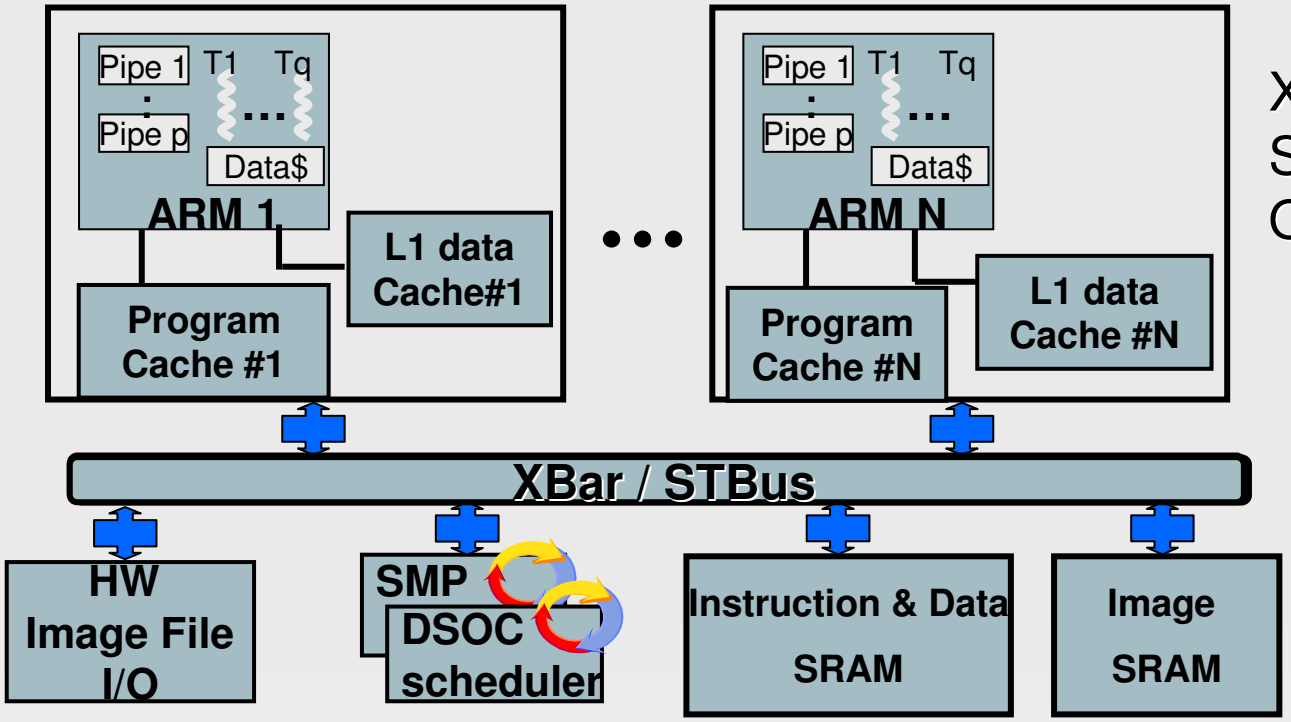




Optical NoC Architecture

- Multiple signals of different wavelengths in the same waveguide
  - No contention, high bandwidth density → 20 GB/s
  - Simple, scaleable interconnect → simpler prog. models
- Constant latency (<1 ns), function of:
  - Optical index of materials (Si, SiO_2)
  - Light propagation delay
  - Waveguide length
- Frequency limited by optical/electrical interfaces
  - Currently 100 MHz

ONoC Evaluation in a System-Level Platform

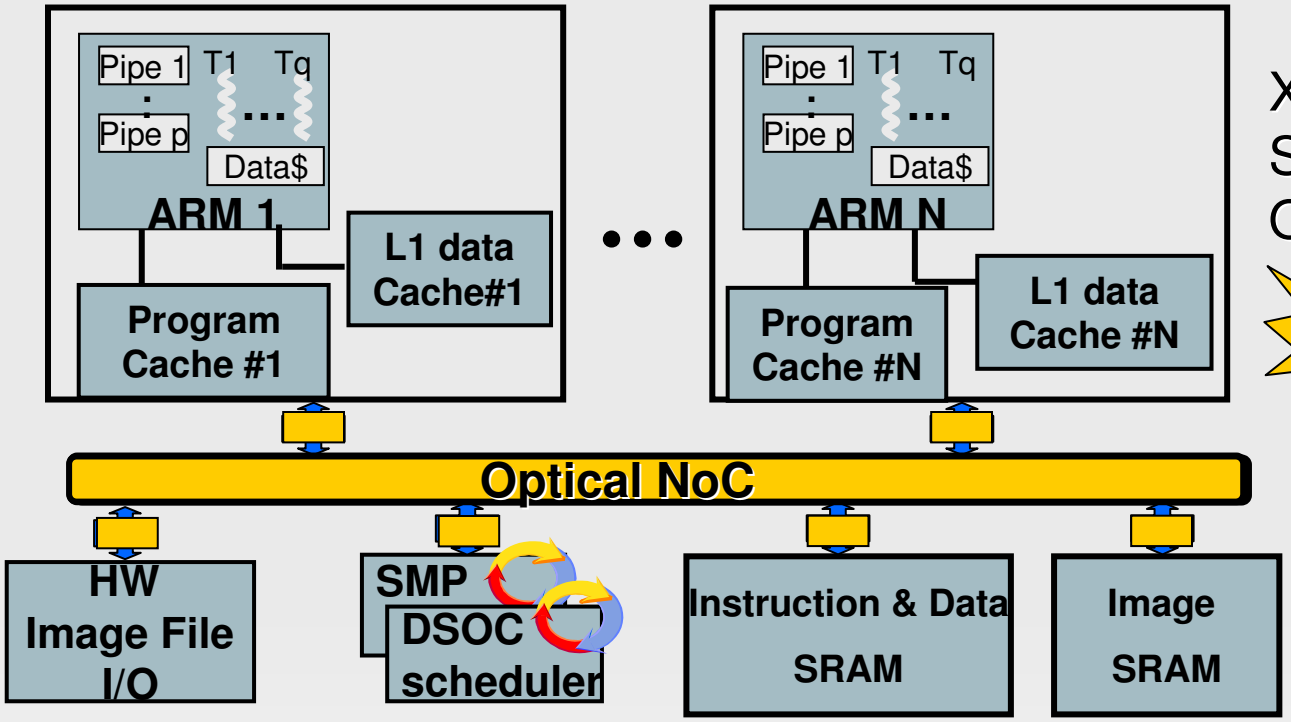


XBar @ 200 MHz
STBus @ 200 MHz
ONoC @ 100 MHz

StepNP Platform
MultiFlex Mapping

- Applications
  - MPEG4
    - Intensive inter-processor communication (40%)
  - Cavity detection application
    - Memory consuming application

ONoC Evaluation in a System-Level Platform

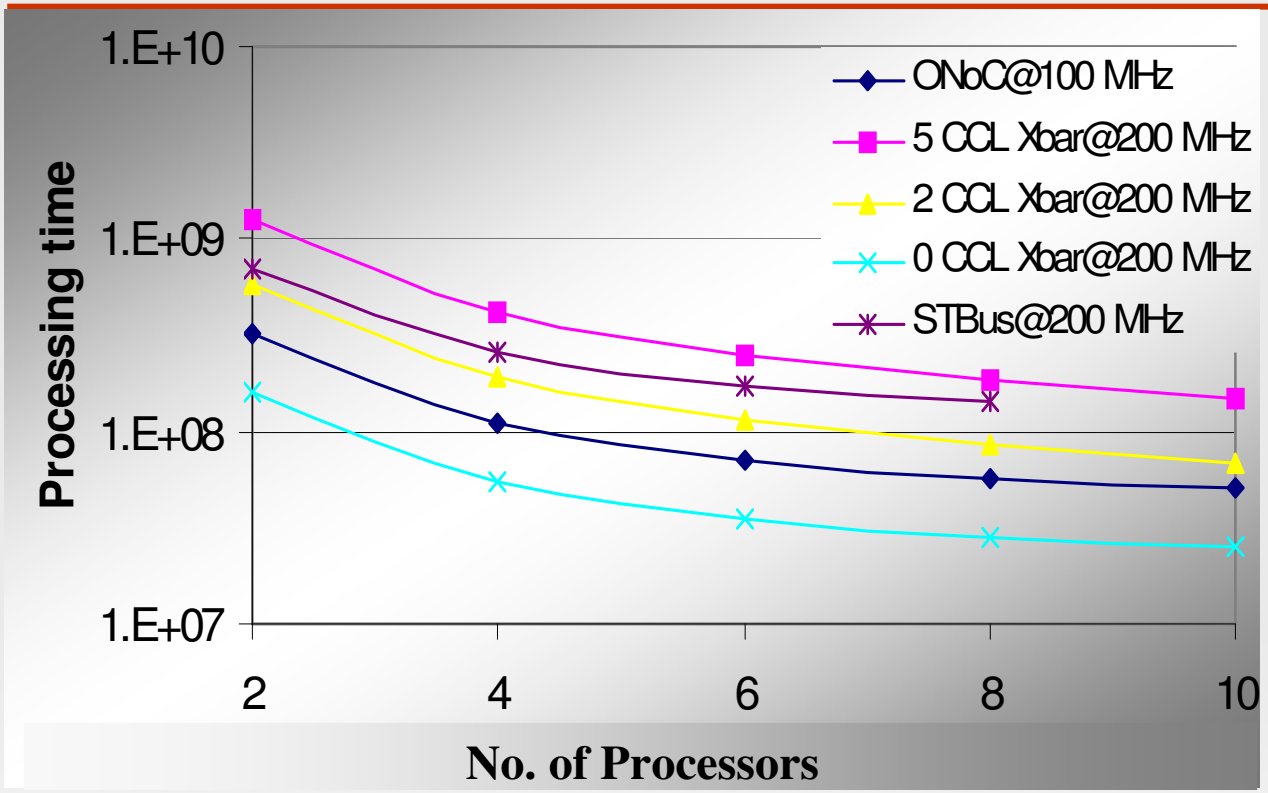


XBar @ 200 MHz
STBus @ 200 MHz
ONoC @ 100 MHz

System-level model for ONoC and optical/electrical interfaces

- Applications
  - MPEG4
    - Intensive inter-processor communication (40%)
  - Cavity detection application
    - Memory consuming application

Results for MPEG4 Application



Results based on high-level STBus model.

More recent implementations of STBus may exhibit higher performances.

- ONoC vs. STBus 2X speedup
- ONoC vs. XBar (5 cycle latency) 3.5X speedup

Summary

- System-Level Evaluation of MPSoC Integrating Optical NoC
  - First results for global simulation of MPSoC including optical network
- Cooperation between Physical Designers and System-Level Designers
  - Physical Design Team
    - Ecole Centrale de Lyon (Prof. Ian O`Connor)
  - System-Level Design Team
    - ST Microelectronics (MultiFlex Team) – MPSoC including STBus and XBar Networks
    - Ecole Polytechnique de Montreal – global modeling and simulation for Opto-Electrical MPSoC