# MPSoC 2006

## DaVinci™ technology for digital video applications

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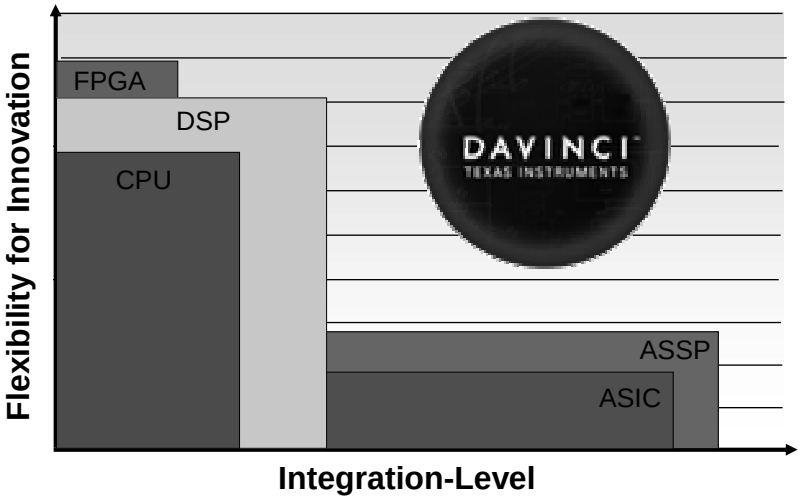
*System Architect*



## Overview

- DaVinci™ technology overview
- **DM644x SoC architecture**
- Software platform overview
- Video performance
- Power management

## Digital media SoC platform






## Complete offering to enable digital video innovation

**Processors: Digital video system-on-chips**

- **TMS320DM6443 – Video decode**
- **TMS320DM6446 – Video encode/decode**


**Software: Open, optimized and production tested**

- **Platform-optimized, multimedia codecs**
- **Platform support package**
- **Linux support package**
- **Industry-recognized APIs**
- **Multimedia frameworks**

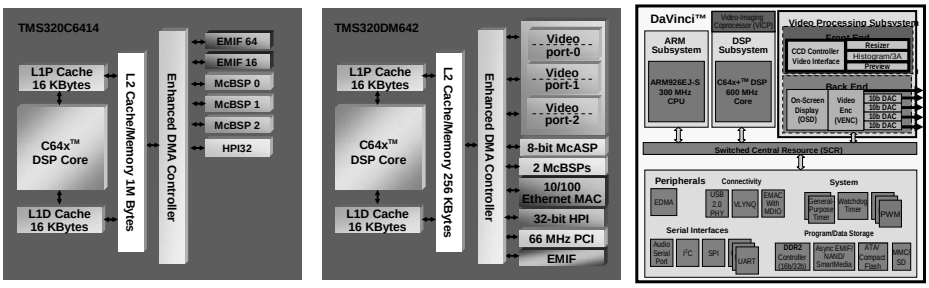
**Tools: Validated software and hardware development**

DVEVM
Digital Video Evaluation Module

montavista

# Video chip evolution

**Video-capable DSP** | **Digital Media Processor** | **Digital Media SOC**





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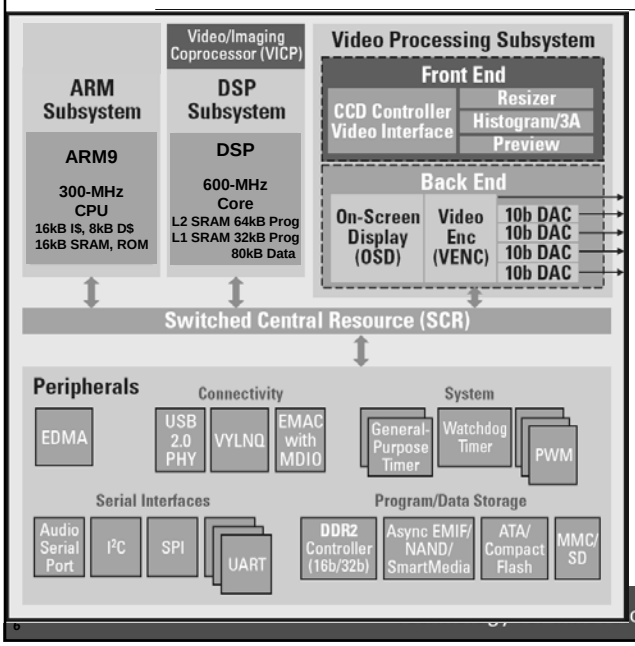
# TMS320DM644x block diagram




Quality Multi-Format Video Encode/Decode Support
- **600 MHz C64x+ DSP**
- **Video Accelerators**
- **High Bandwidth DDR2 Memory Interface**
- **Integrated Video Output**

System Integration & Flexibility
- **300 MHz ARM Host Processor**
- **Programmable for Changing Standards**

System Connectivity
- **Ethernet MAC for Streaming Video**
- **USB 2.0 for Consumer Peripherals**

Video Storage
- **ATA HDD interface**
- **True IDE Compact Flash Interface**

Dedicated Video Processing Sub-system
- **Front end – Resizer, Image processing engine, 16-bit digital input**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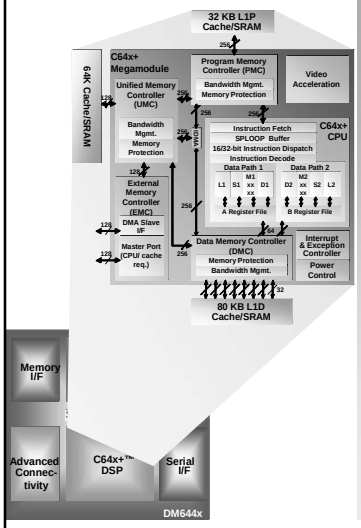
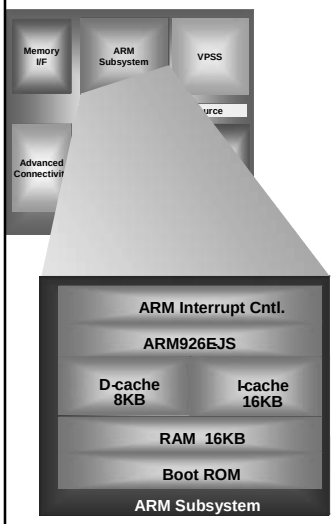
# Video Optimized C64x+™ DSP




| DM644x™ Feature | Benefit |
|---|---|
| ▸ **Video Optimized DSP**<br>▪ Video Acceleration<br>▪ 32kB L1P Cache/ SRAM<br>▪ 80kB L1D SRAM<br>• Up to 32kB Cache<br>▪ 64kB L2 Cache/SRAM<br>▪ 600 MHz | **Video**<br>▸ H.264 MP D1 Decoding<br>▸ VC-1/WMV9 D1 Decoding<br>▸ MPEG-2 MP@ML D1 Decoding<br>▸ MPEG-4 ASP D1 Decoding<br>▸ H.264 BP D1 Encoding<br>▸ Simultaneous H.264 BP CIF Enc/Dec<br>**Audio (Concurrent with Video)**<br>▸ MPEG-4 AAC LC and HE<br>▸ MP3<br>▸ MPEG-1 Layer 1&2<br>**Security**<br>▸ 128-Bit AES Decryption<br>▸ Microsoft DRM Support |
| ▸ **Programmability** | ▸ **Multi-Format Video Capability**<br>▸ **Future Proof – Easily Upgradeable** |
| ▸ **C64x+ CPU**<br>▪ SPLOOP Buffer<br>▪ 16-Bit Instruction Coding | ▸ **100% Code Compatible from C64x™**<br>▸ **Greater than 20% Code Size Reduction** |

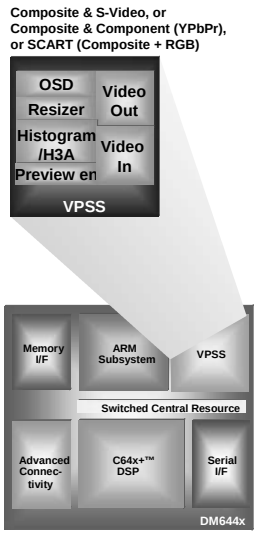


# ARM host




| DM644x™ Feature | Benefit |
|---|---|
| ▸ **ARM9 Host Processor**<br>▪ 300 MHz | ▸ **Standard OS Environment**<br>▸ **Flexible Network Protocol Options**<br>▸ **Simplifies User Interface**<br>▸ **System Control Flexibility** |
| ▸ **Memory**<br>▪ 8kB Data Cache<br>▪ 16kB Instruction Cache<br>▪ 16kB RAM | ▸ **Efficient Application Execution** |

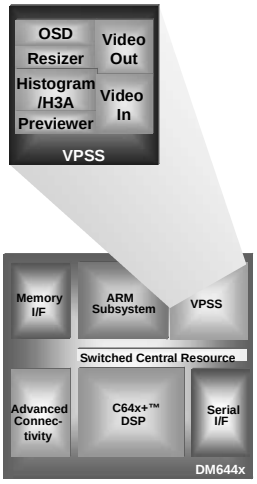
# Video processing sub system




| DM644x Feature | Benefit |
|---|---|
| ▸ **Integrated Video Output**<br>▪ RGB888 @ 75 MHz<br>▪ BTU656 : 8 or 16 bit @ 75 MHz<br>▪ Support for Standard LCD I/F | ▸ **Optimized Video System Cost**<br>▸ **Standard Encoder Connectivity** |
| ▸ **4 10-bit 54MHz DACs**<br>▪ Composite<br>▪ S-Video<br>▪ Component: RGB, YPbPr<br>▪ NTSC/PAL: 480/576 Interlaced<br>▪ NTSC/PAL: 480/576 Progressive | ▸ **Integrated Display Driver**<br>▸ **Multi-Format Support**<br>▸ **Optimized Video System Cost** |
| ▸ **Integrated Video Input**<br>▪ CCD/CMOS Interface<br>• 16 bit at 75 MHz<br>▪ BTU601/656 Interface<br>• 8 or 16 bit at 75 MHz<br>▪ Color Space Conversion | ▸ **Analog Codec Connectivity**<br>▸ **Digital Video Interface**<br>▸ **Glueless Camera Interface**<br>▸ **Video Format Flexibility** |
| ▸ **Preview en**<br>▪ Bayer RGB to YCbCr 4:2:2 color space conversion | ▸ **Off loads the DSP**<br>▸ **Programmable noise filter** |

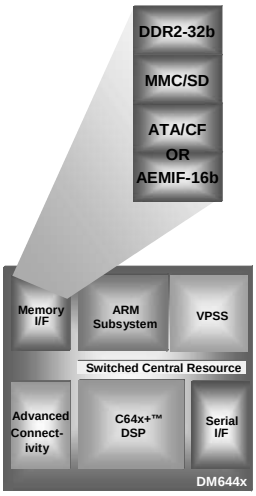


# Video processing sub system (continued)




| DM644x Feature | Benefit |
|---|---|
| ▸ **On Screen Display (OSD)**<br>▪ Video Window<br>• RGB888<br>• YCbCr 4:2:2<br>▪ One OSD Bitmap Window<br>• RGB656<br>• One Attribute Window<br>• 8 levels of blending | ▸ **Picture in Picture Capability**<br>▸ **Easy to Use Attribute Window**<br>▸ **On Screen Application Control** |
| ▸ **Resizer**<br>▪ 4x to 1/4x Resizing<br>• N/256 Zoom step<br>▪ Linear and Bi-Cubic Resize Algorithm | ▸ **Automatic Video Rescale**<br>▸ **Offload CPU Processing** |
| ▸ **Histogram/H3A**<br>▪ Statistical Engine for Calculating Exposure, White Balance, and Focus<br>▪ Histogram data collection<br>▪ Statistics collected in RGB Color Space<br>▪ ARM and/or DSP can use these statistics to control camera functions | ▸ **Automatic Focus Control**<br>▸ **Automatic White Balance Correction**<br>▸ **Automatic Exposure Compensation** |

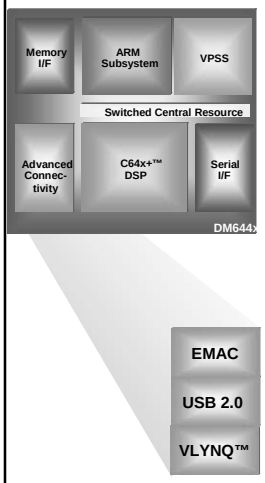
# Memory and storage interfaces




| DM644x™ Feature | Benefit |
|---|---|
| ▸ **DDR2-333**<br>▪ 32-Bit Interface<br>▪ Up to 256MB<br>▪ 166 MHz Clock | ▸ **Quality Video Processing**<br>▸ **Advanced Codec Capability** |
| ▸ **Hard Disk Interface**<br>▪ ATA/ATAPI-5 HDD Interface<br>▪ True IDE Compact Flash<br>▪ Shared with EMIF | ▸ **Local Video Storage** |
| ▸ **EMIF**<br>▪ 4 Chip Selects<br>▪ NAND Flash Connection<br>• 2 x 8/16-bit NAND Devices<br>• SM/xD<br>▪ Asynchronous Memory<br>▪ Shared with ATA | ▸ **Easy Boot Configuration**<br>▸ **Expansion Capability** |
| ▸ **MMC/SD** | ▸ **MultiMedia Card Interface** |

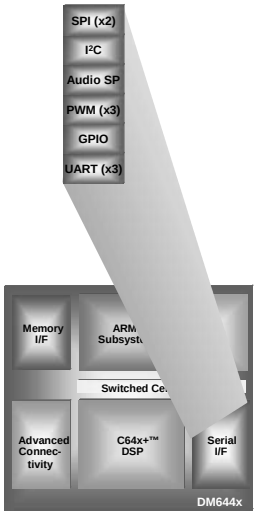



# Advanced connectivity




| DM644x™ Feature | Benefit |
|---|---|
| ▸ **Ethernet MAC**<br>▪ 10/100 Mb/s<br>▪ MII to Switch or PHY<br>▪ MDIO Interface | ▸ **Real-Time Streaming Video**<br>▸ **Integration Optimizes Cost** |
| ▸ **USB 2.0**<br>▪ LNK + PHY<br>▪ High Speed (480Mps)<br>▪ Host or client | ▸ **Standard Expansion Interface**<br>▸ **High-speed Video Uploads** |
| ▸ **VLYNQ™**<br>▪ 75 MHz Serial Connection<br>▪ 4 Serial Receive Pins<br>▪ 4 Serial Transmit Pins | ▸ **FPGA Interface**<br>▸ **802.11 WLAN Interface** |

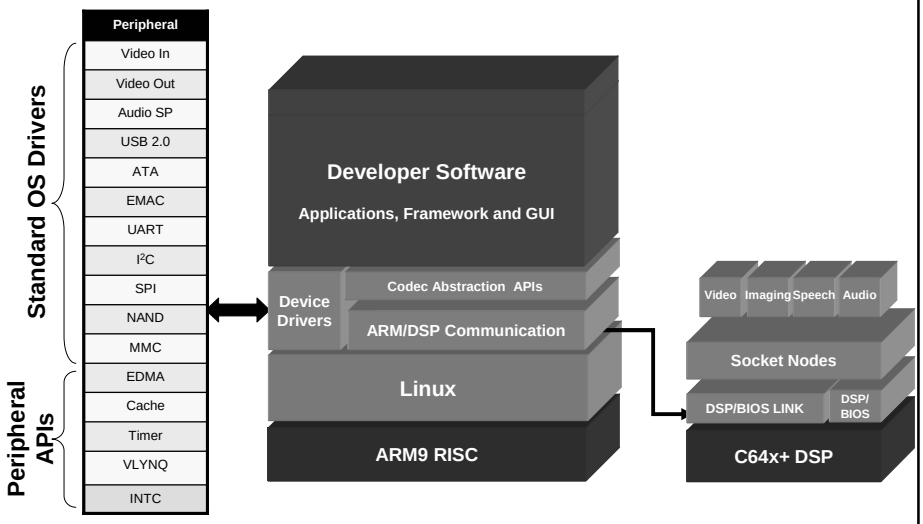
# Serial interfaces




| DM644x Feature | Benefit |
|---|---|
| ▸ **Audio Serial Port**<br>▪ AC97 Support<br>▪ I2S Audio Connection | ▸ **Low Cost Codec Connectivity**<br>▸ **Audio Format Flexibility** |
| ▸ **UART (3)**<br>▪ One with Flow Control | ▸ **Bluetooth Interoperability**<br>▸ **Remote Control Capability** |
| ▸ **I²C** | ▸ **Peripheral Configuration** |
| ▸ **SPI (2)** | ▸ **Peripheral Configuration** |
| ▸ **PWM (3)** | ▸ **PLL Synchronization**<br>▸ **PTZ/Focus Camera Control** |
| ▸ **GPIO** | ▸ **Optional User Peripherals** |



# Software platform overview



# Video performance in an end system

## Benchmarks: DM644x Video Capabilities

| | TMS320DM6446 | TMS320DM6443 |
|---|---|---|
| Standalone Codecs | | |
| MPEG-2 MP ML Decode | 1080i+ (60 fields/30 frames) | 720+ |
| MPEG-2 MP ML Encode | D1+ | n/a |
| MPEG-4 SP Decode | 720p+ | 720p+ |
| MPEG-2 SP Encode | 720p+ | n/a |
| VC1/WMV 9 Decode | 720p+ | 720p+ |
| VC1/WMV 9 Encode | D1+ | n/a |
| H.264 (Baseline) Decode | D1+ | D1+ |
| H.264 (Baseline) Encode | D1+ | n/a |
| H.264 (Main Profile) Decode | D1+ | D1+ |



# Power management

- Intended to be used for battery powered devices and not just wall plugged applications
- **Voltage scaling**
  - From 1.2V to 0.95V core VDD → up to 37% reduction in active power and 50% reduction in leakage
- **Process compensation**
  - Blow fuses for voltage compensation; increase voltage for weak process and decrease voltage for strong process → 100-200 mV reduction in core voltage
- **Multiple Vt transistors**
  - Trade-off area, speed, and power using high Vt, standard Vt, and Long L transistors → up to 50% reduction in leakage power
- **Pre-silicon power simulations**
  - Improve RTL and microarchitecture based on power simulations → 50% reduction in active power in key blocks
- **Multiple power domains**
  - DSP and VICP on separate power domain from rest of the core VDD → 50% reduction in leakage power
- **Mode aware IO**
  - Turn off DDR2 SSTL1.8V IO receivers when not doing reads → 40mW power savings when no reads to DDR2

# Questions