Benchmarking System Applications on

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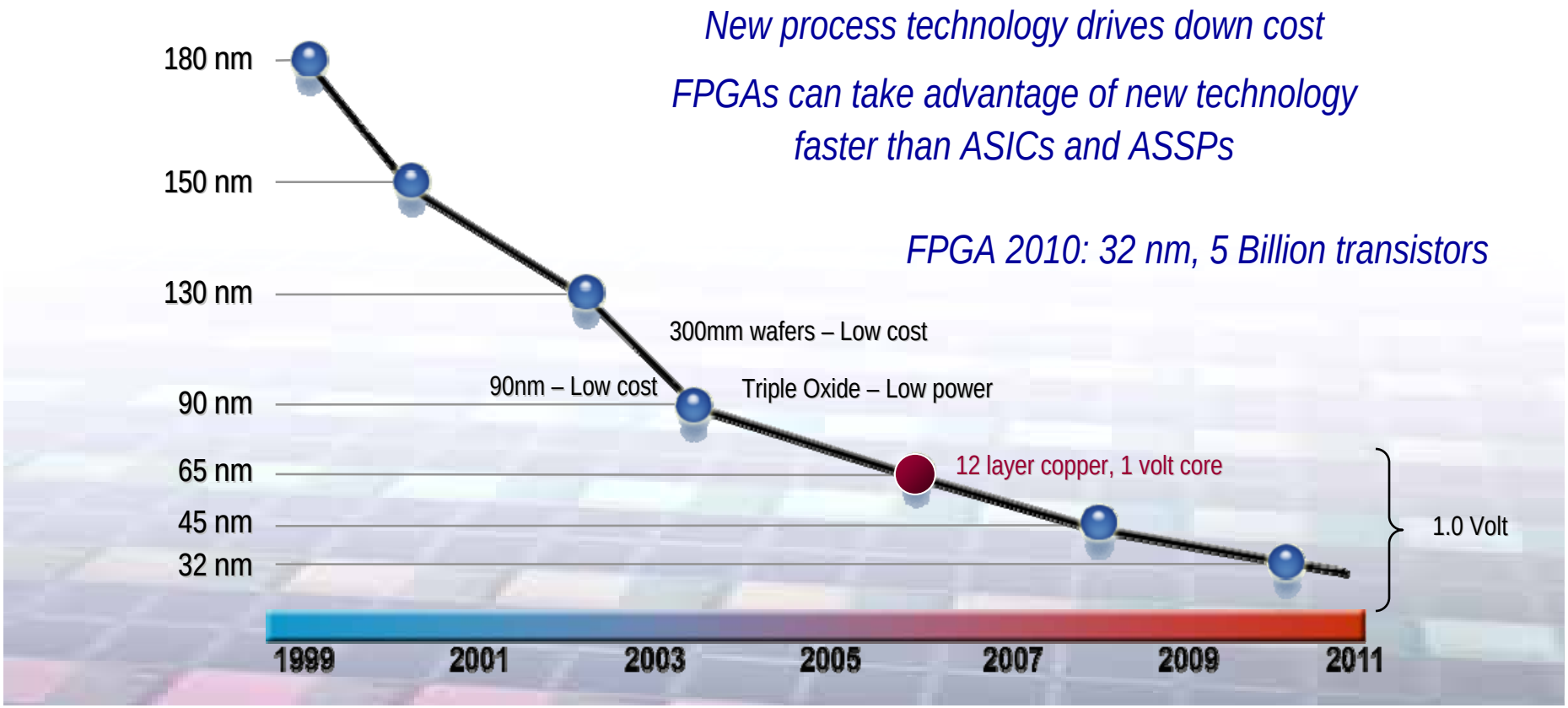
Structure of the talk

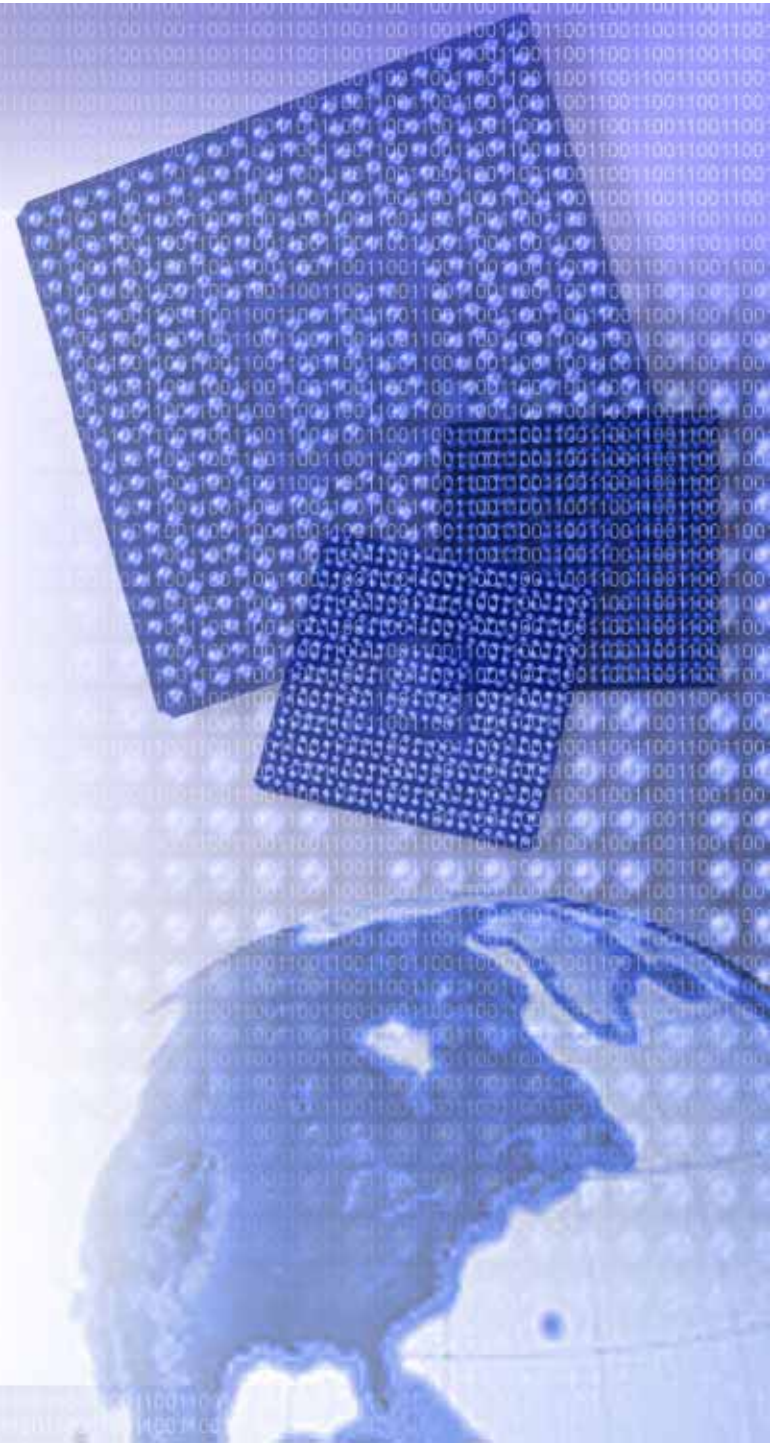
- FPGAs in 65nm technology going towards 32nm
- Virtex 5 family
- Benchmarking Virtex 5 LUT6 fabric
- Benchmarking Memory sizes
- New Microblaze in Virtex 5 fabric
- Conclusion

FPGAs Drive the Process

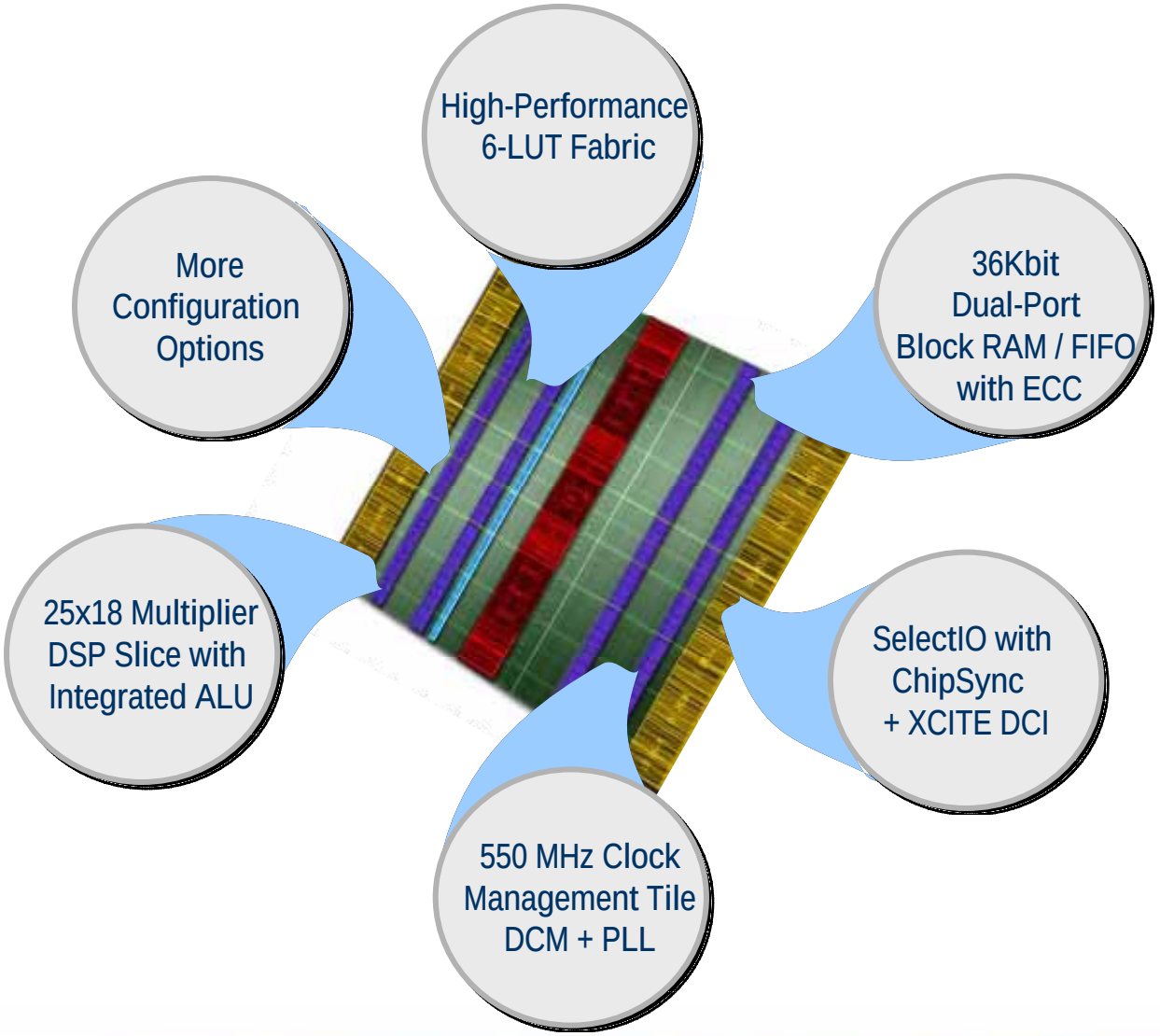


The cost of IC development increases. Therefore customers want to buy reconfigurable and programmable platforms, instead of developing their own.

LX Platform Overview



System components



Virtex-5 Logic Architecture

True 6-input LUTs

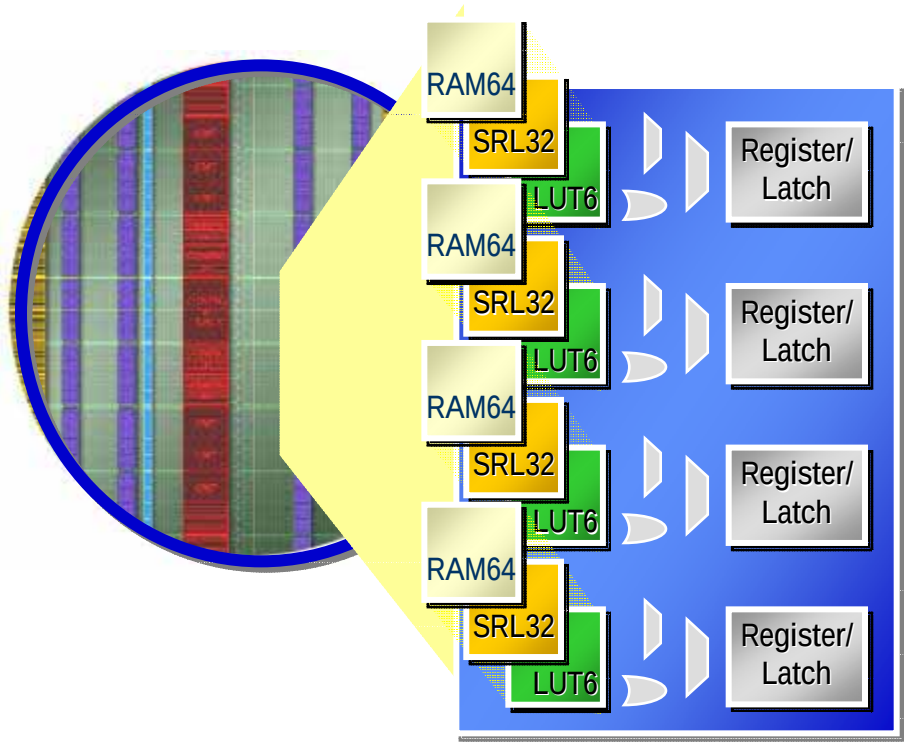
- with dual 5-input LUT option
- 1.4 times the value for actual logic
- only 1.15 times the cost in silicon area.

64-bit RAM per M-LUT

- about half of all LUTs

32-bit or 16-bit x 2

- shift register per M-LUT

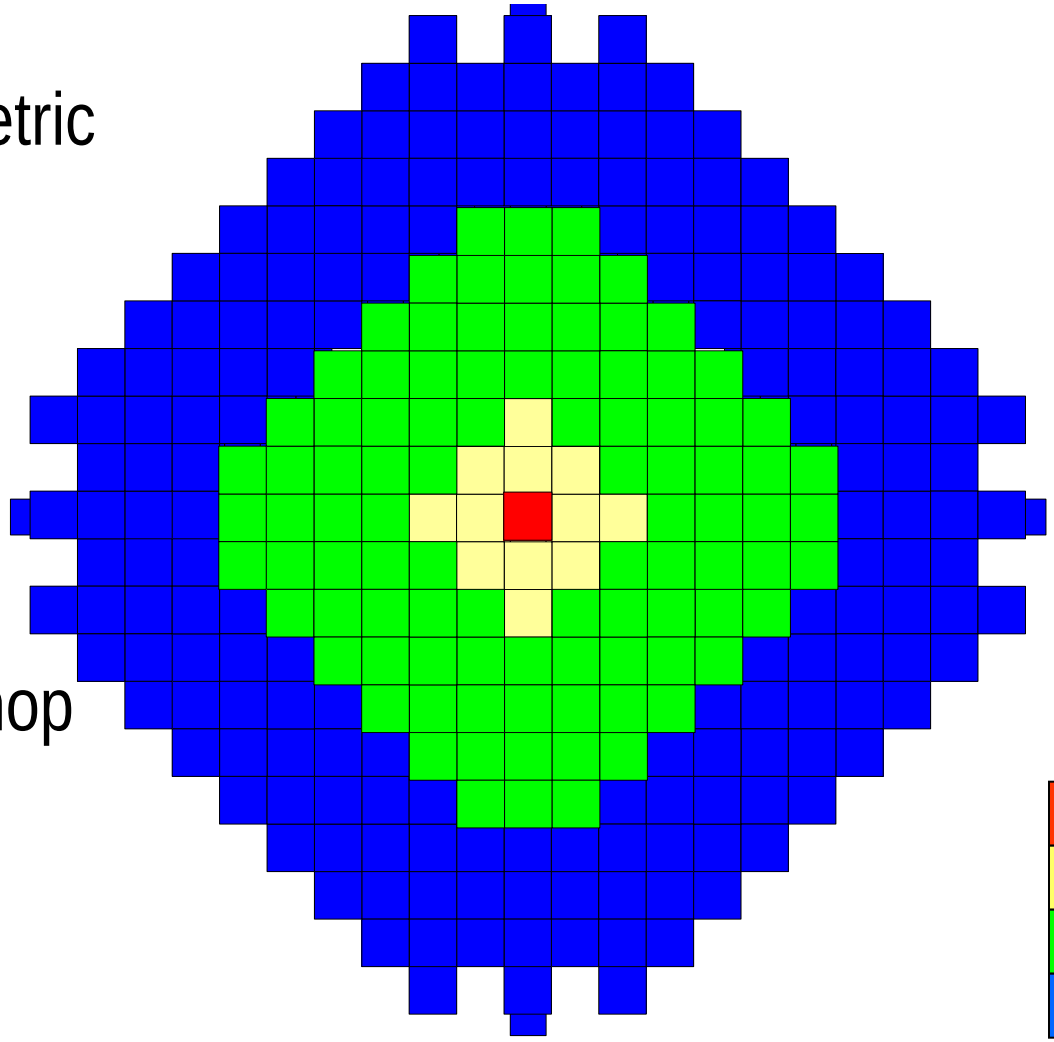


Virtex-5 Routing

More symmetric pattern

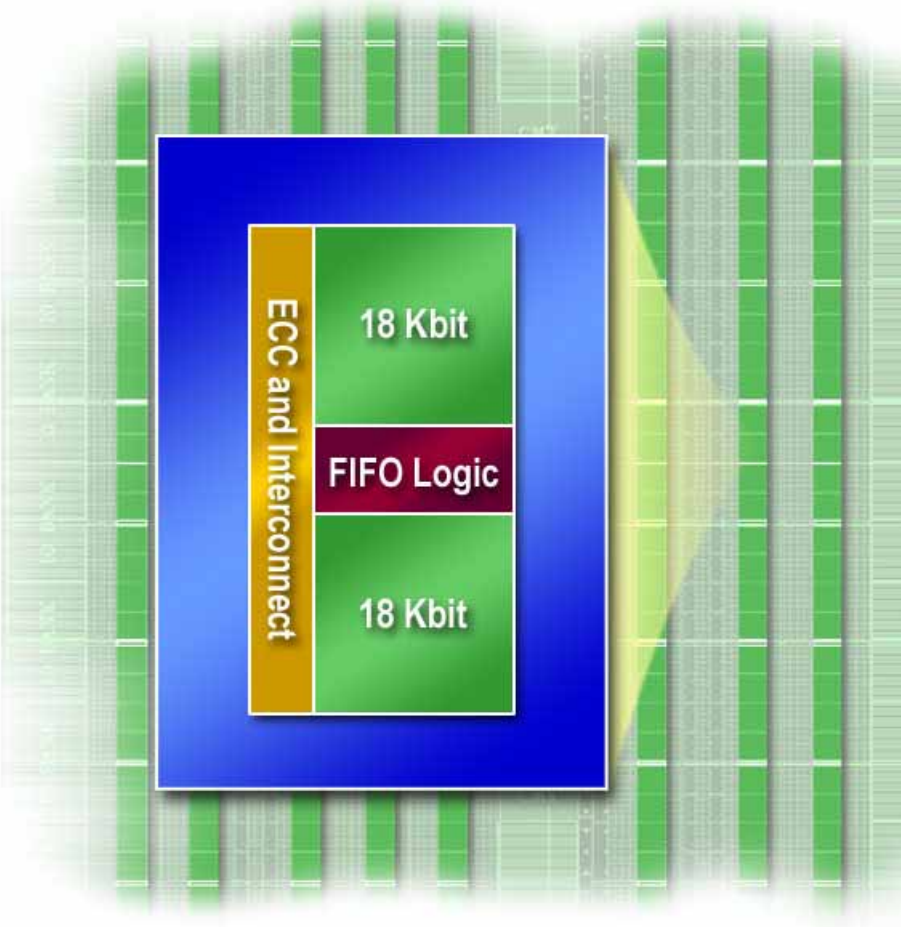
More logic reached per hop

Same pattern for all outputs



BRAM/FIFO

- 36 Kbit BRAM
  - Integrated FIFO Logic for multi-rate designs
  - Built-in ECC
  - Cascadable to build larger RAM arrays
  - Dual Port: a read and write every clock cycle
- Performance up to 550 MHz



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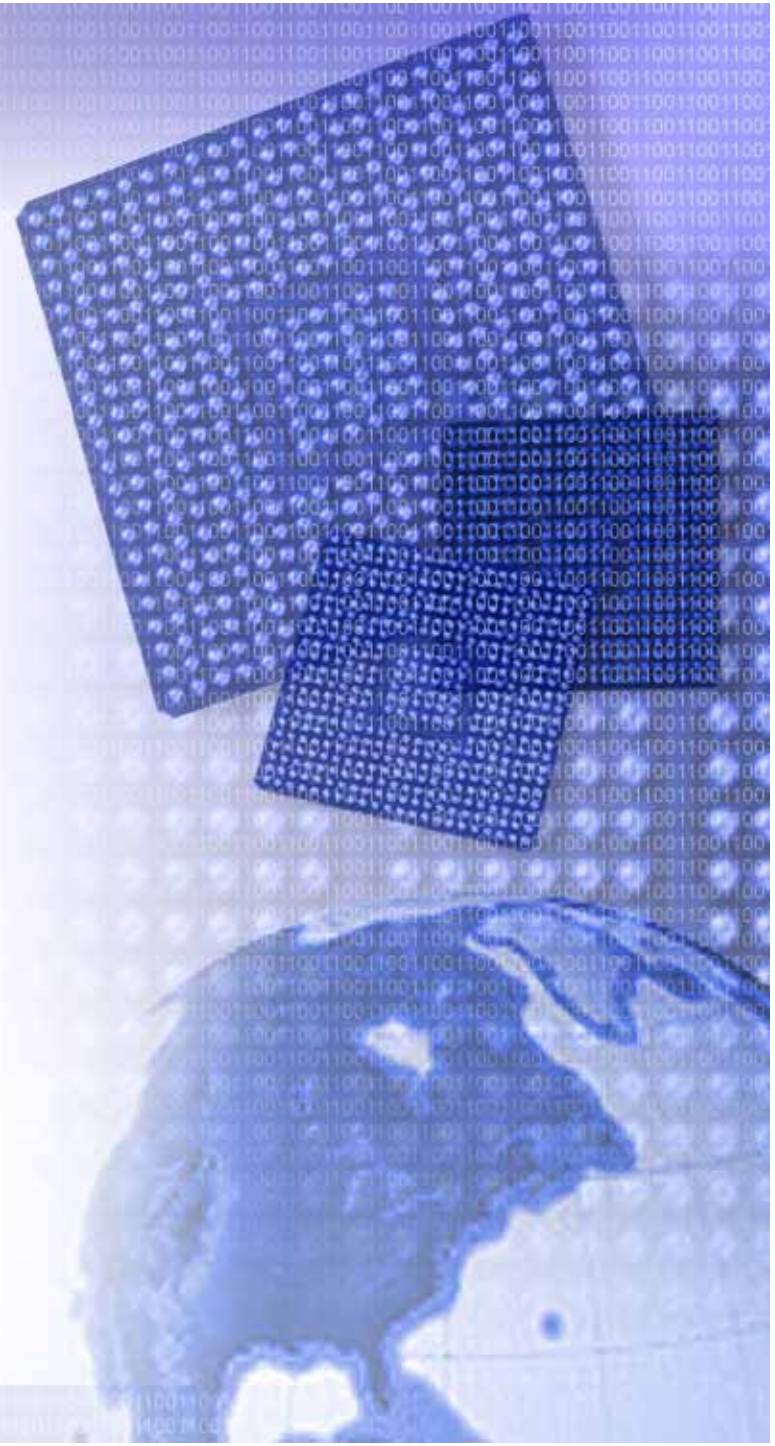
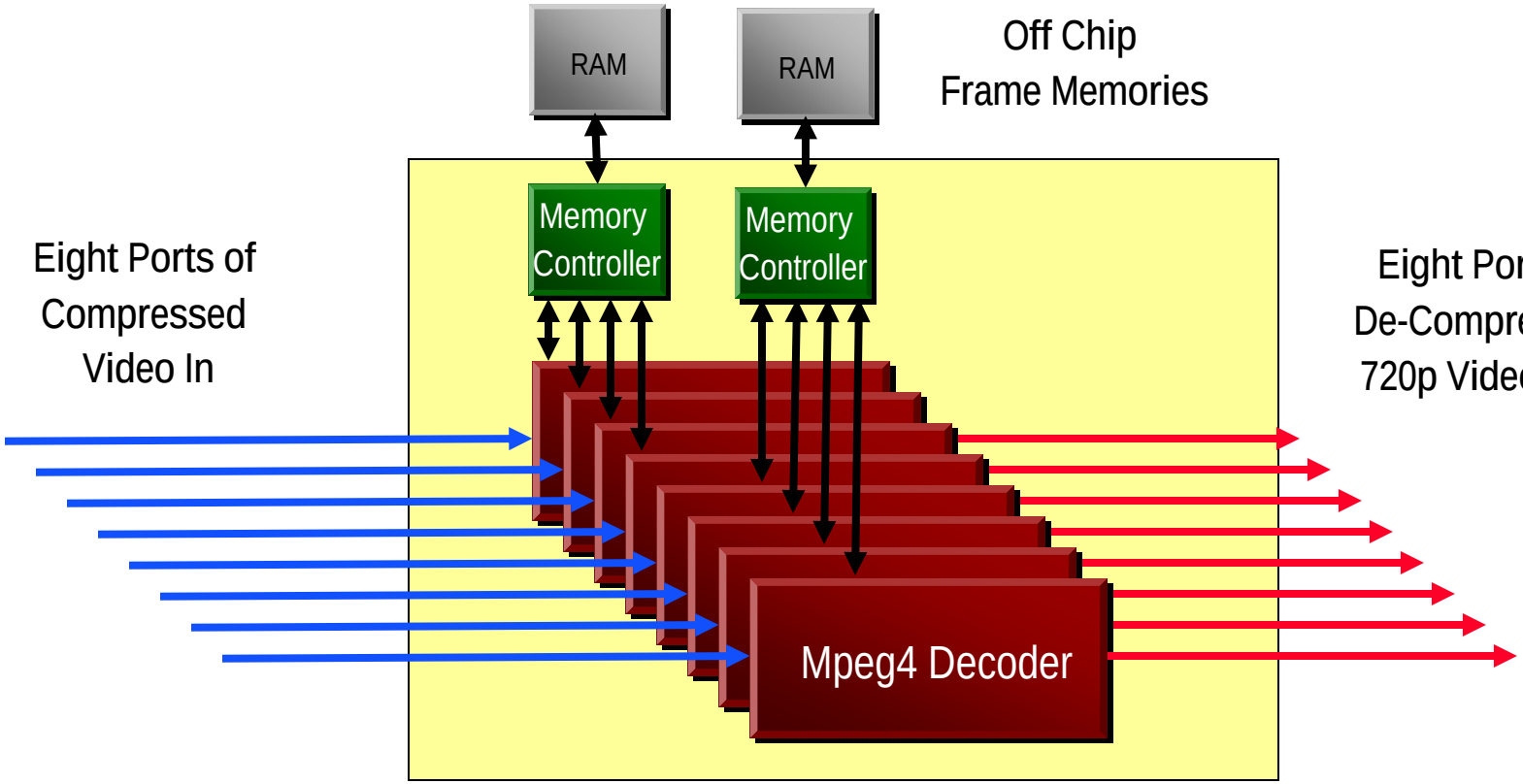
Virtex-5 Applications Benchmarks



8 MPEG4 decoders

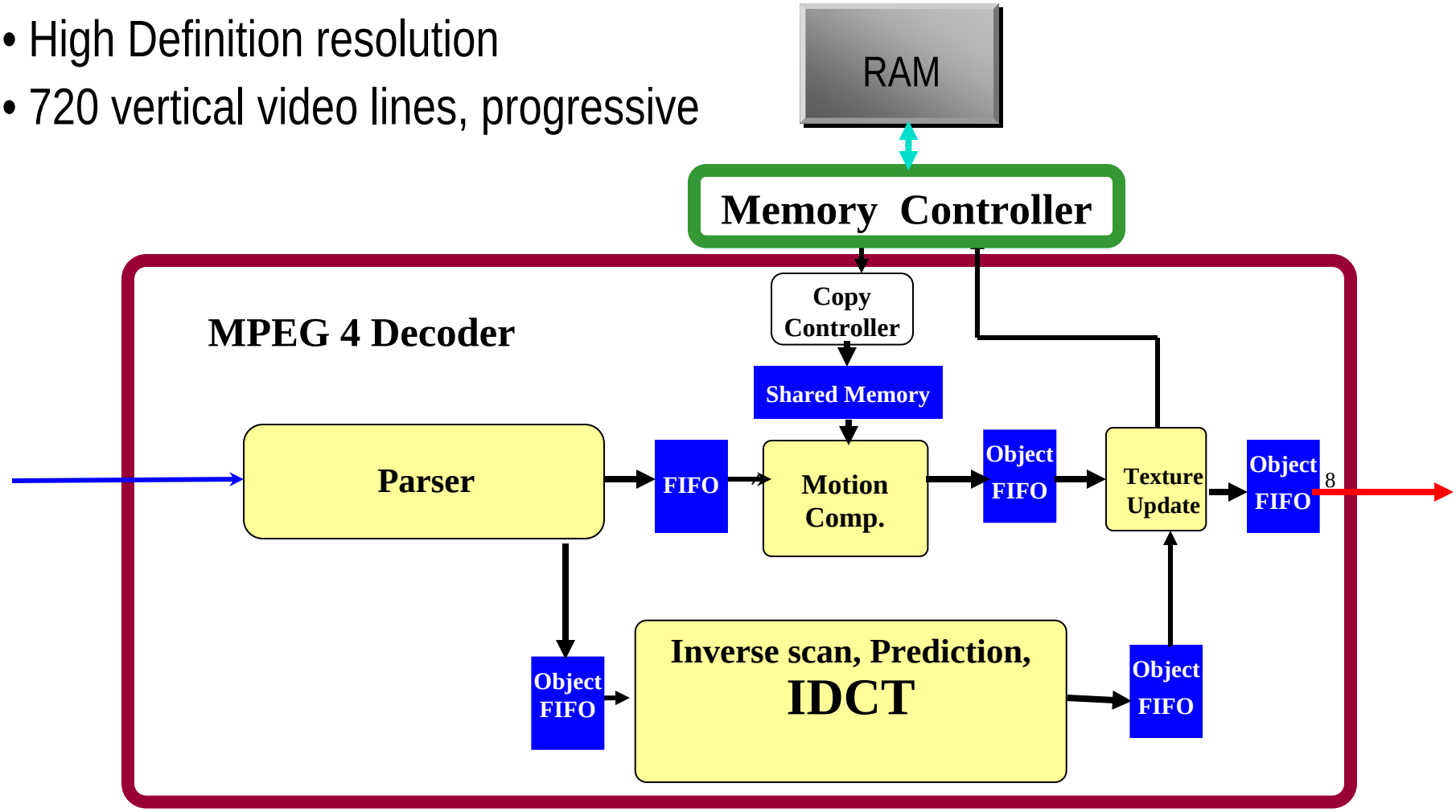


Category	Virtex-4	Virtex-5
Tools	XST/ISE 8.1.02i	XST/ISE 8.2i*
Devices	XC4VFX140-11	Virtex5 part

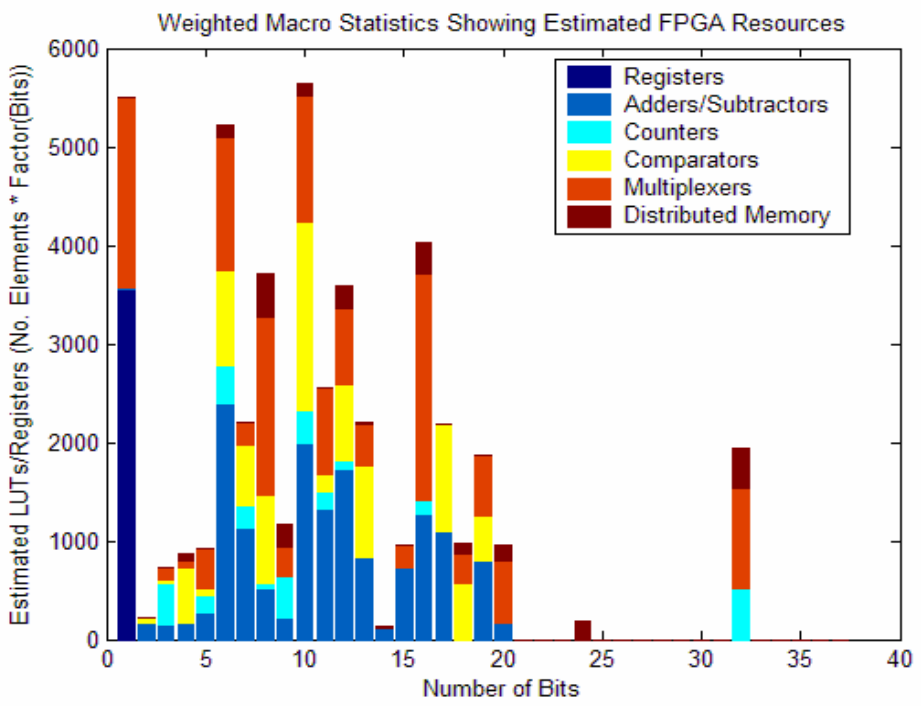
* Used internal version Im.11, early release of 8.2i

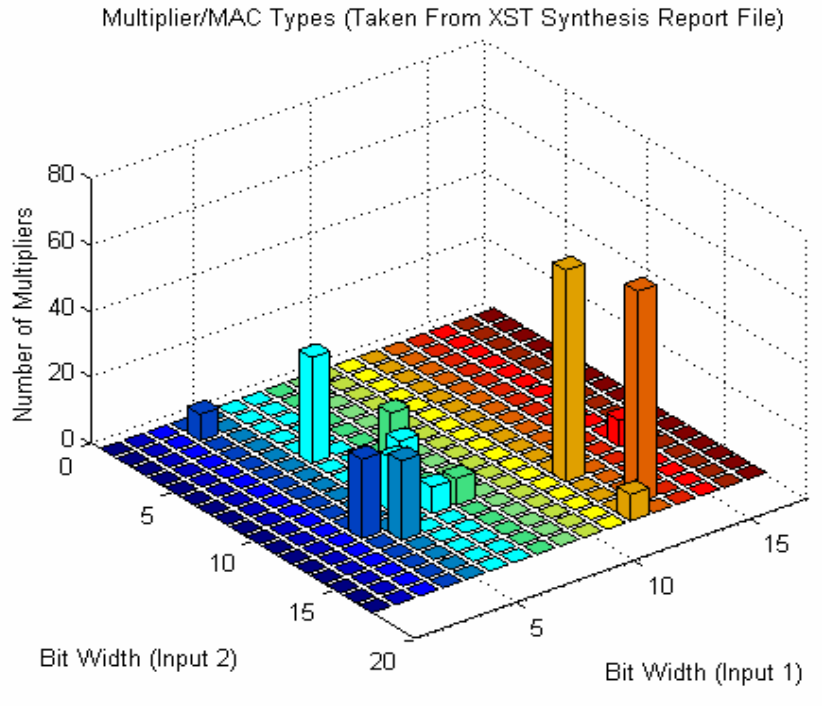
One MPEG4 Video Decoder

- High Definition resolution
- 720 vertical video lines, progressive



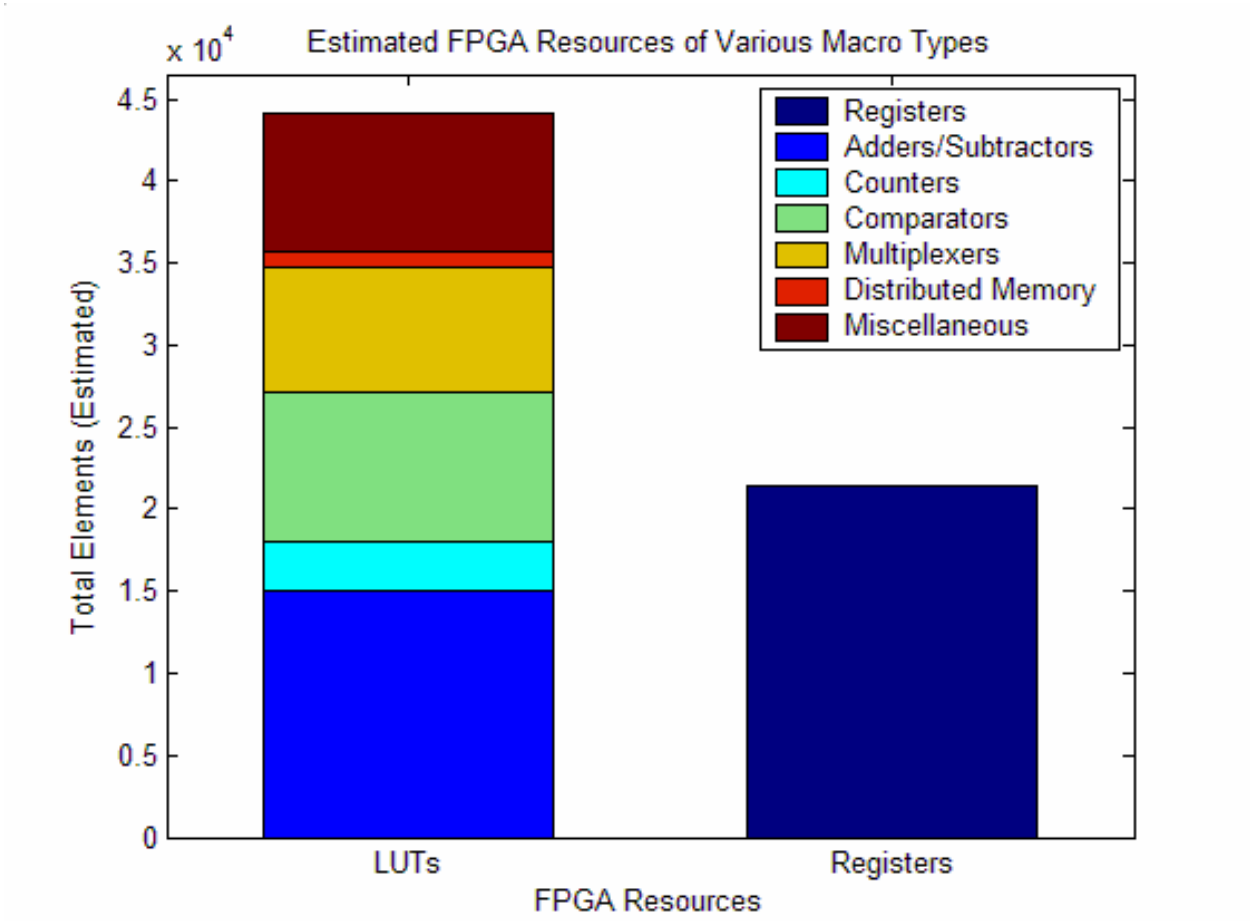
MPEG-4 Decoder: Macro Statistics
(extracted from XST report)



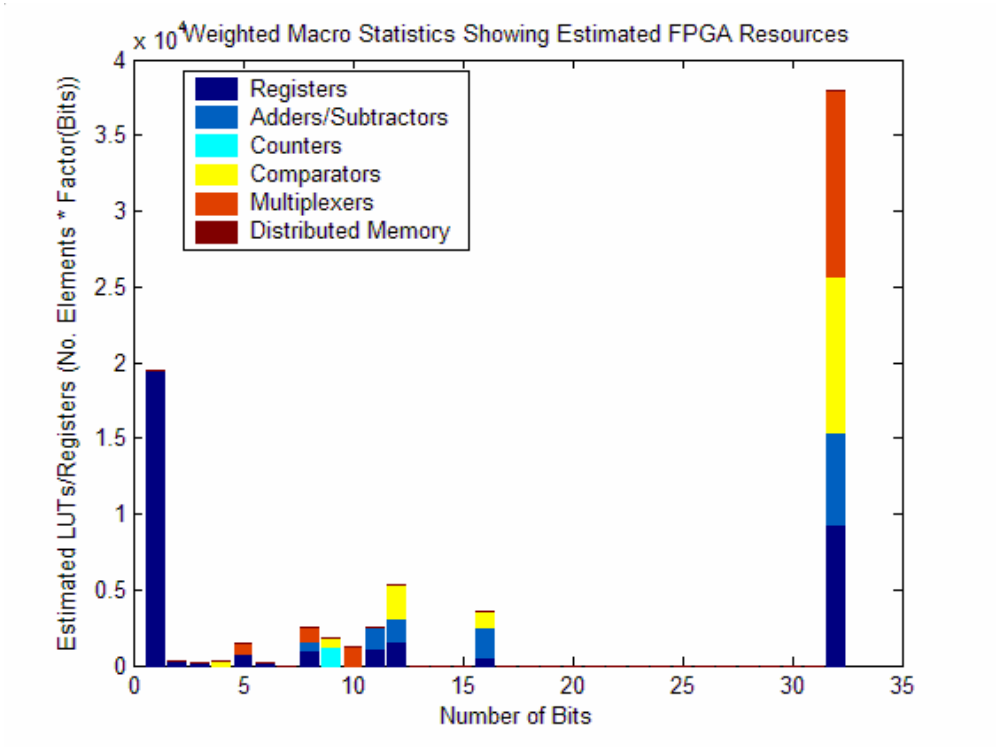


- Large, diverse design with varying data widths and macro types
- Notes: Registers listed as 1-bit elements; 304 multipliers in design

MPEG-4 Decoder: Resources



Comparison: IP Router



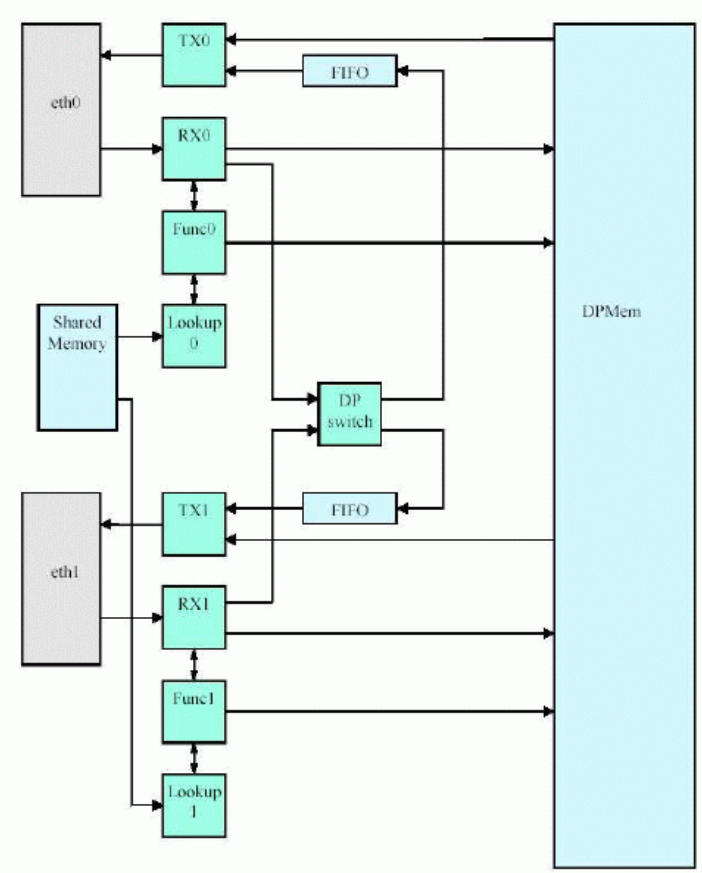
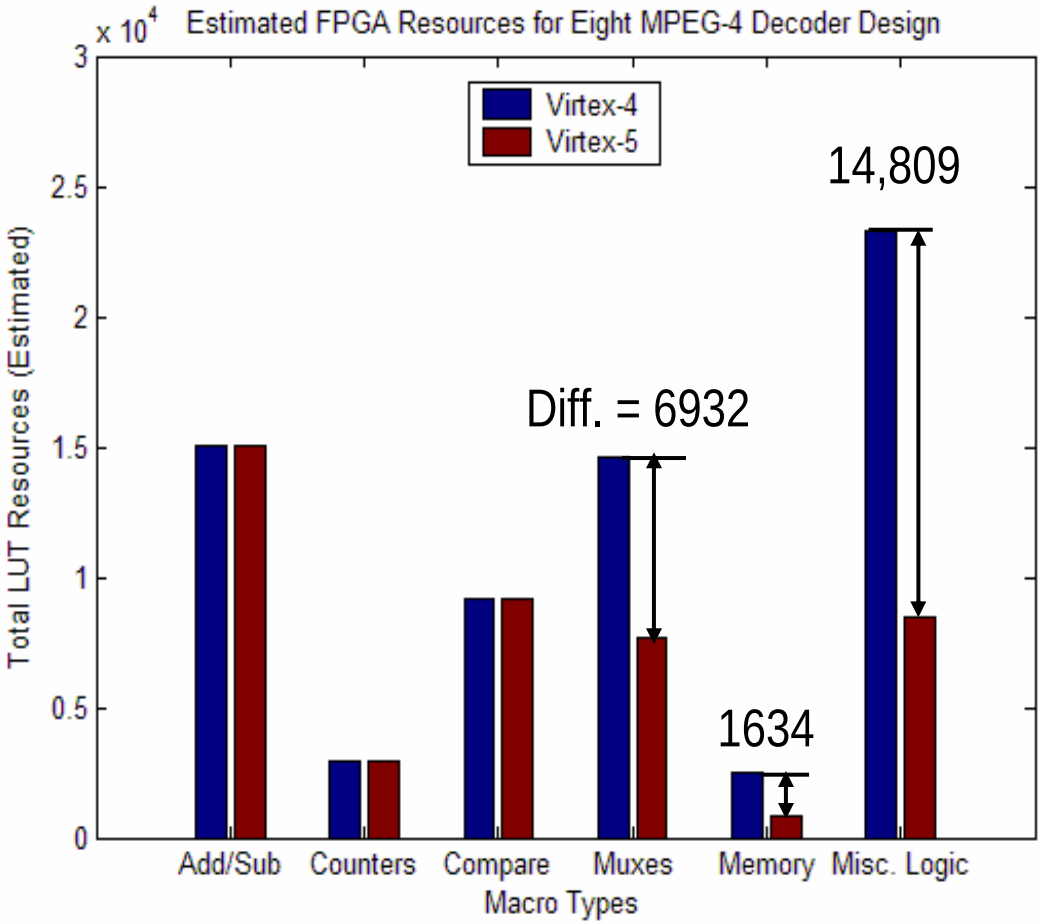


Figure 1. IP router architecture, showing two of the 16 ports

- Note: Registers are associated with bit widths

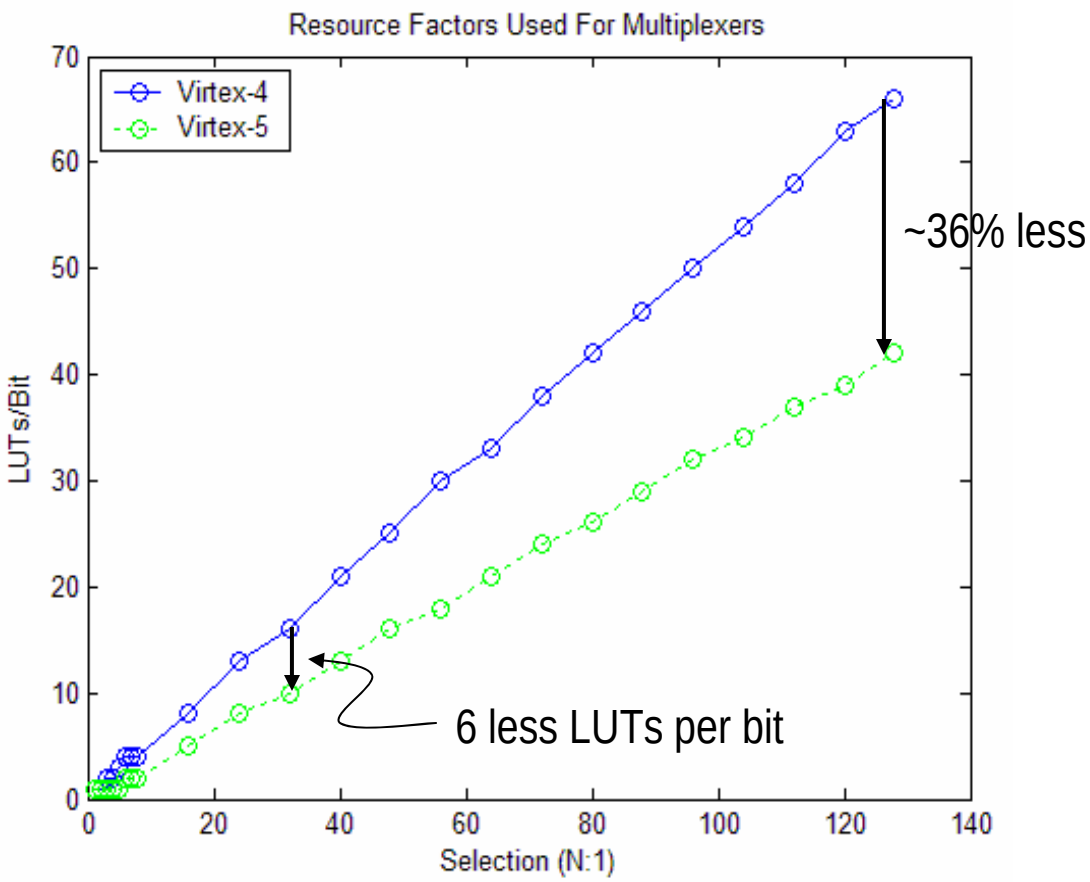
8 Decoders: Resources



Design Resources	Virtex-4	Virtex-5
	Used	Used
Registers	21,248	20,242
LUTs	**67,523**	**44,148**
BlockRAMs	233	233
DSP Elements	192	216

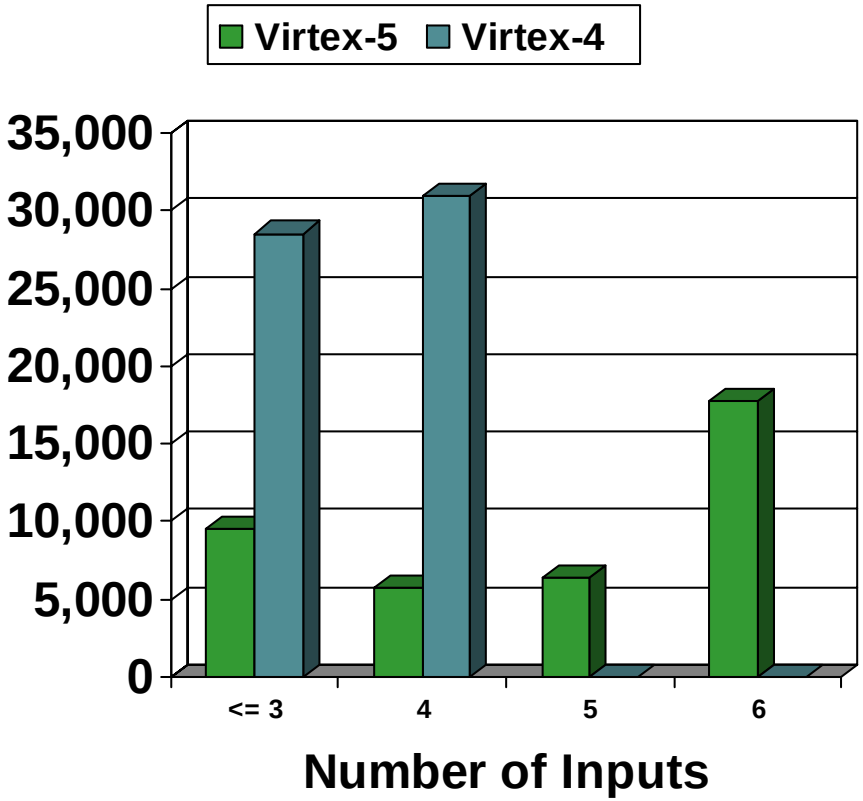
- 35% fewer LUTs
- dramatic improvements for multiplexers, memory, and misc. logic
- Same VHDL source code used for both designs

Virtex-5: Multiplexers



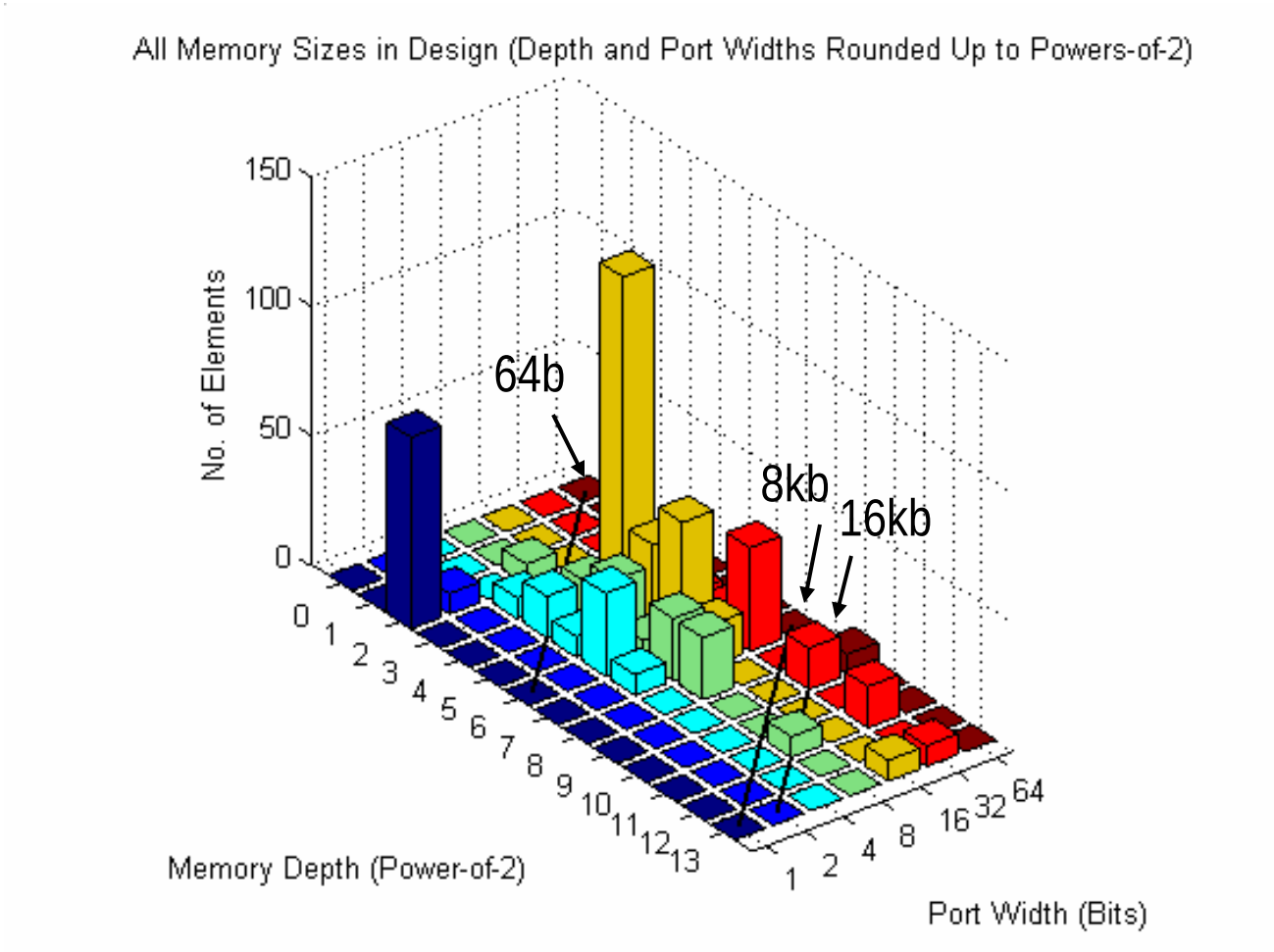
- Six-input LUTs provide efficient implementations of multiplexers
- Data derived from independent test cases

Logic Synthesis-Driven Results



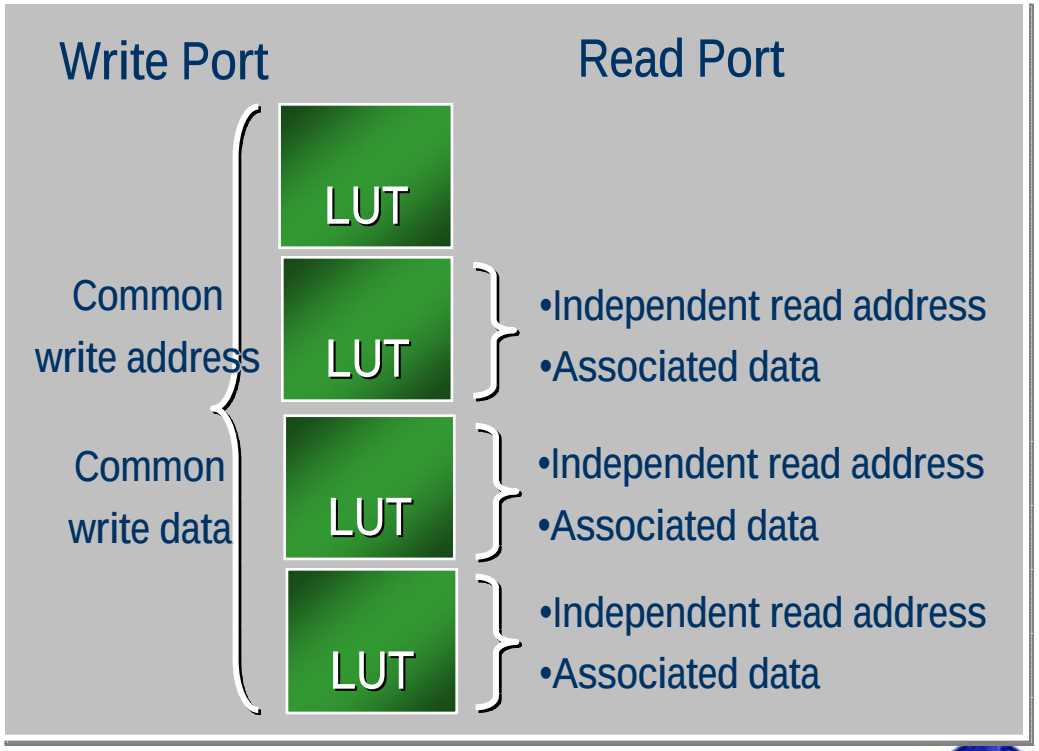
- Synthesis uses 6-input LUTs efficiently : fewer logic levels
- 23% increase in synthesized frequency, from 95MHz to 117MHz
- From 720p to 1080p video standards with little effort

Memory Analysis

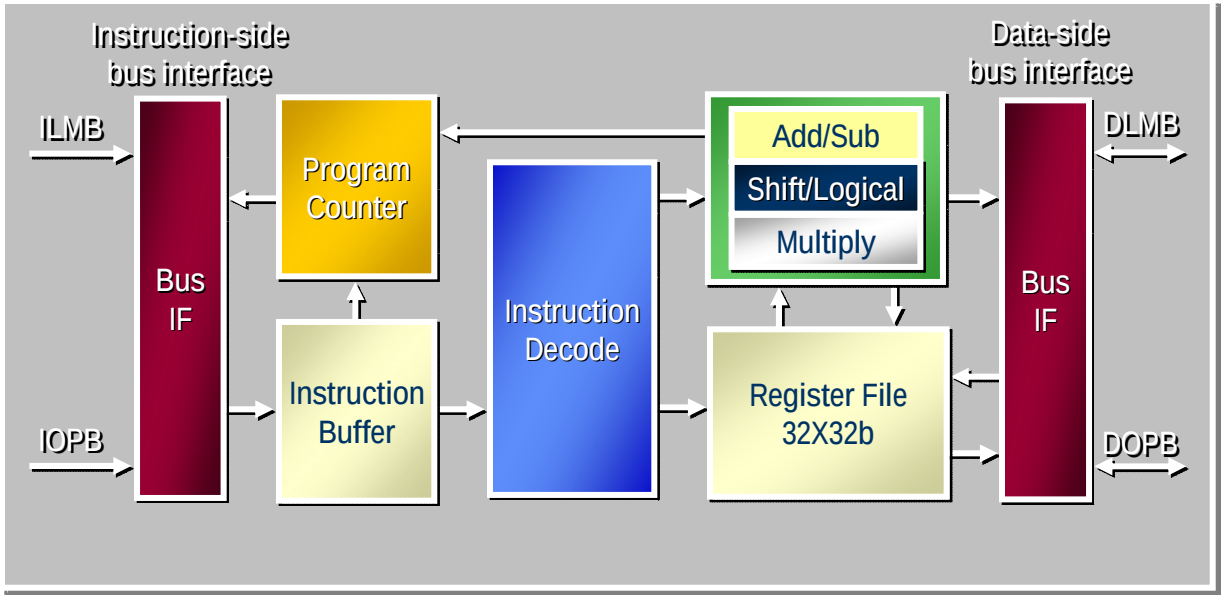


Quad-Port Memory in Four LUT6

- Write Port: Four LUT6s share the data input and can also share a distributed write address
- Read Ports: Three independent read operations
- 32 x 32 Quad-Port RAM structure in 64 LUTs
- 6x density improvement over Virtex-4



Application Example: new MicroBlaze 5.0

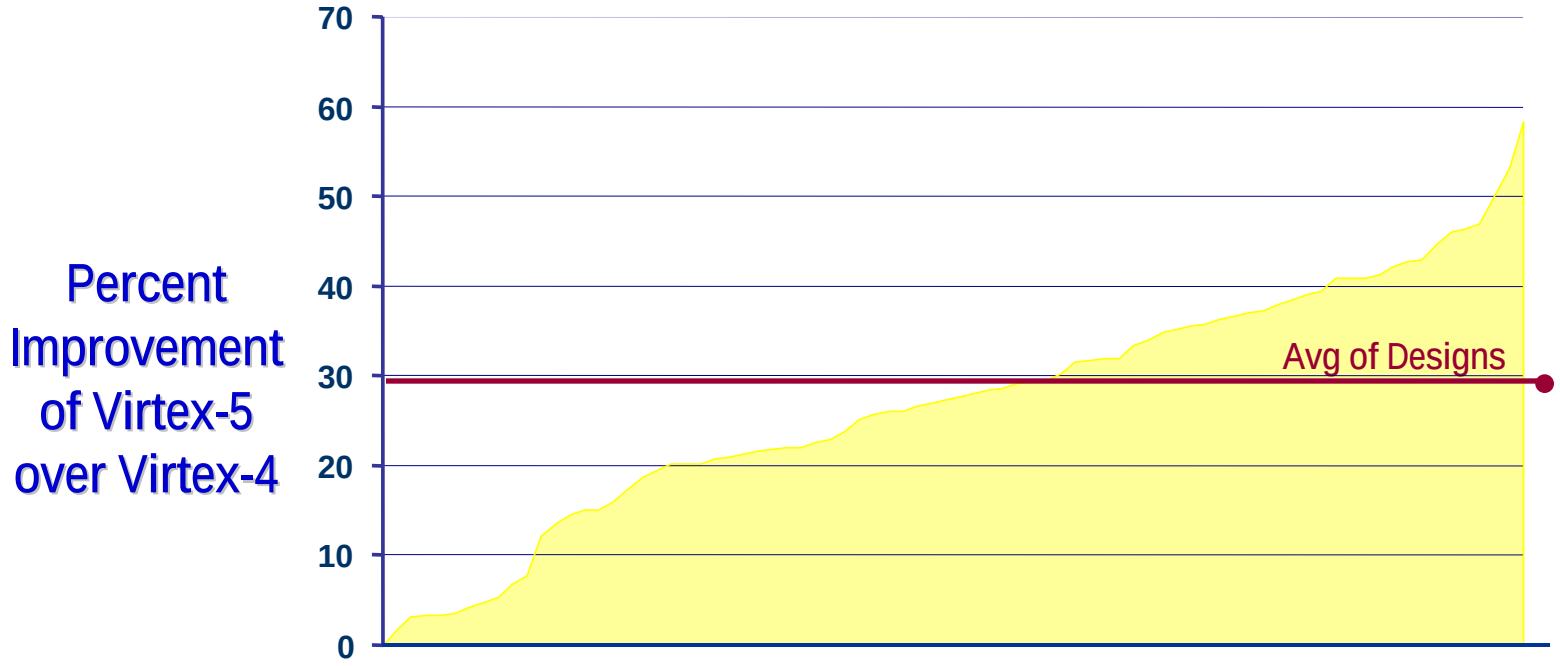


- Better use of new LUTs
  - 1269 LUT4s in Virtex-4, MB 4.0
  - 1400 LUT6s in Virtex-5, MB 5.0
- from 3 stage -> 5 stage pipeline
- new processor: from 0.92 DMips/MHz to 1.14 DMips/MHz
- 180MHz -> 201 MHz
- 166 -> 230 Dhrystone Mips

Use new 6 LUT, 2 stage deeper pipe, 10% more MHz, 39% better performance

Suite of Benchmarks

Suite of 74 designs run against ISE8.1i
Slow speedgrade (-10) Virtex-4 compared to slow speedgrade (-1) Virtex-5



~30% average advantage for Virtex-5 fabric vs. Virtex-4

- As high as 56% advantage for some designs

Benchmark: Summary

- Virtex 5: Leading 65 nm technology FPGA platform
- New 6-input LUT logic that is 30% better
- Range of Memory sizes mapped onto LUTram and BRAM
- Demonstrated example of video benchmark with 35% fewer LUTs and 23% increased frequency
- New Microblaze with 39% improved performance
- FPGA design will be driven by system level benchmarks