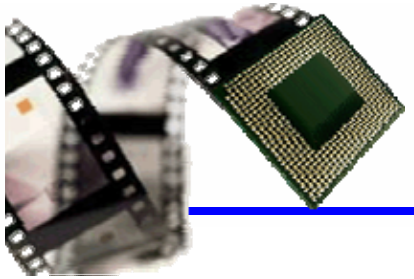


MPSOC'06

Developing a fully Scalable MPEG-4 AVC/ H.264 Video Codec using a proven MPSoC architecture and heterogeneous design methodology

Ian Walsh, CEO
MnD Semiconductors
August 17, 2006
Estes Park, Colorado, USA

Key Question

Can Multiprocessor architecture based solutions versus Multiple Processor solutions be commercially competitive and technically viable, providing OEMs a real value proposition?

If so, great and how can we capitalise on this?

If not, then ……..

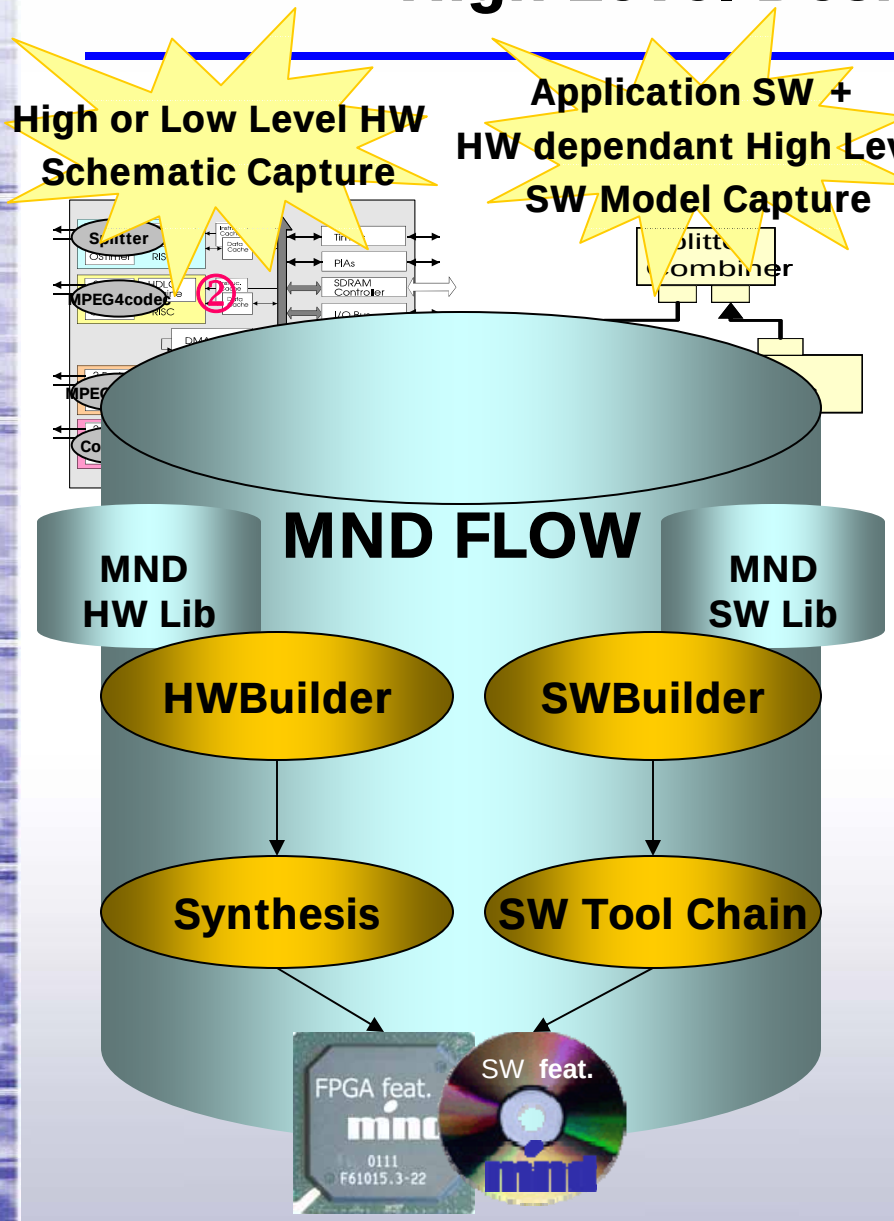
Design Brief

- MPEG-4 AVC / H.264 video codec, including single or multi-channel, High Profile Encoder, Decoder and Transcoder
- Fully scalable and programmable solution
- For one or more of the same MPSoC chip with software to implement any level of codec
- Performance equal to or better than current FPGA and/or DSP alternatives
- Extremely price competitive

Starting Point

- An MPSoC architecture
- A heterogeneous design methodology

High Level Design: Technology Vision

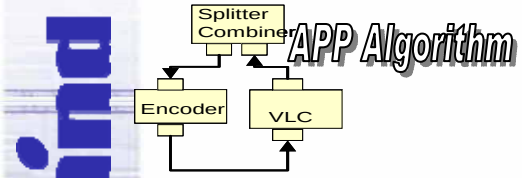


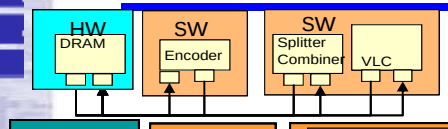
- MND provides **a flexible design platform combining** a comprehensive **HW+SW IP database** and an **environment** allowing **for powerful IP composition** and **HW/SW integration**

- **Multi-Target ASIC / FPGA / …**
- **Seamless integration with existing tools**

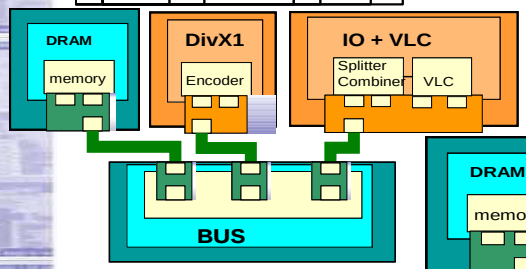
- **MND Breakthroughs:**
  - **Stable Data base concept with large flexible IP selection**
  - **HWBuilder: Powerful IP composition approach ensuring correct by construction HW**
  - **SWBuilder: Unique HW-SW Integration solution**

MND Methodology
SW driven ESL to RTL Flow

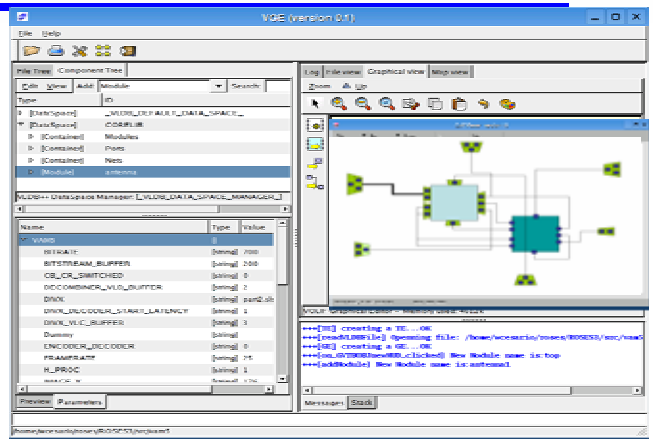


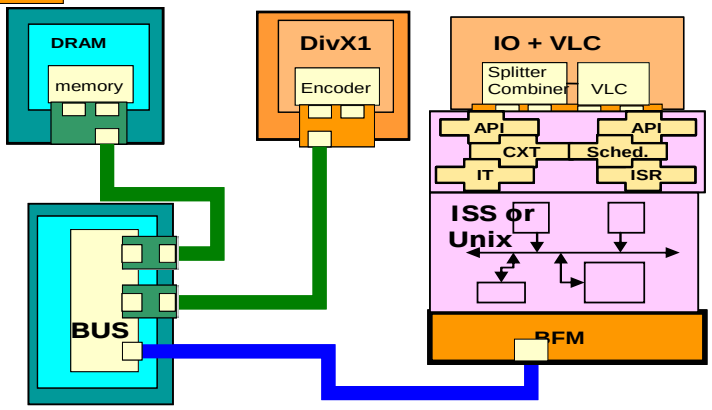


PARTITIONING



TLM PROTOTYPING

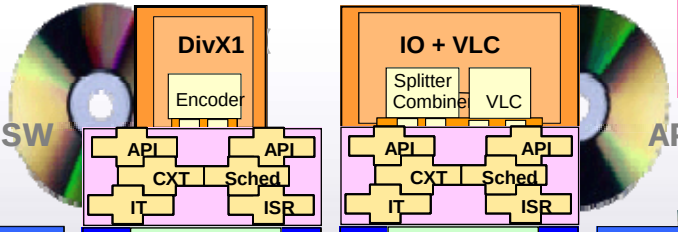




OS GENERATION
& HdS VALIDATION

SWBuilder

BINARIES PRODUCTION

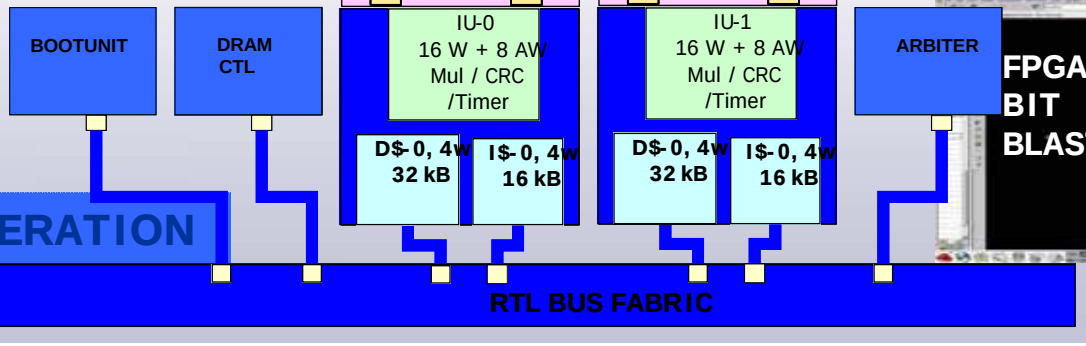


TEST SW

APP SW

FPGA FIT

HWBuilder



RTL HW GENERATION

5 Main Challenges

1. Thoroughly understanding the application and standards
2. Structuring the MPEG-4 AVC algorithm to run efficiently on the MPSoC architecture
3. Building a prototype platform that quickly enables the integration and test of RTL and application software
4. Optimising the µP cores and Instruction Set Architecture (ISA) to achieve the highest performance for the least silicon area
5. Convincing the Market Players that it is both technically viable as well as commercially viable

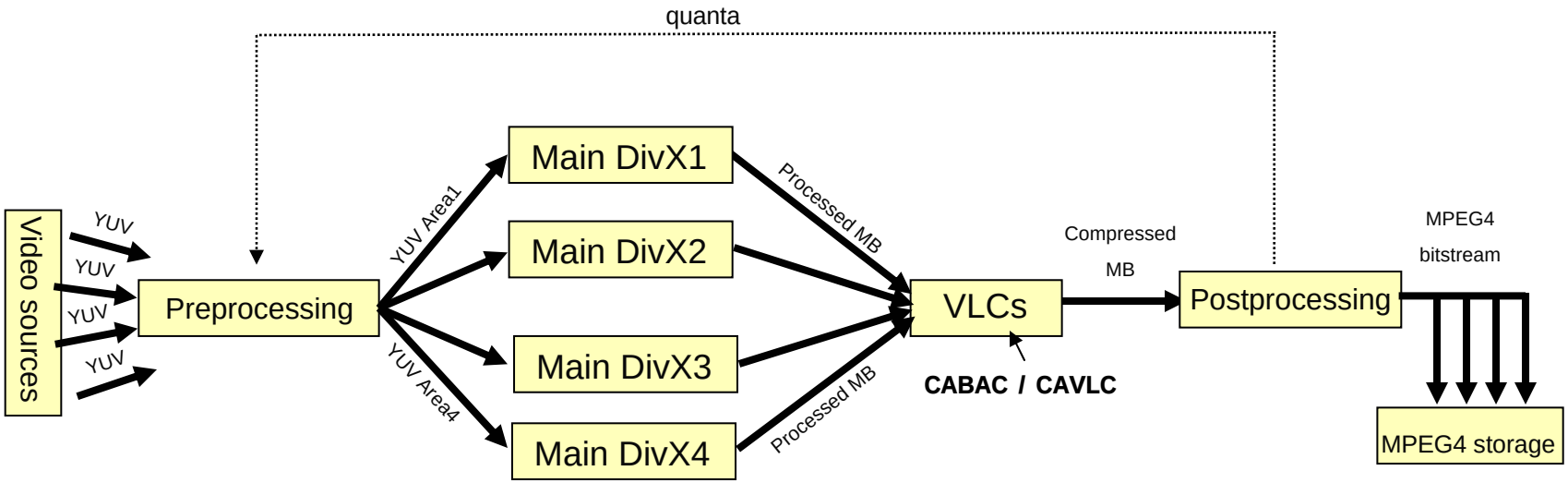
1. Thoroughly understanding the application and standards

Demands a real heterogeneous engineering team and approach in order to get an efficient solution that benefits from the intrinsic attributes of an MPSoC

- **Hardware engineers and software engineers MUST fully understand the application and standards**
- **From the Get-Go, hardware and software engineers must each appreciate each others contribution and fully support each other throughout the development, test and debug process**

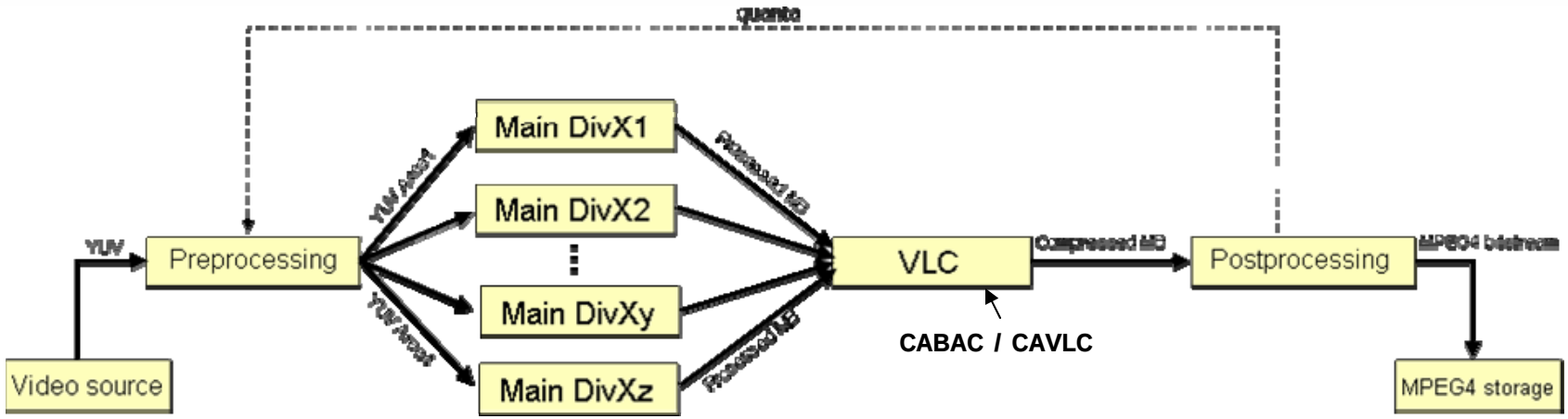
2. Structuring the MPEG-4 AVC algorithm to run efficiently on the MPSoC architecture

Parallelization of Video Streams



Exclusive Video Codec Algorithm with split screen functionality to aggregate video streams onto a common media

Multi-Processor Video Codec Solution



Small Resolution (1:1)

Tailored HW & Upgradeable SW

Exclusive
Video Codec Algorithm for
High-Quality
High Performance
On-Demand Codec

Multi-Standard

Up to High Resolution (n:m)

• Building a Prototype Platform…

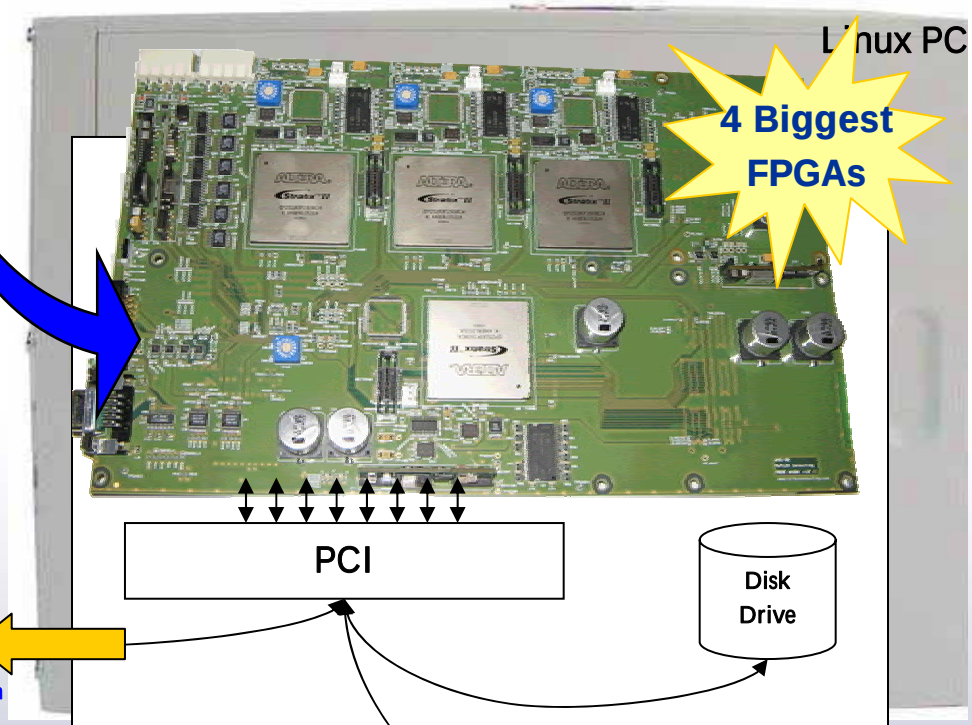
Type	Standard	Res.	fps	Freq.
Encode	MPEG4	D1	30	200

Encode / Decode | MPEG2 / MPEG4 / H.264 / … | QCIF / CIF / D1 / HD / … | … | …

Live Video stream from Camera to Video player on the screen

Video Monitor

Linux PC



Digital Camera

Output: MPEG4 Bitstream

Input : YUV411 Bitstream

4. Optimising the µP cores and Instruction Set Architecture (ISA)…

Challenges from the Algorithm:

- Pipelining
- Parallelization
- Preload
- Memory versus registers
- Parameterization

µP Core and ISA solutions:

- Video Coprocessor with SIMD instructions
- Inter µP messaging
- Inter chip connectivity