A Configurable Processor for Outer Modem Applications

- A Contribution to Software Defined Radio -

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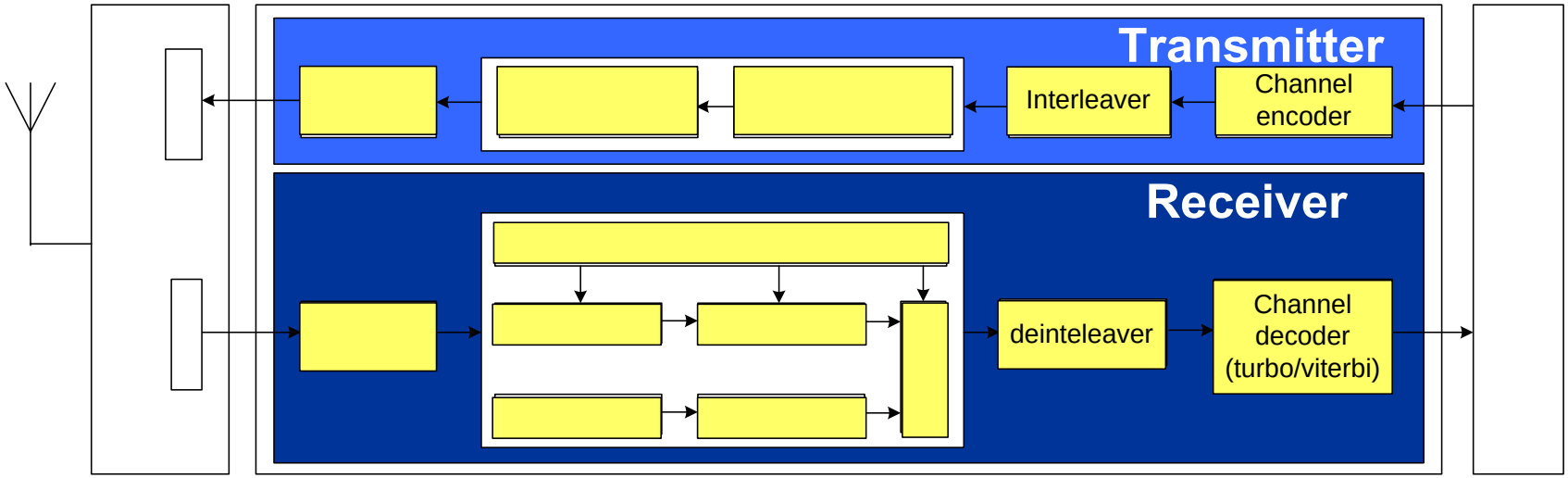
Wireless Flexibility Requirements

- Terminals have to support different layers
  - ⇨ E.g. Personal network, hot spot, cellular
- Typically different standards exist for each layer
  - ⇨ E.g. UMTS, CDMA2000
- Evolution of individual standards
  - ⇨ E.g. UMTS -> HSDPA
- Support of different standards at the same time
  - ⇨ E.g. DVB Downlink + UMTS Uplink
  - ⇨ E.g. horizontal (Intra-Layer) + vertical (Inter-Layer) „handover“
- Adaption to different QoS requirements
  - ⇨ E.g. Content (Voice/Data), channel
- Future systems have to be adaptive
  - ⇨ Adaptive self-configuration of e.g. modulation and coding dependent on the current system context, channel state and QoS requirements

Anatomy of Wireless Protocols



Filtering: suppress signals outside frequency band

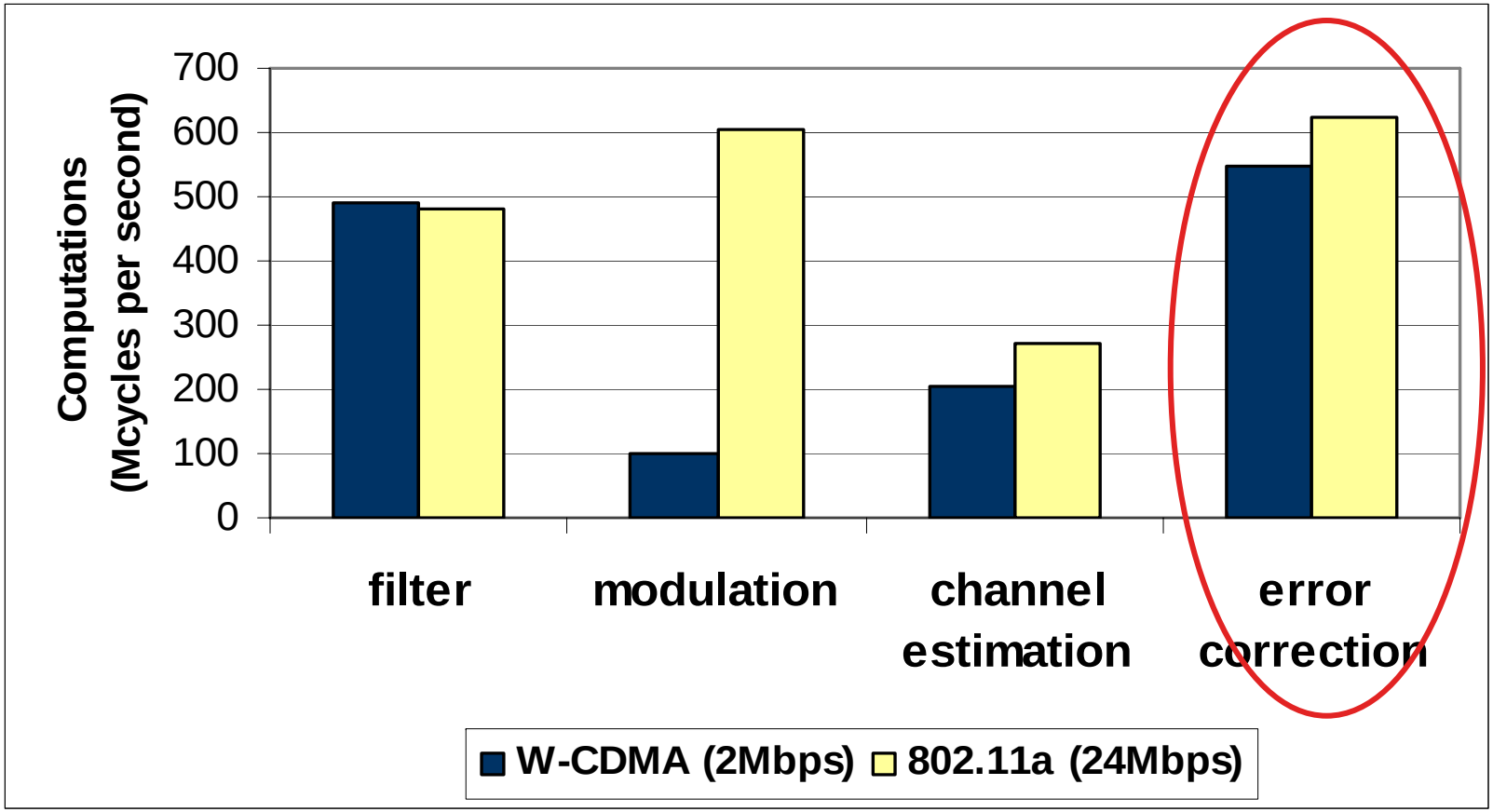
Modulation: map source information onto signal waveforms

Channel Estimation: Estimate channel condition for transceivers

Error Correction: *correct errors induced by noisy channel*

Source: Scott Mahlke / MPSoC'06

Software Defined Radio - Performance



- 802.11a has higher number of total computational cycles
- W-CDMA requires higher computational cycles per bit

Source: Scott Mahlke / MPSoC'06

Channel Codes used in Standards

Standard	Codes	Rates	States	Blocksizes	Throughput*
GSM	CC	1/2...1/10	16, 64	33...876	...12 kbps
EDGE	CC	1/2,1/3	64	39...870	5...62 kbps
UMTS	CC	1/2,1/3	256	1-504	...32 kbps
	TC	1/3	8	40-5114	...2 Mbps
CDMA-2k	CC	1/2...1/6	256	1-744	...38 kbps
	TC	1/2...1/5	8	378...20736	...2 Mbps
IEEE802.11	CC	1/2...3/4	64	1-4095	6...54 Mbps
	CC	2/3	256		
	LDPC	1/2...5/6	-	...1944	...450 Mbps
Hiperlan	CC	1/2,9/16,3/4	64	1-4095	6...54 Mbps
IEEE802.16	CC	1/2...7/8	64	...2040	...24 Mbps
	DB-TC	1/2...3/4	8	... 648	...24 Mbps
	LDPC	1/2...3/4	-	...~2500	>100Mbps
DVB-S2	LDPC	¼..9/10	-	...58192	...40 Mbps
Inmarsat	TC	1/2	16	...2500	...64kbps

* throughput/channel

Outer Modem State-of-the-art

- **ASIC IP blocks (e.g. STM Greenside chip - Basestation application)**
  - ⇨ For each code: implement different channeldecoder
  - ⇨ High architectural efficiency, very limited flexibility
- **Processor (e.g. Alcatel Evolium 4 x ADI Tigersharc - Basestation application)**
  - ⇨ Instruction-level flexibility, simple programming model
  - ⇨ Relatively low architectural efficiency, large latency
- **FPGA (e.g. NDSatCom - Satellite application)**
  - ⇨ Bit-level flexibility, complex programming model
  - ⇨ Moderate performance, medium architectural efficiency
- **ASIPs: application specific instruction set processors**
  - ⇨ Design time e.g. Tensilica, LISATek, ARC
  - ⇨ Reconfigurable array as functional unit in processor pipeline e.g. XiRisc

dr-ASIP Architecture

- Exploit IS programmability
  - ⇨ Simple programming model
  - ⇨ Decoding algorithms e.g. Log-MAP, Viterbi
- Exploit hardware reconfigurability
  - ⇨ Fast run-time switching
  - ⇨ Code parameters e.g. constraint length, polynom

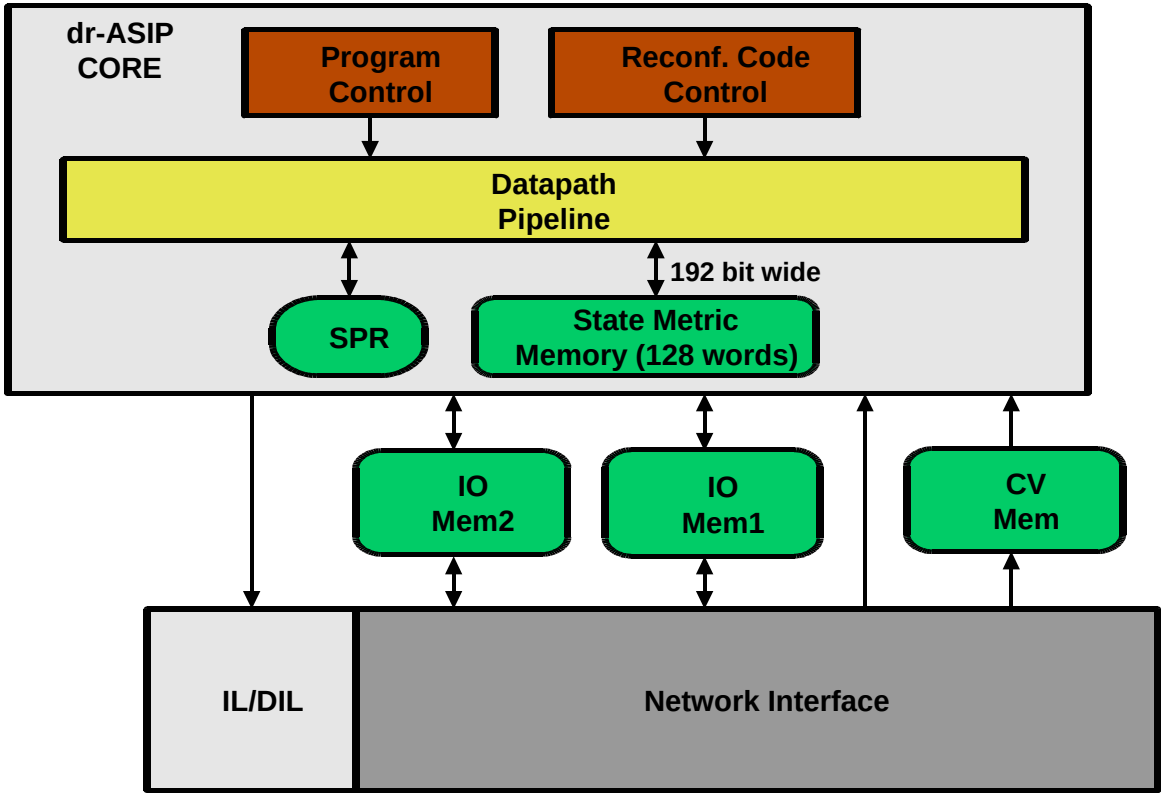
Dynamically reconfigurable ASIP (dr-ASIP)

- Specific application: application knowledge is key
  - ⇨ Profiling / inspection of C-Code doesn‘t help
  - ⇨ Full ASIP approach i.e. no predefined configurable pipeline template
  - ⇨ „Just enough flexibility“ (bottom up approach)
  - ⇨ Assembler code

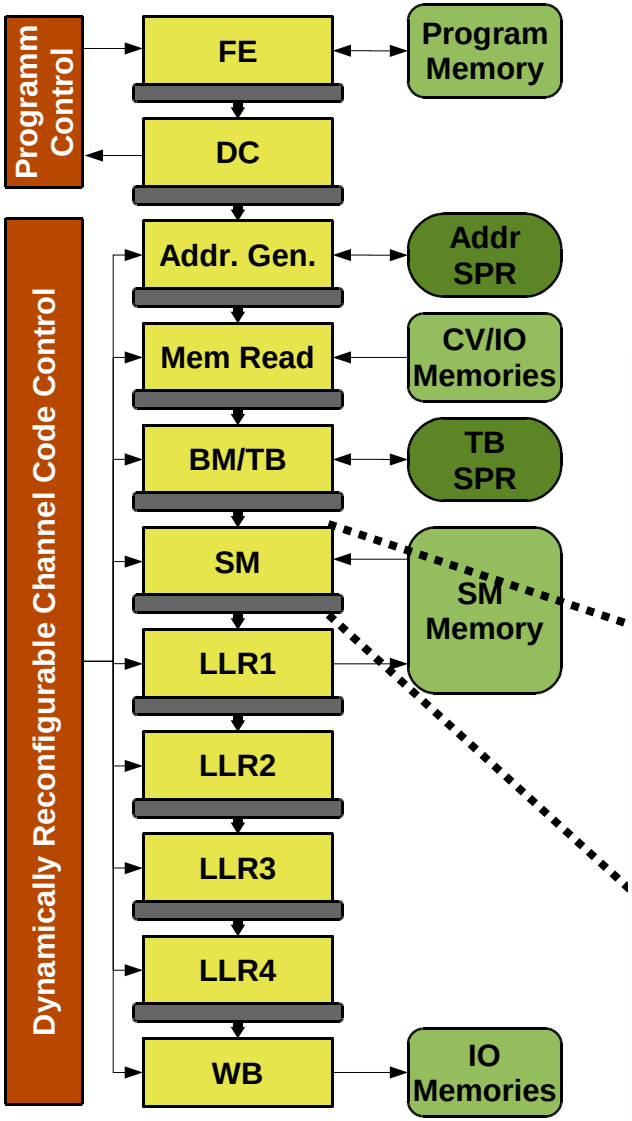
dr-ASIP Architecture

LISATek approach

- No limitation on design space
- Application specific instruction set, memory structure and irregular datapath
- Packet based Network Interface



Datapath Pipeline



- Address, control, algorithmic instructions (24 bit)
- 1 cycle dynamic reconfiguration
- 629 bits reconfiguration memory

```
reconf
stAZS 0
setCVA 0x8000
setAPWiRDA 0x2000
ldSMR 0
fwdrec 3,1,1
fwdrec 3,1,2
...
fwdrec 3,1,18
fwdrec 3,1,19
modCVA 60
modAPWiRDA 20
setWBA 0x4000
modWBA 19
RPT NXT_2 9_times
  bwdacq -3,-1
  bwdacq -3,-1
  bwdrecapo -3,-1,19
  bwdrecapo -3,-1,18
  ...
  bwdrecapo -3,-1,2
  bwdrecapo -3,-1,1
  bwdrecapo 0,0,0
RPT NXT_50 2_times
  modCVA 57
  modAPWiRDA 19
  ldSMR 19
  fwdrec 3,1,0
  fwdrec 3,1,1
  ...
  fwdrec 3,1,18
  fwdrec 3,1,19
  modCVA 60
  modAPWiRDA 20
  modWBA 39
  ldSMR 63
  RPT2 NXT_2 9_times
    bwdacq -3,-1
    bwdacq -3,-1
  bwdrecapo -3,-1,19
  bwdrecapo -3,-1,18
  ...
  bwdrecapo -3,-1,2
  bwdrecapo -3,-1,1
  bwdrecapo 0,0,0
modCVA 57
modAPWiRDA 19
ldSMR 19
fwdrec 3,1,0
fwdrec 3,1,1
...
fwdrec 3,1,18
fwdrec 3,1,19
stAZS 63
modCVA 6
modAPWiRDA 2
modWBA 39
ldSMR 63
bwdacq -3,-1
bwdacq -3,-1
bwdrecapo -3,-1,19
bwdrecapo -3,-1,18
...
bwdrecapo -3,-1,2
bwdrecapo -3,-1,1
bwdrecapo 0,0,0
RPT NXT_2 FOREVER
  nop
  nop
```

Results

Synthesis with 65nm low power standard cell library

- 56Kgates (~ 0.1mm^2) @ 400 MHz clock frequency
- Turbo decoder throughput up to 20 Mbps @ 5 iterations (w/o IO)
- Convolutional decoder throughput up to 133 Mbps (w/o IO)

Comparison Turbo-Decoding

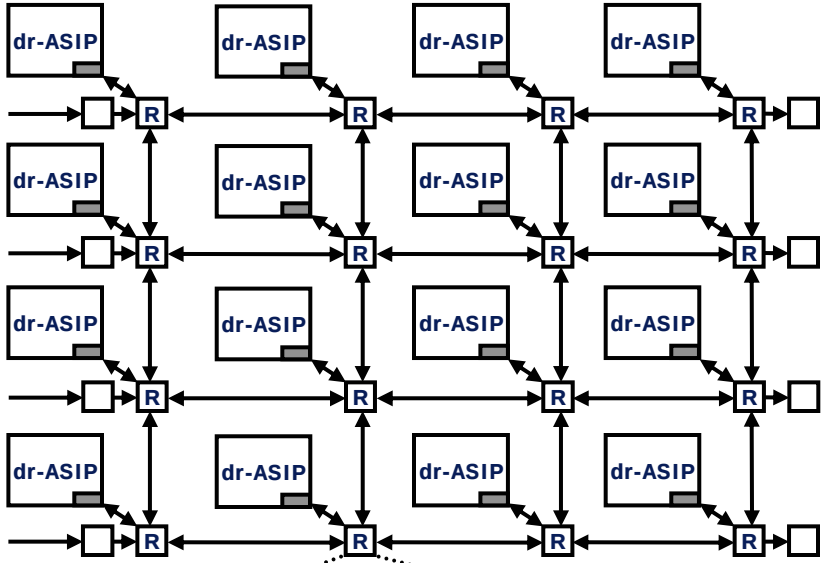
- XiRisc (DATE04) : ~ 0.1 Mbps @ 100MHz @ 180 nm
- Tensilica Core (DATE03) : ~ 1.4 Mbps @ 133MHz @ 104 Kgates @ 180nm
- ENST ASIP (DATE06) : ~ 4.4 Mbps @ 335MHz @ 93Kgates @ 130nm

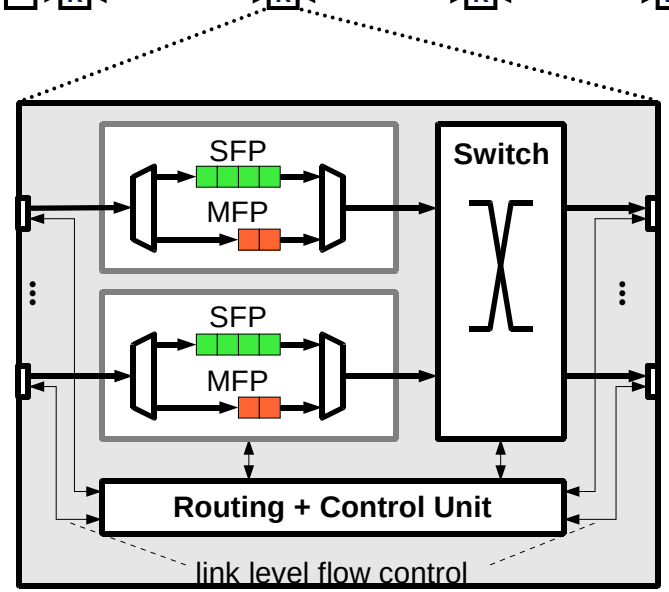
<u>Multiprocessor Architecture (MPSoC)</u>

- Nodes: dr-ASIP
- Communication Network
  - ⇨ I/O traffic & configuration data: long data blocks
    - – Irregular random traffic
    - – Multiple flit packets, wormhole routing
  - ⇨ Interleaving traffic: small blocks with high throughput
    - – Uniform traffic
    - – single flit packets: store & forward control

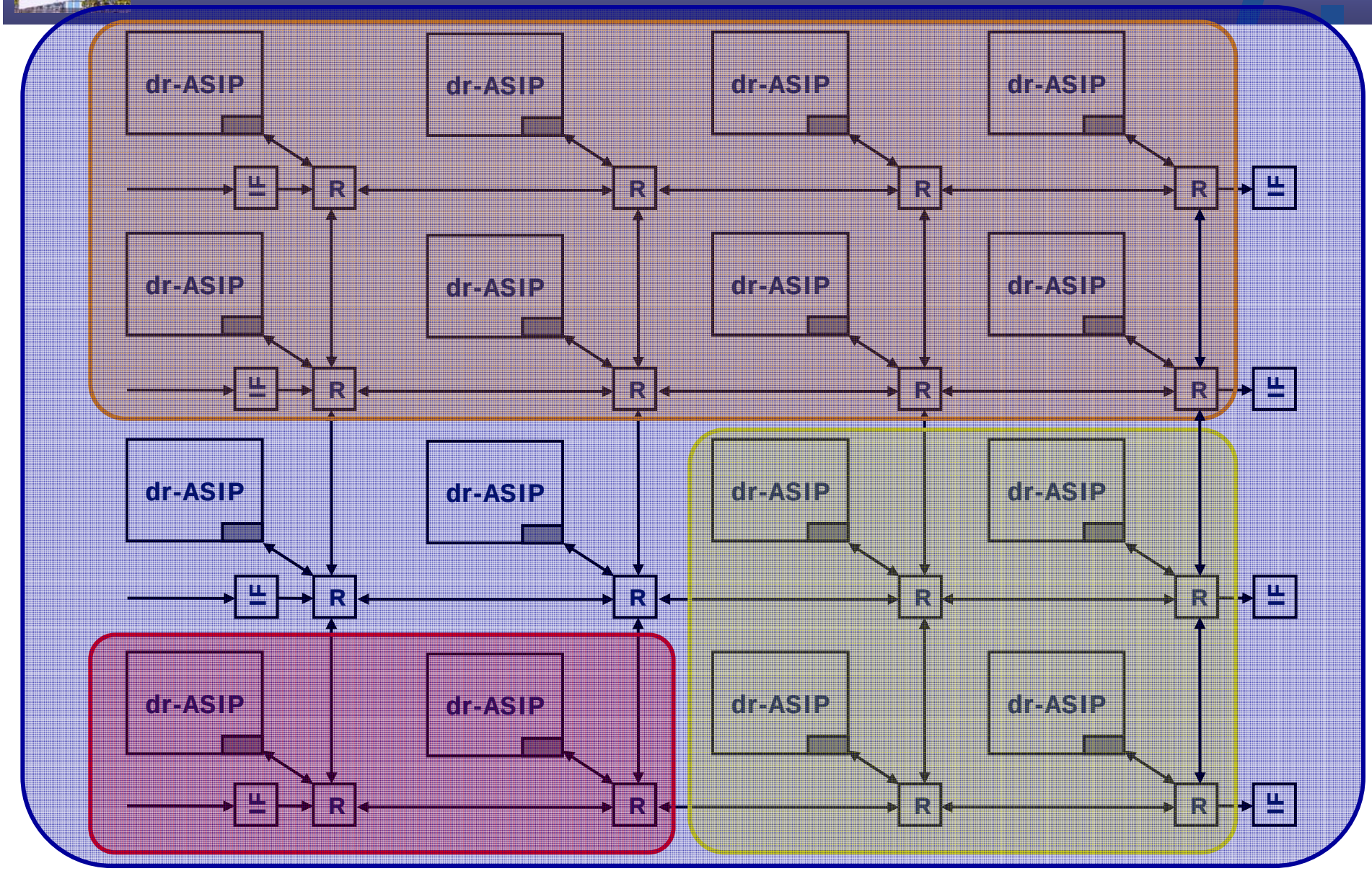
MPSoC

- 2D mesh topology
  - ⇨ Regularity/scalability
- Dimension-Order Routing
  - ⇨ Deterministic
  - ⇨ Good performance
  - ⇨ Efficient to implement
- Input-queued router
  - ⇨ Two virtual channels
  - ⇨ Higher priority for SFP





Reconfigurable Array



Results

Standard	Codes	Rates	Throughput	Architecture
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EDGE	CC	1/2,1/3	5...62 kbps	dr-ASIP
UMTS	CC	1/2,1/3	...32 kbps	dr-ASIP
	TC	1/3	...2 Mbps	dr-ASIP
CDMA-2k	CC	1/2...1/6	...38 kbps	dr-ASIP
	TC	1/2...1/5	...2 Mbps	dr-ASIP
IEEE802.11	CC	1/2...3/4	6...54 Mbps	MPSoC
	CC	2/3		
	LDPC	1/2...5/6	...450 Mbps	in progress
Hiperlan	CC	1/2,9/16,3/4	6...54 Mbps	MPSoC
IEEE802.16	CC	1/2...7/8	...24 Mbps	dr-ASIP
	DB-TC	1/2...3/4	...24 Mbps	in progress
	LDPC	1/2...3/4	>100Mbps	in progress
DVB-S2	LDPC	1/4...9/10	...40 Mbps	in progress
Inmarsat	TC	1/2	...64kbps	dr-ASIP

Conclusion

- Channel decoder is an important building block in baseband processing of wireless communication systems

- Combination of application specific IS programmability with dynamic hardware reconfigurability provides very good trade-off between flexibility and performance

- Flexible LDPC decoder implementation is the next big challenge

For more information please visit

www.eit.uni-kl.de/wehn