Hardware/Software Co-Design of an FPGA-based Embedded Tracking System

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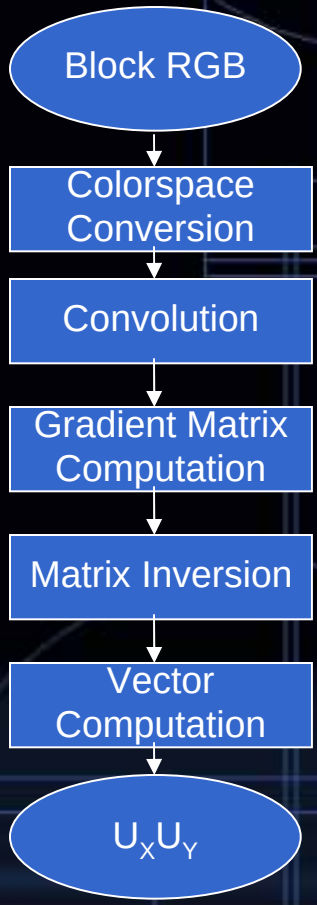
Overview

- Our group assisted in hardware design for surveillance system
- Requirements included:
  - Mobile deployment
  - Speedup over PC/software based approach
  - Large scale deployment/low cost
  - Flexibility
- Yokogawa developed system requirements
- Verificon developed software version
- Princeton was to provide a hardware acceleration system

Task Decomposition

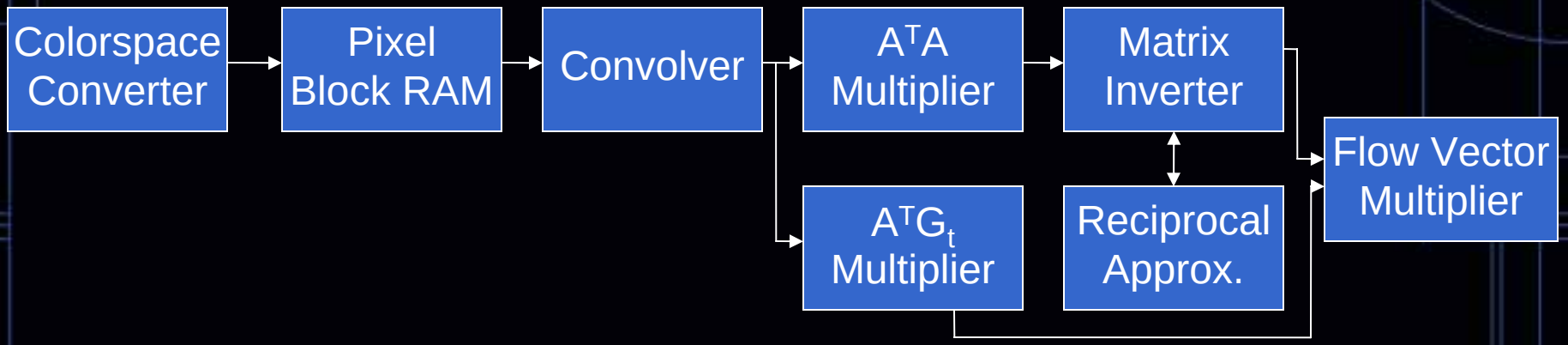
- Analyzed core of KLT algorithm for constituent tasks
- From colorspace conversion on, fractional notation required
- Convolution and matrix multiplication imply need for multipliers and adders
- Matrix inversion?



Representation

- Originally computed limits for fixed-point representation
- Feasibility measure acquired based on 14-bit data values
- Deemed insufficient for algorithmic precision
- Converted arithmetic to floating-point
  - 24-bit reduced IEEE floating-point
  - Required design of FP adder and FP multiplier
- Still reliant on standard FPGA adders and multipliers
- Necessary to consider given FPGA resources

Architecture



- Convolution involves filter masks with elements either 1 or -1
- Eliminate multipliers, add/subtract units needed
- $(A^TA)^{-1}A^TG_t$ split into parallel multiplications