ADVANCE PROGRAMME

SUNDAY JUNE 24: WELCOME

18.00   **Registration**

19.00   **Welcome reception**

MONDAY JUNE 25: MPSOC APPLICATION DAY

8.30   **Registration continued**

SESSION 1: KEYNOTE

8.30   **Mario Tokoro, Sony, Japan**
On Designing Dependable Systems for Social Infrastructures

9.30   **Break**

SESSION 2: MINI-KEYNOTES

10.00   **Youn-Long Lin, National Tsing Hua University & Global Unichip Corp., Taiwan**
Design Challenge of a Super-HDTV Decoder

10.12   **Jean-Philippe Fassino, STMicroelectronics, France**
Nomadik Multiprocessing Framework, a component-based programming model for MP-SoC

10.24   **Thierry Collette, CEA LIST, France**
New Multi-Core Architecture means New execution and programming models

10.36   **Hiroto Yasuura, Kyushu University, Japan**
Dependability of MPSoC for Applications in Social Information Infrastructure

10.48   **Mark Hampton, Certess, France**
Functional Qualification for SOC

11.00   **Deepu Talla, Texas Instruments, USA**
A reference design for a DaVinci(TM) technology MPSoC targeting digital imaging consumer products

11.12   **Panel discussion with the lecturers**

12.00   **Lunch**

SESSION 3: IN-DEPTH TECHNICAL PRESENTATIONS

13.30   **Masaki Gondo, eSOL, Japan**
The need to blend SMP and AMP within a single RTOS

14.00   **Subhasish Mitra, Stanford University, USA**
Robust System Design with MPSoCs: Unique Opportunities

14.30   **Maurizio Paganini, STMicroelectronics, France**
Nomadik - the ultimate mobile multimedia processing platform

15.00   **Break**

15.30   **Jean-René Lèquepeys, CEA Grenoble, France**
Key Technologies for wireless sensor networks

16.00   **Soonhoi Ha, Seoul National University, South Korea**
A model-based embedded SW development methodology for MPSoC

16.30   **Kees Vissers, Xilinx, USA**
Building and programming complete MPSoCs in reconfigurable systems

17.00   **Panel discussion with the lecturers**

18.00   **Puppet Play (Ningyo Jyoruri)**

19.00   **Diner**

TUESDAY JUNE 26: HARDWARE DAY

SESSION 4 KEYNOTE

8.30   **Tryggve Fossum, Intel, USA**
Towards a Personal Super computer

9.30   **Break**

SESSION 5: MINI-KEYNOTES

10.00   **Olivier Franza, Intel Massachusetts, Inc., USA**
Clock System Design Risks and Opportunities under the MPSoC Paradigm

10.12   **Norbert Wehn, University of Kaiserslautern, Germany**
Reliability-Aware LDPC Decoder Architecture

10.24   **Pieter van der Wolf, NXP Semiconductors, The Netherlands**
Infrastructures for Modular Integration of MPSoCs

10.36   **Hannu Tenhunen, Royal Institute of Technology, Sweden**
Agent-Based Reconfigurability for Fault-Tolerance in Network-on-Chip

10.48   **Yankin Tanurhan, Actel Corporation, USA**
FPGA based Multi Processor Solutions for System Management in the TCA World

11.00   **Eshel Haritan, CoWare Inc., USA**
Reconstructing MPSOC – Separate Myth from Facts

11.12   **Panel discussion with the lecturers**

12.00   **Lunch**

SESSION 6: IN-DEPTH TECHNICAL PRESENTATIONS

13.30   **Soo-Ik Chae, Seoul National University, South Korea**
A SystemC-based Design Environment for Multimedia SoCs

14.00   **Toshihiro Hattori, RENESAS, Japan**
MPSoc Approaches for low-power embedded Soc's

14.30   **Doris Keitel-Schulz, Qimonda, Germany**
Memory System Solutions and its Influence on System Partitioning

15.00   **Break**

15.30   **Omar Hammami, LEI - UER-EI - ENSTA, France**
Multiobjective Design Space Exploration of MPSOC with Direct Execution

16.00   **Marek Jersak, Symtavision, Rolf Ernst, TU Braunschweig, Germany**
Formal analysis and optimization of heterogeneous networks in industrial practice - from networked systems to MpSoC

16.30   **Panel discussion with the lecturers**

17.00   **Sake Winery Visit**

20.00   **Diner**

Read more at:

http://tima.imag.fr/mpsoc/lectures.html

WEDNESDAY JUNE 27: CODESIGN DAY

SESSION 7: KEYNOTE

8.30 Hiroaki Takada, Nagoya University, Japan
Embedded System and Multi-Processor Technology Trends in the Automotive Industry

SESSION 8: IN-DEPTH TECHNICAL PRESENTATIONS

9.30 Takashi Miyamori, Toshiba, Japan
MPSoC Architecture Trade-offs for Multimedia Applications

10.00 Frederic Petrot, TIMA Laboratory, France
Abstract executable modeling of MPSoC HW/SW interfaces

10.30 Break

SESSION 9: MINI-KEYNOTES

11.00 Marcello Coppola, STMicroelectronics, France
An innovative EDA flow for on-chip communication infrastructure

11.12 Frank Schirrmeister, Imperas, Inc., USA
The Impact of MPSoC Requirements on Software Programming

11.24 Kees Goossens NXP Semiconductors, The Netherlands
Debug, Test, and Security Services on Networks on Chip

11.36 Wayne Wolf, Princeton University, USA
Computer Vision and MPSoCs

11.48 Jan Madsen, TUD, Denmark
If Formal Analysis is the Answer – What was the Question?

12.00 K. Charles Janac, Arteris, France
When is the use of a NoC Most Effective and Why

12.12 Drew Wingard, Sonics Inc.,USA
High-performance multithreaded memory subsystems for MPSoC's

12.24 Panel discussion with the lecturers

13.30 Lunch

14.45 Trip to Whirlpool and Dinner

THURSDAY JUNE 28: SOFTWARE DAY

SESSION 10: IN-DEPTH TECHNICAL PRESENTATIONS

8.30 Heinrich Meyr, RWTH Aachen University, Germany
Re-configurable ASIPs: Is there any need for these architectures?

9.00 Atsuhiro Suga, Fujitsu Laboratories Ltd., Japan
Automatic thread distribution mechanism suitable for an embedded multicore processor platform

9.30 Michael Vinov, IBM Research Lab at Haifa, Israel
Challenges in the verification of high-end Systems on a Chip

10.00 Break

SESSION 11: MINI-KEYNOTES

10.30 John Goodacre, ARM, UK
Extending the Cortex ARM version-7 architecture for next generation multicore

10.42 Gert Goossens, Target Compiler Technologies, Belgium
Ultra-Low Power? Think Multi-ASIP SoC!

10.54 Ulrich Ramacher, Infineon Technologies AG, Germany
Proposal for comparison of SDR baseband solutions

11.06 Rainer Leupers, RWTH Aachen, Germany
HySim: Fast Hybrid Processor Simulation for MPSoC Virtual Platforms

11.18 Masaharu Imai, Osaka University, Suita, Japan
A System Level Modeling Method using SystemC for RTOS Centric Embedded Systems

11.30 Ahmed Jerraya, CEA-LETI, France
An open platform to build MPSoC from Components

11.42 Panel discussion with the lecturers

12.00 Lunch

SESSION 12: IN-DEPTH TECHNICAL PRESENTATIONS

13.30 Kazutoshi Wakabayashi, NEC Corp., Japan
MPSoC with many Configurable Processors and design environment

14.00 Rudy Lauwereins, IMEC, Belgium
Solving the idle power problem of a multi-core software defined radio

14.30 Lothar Thiele, ETH Zurich, Switzerland
Modular Performance Analysis of MPSoC

15.00 Break

15.30 Mitsuhisa Sato, University of Tsukuba, Japan
Towards a high performance parallel platform for dependable embedded systems

16.00 Hiroyuki Tomiyama, Nagoya University, Japan
RTOS-centric cosimulation of MPSoC

16.30 Eric Verhulst, OpenLicenseSociety, Belgium
Formal modeling and a network centric Real-Time Operating System in less than 2K Bytes as a generic base for MP-SoC and Process Oriented Programming

17.00 Panel discussion with the lecturers

19.00 Diner with Concert of Piano and Vocal

FRIDAY JUNE 29: BUSINESS DAY

SESSION 13: KEYNOTE

8.30 Allen C. H. Wu, Syntronix, Taiwan
Business Changes and Challenges in the Competitive Semiconductor Industry

9.30 Break

SESSION 14: MINI-KEYNOTES

10.00 Joachim Kunkel, Synopsys, USA
Will MPSoCs make the adoption of ESL tools finally mandatory?

10.30 Chris Rowen, Tensilica, USA
Putting MPSOC to Work in Multimedia

11.00 Masao Nakaya, Renesas, Japan
Economics and Performance of Advanced SoC

11.30 Panel discussion with the lecturers

12.00 Lunch