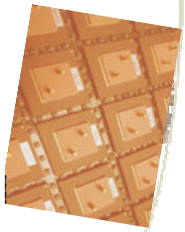
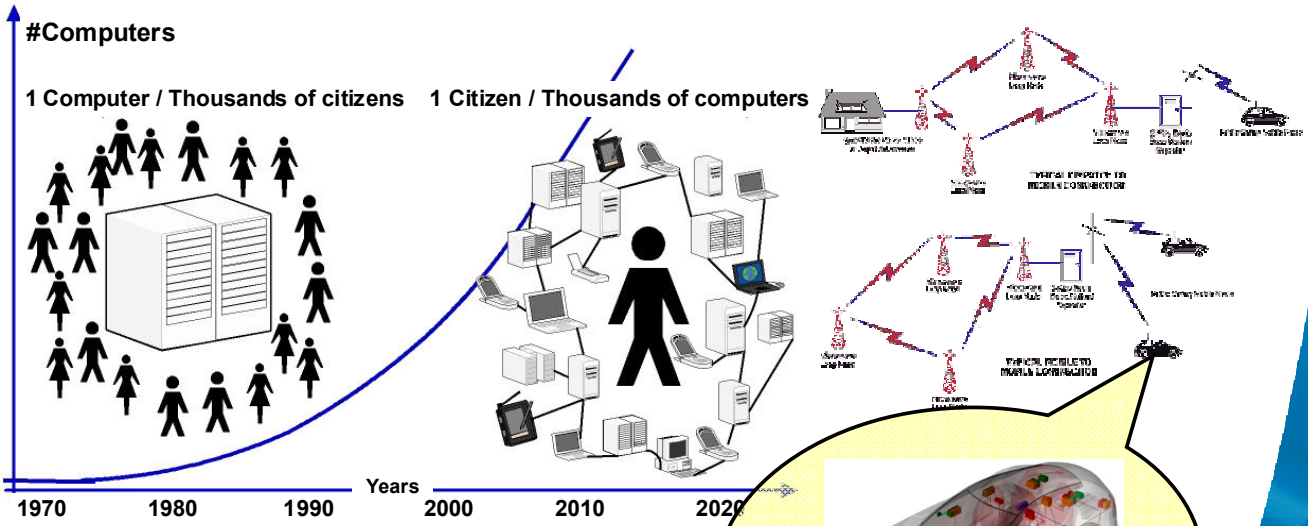


New architecture means new execution model and programming model

Thierry Collette
CEA LIST
Thierry.collette@cea.fr

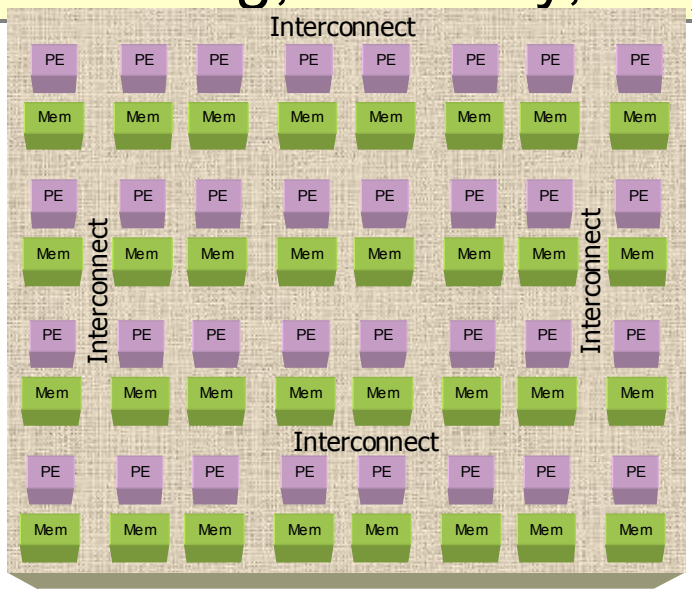
Evolution of the embedded computing



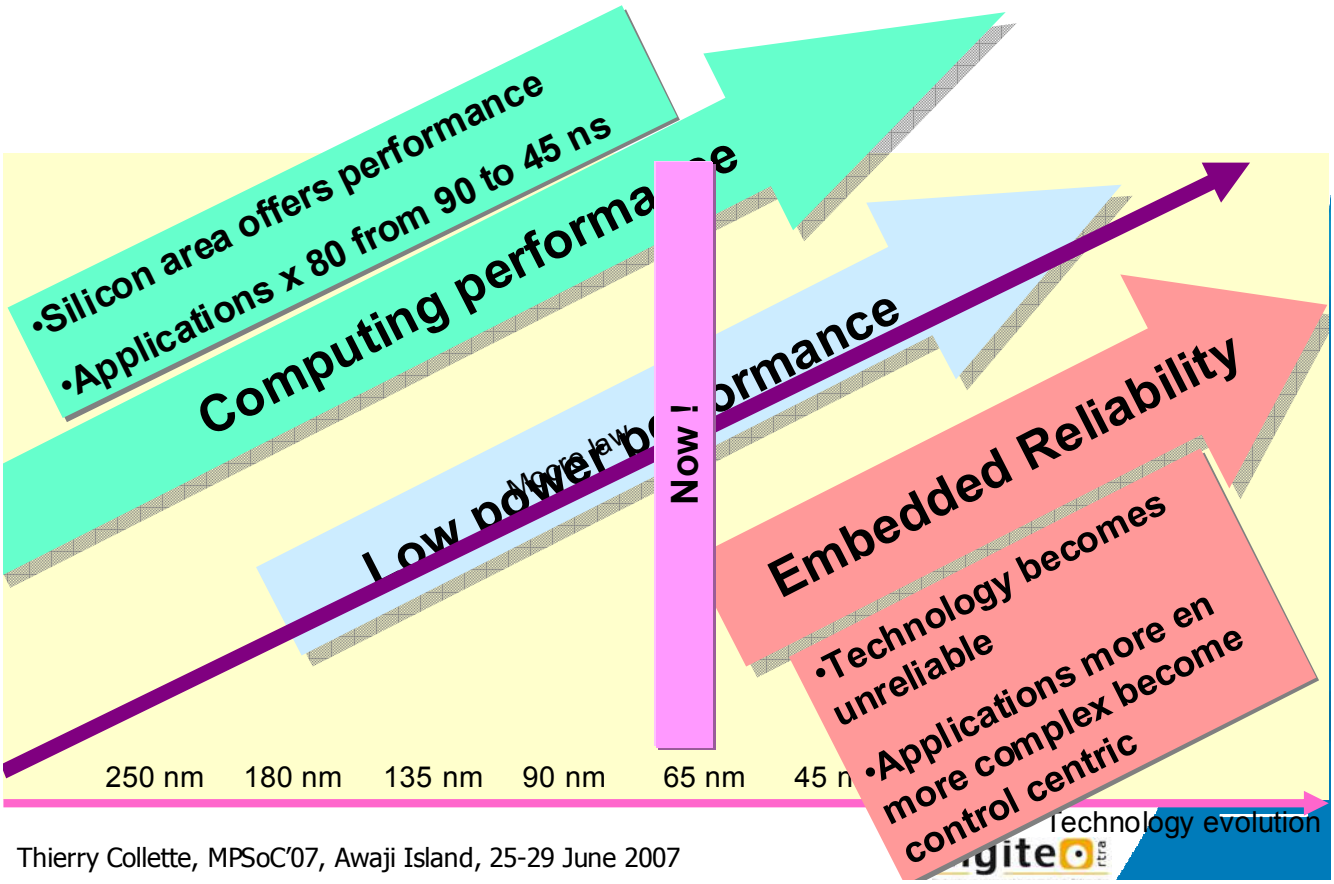
The embedded computing paradigms are different and **will remain different**

Next steps?

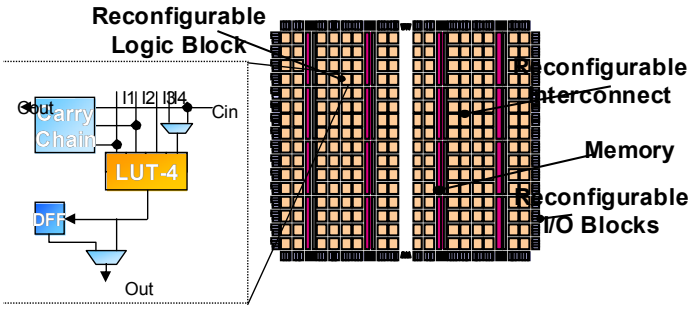
(More than 100 Processors, debug, reliability, …!)

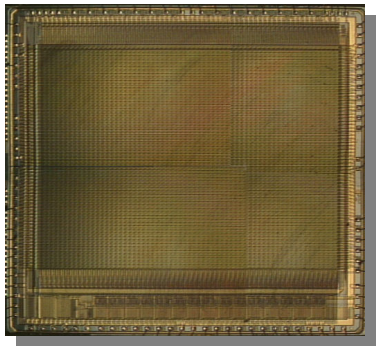


Trends in technology and application road maps



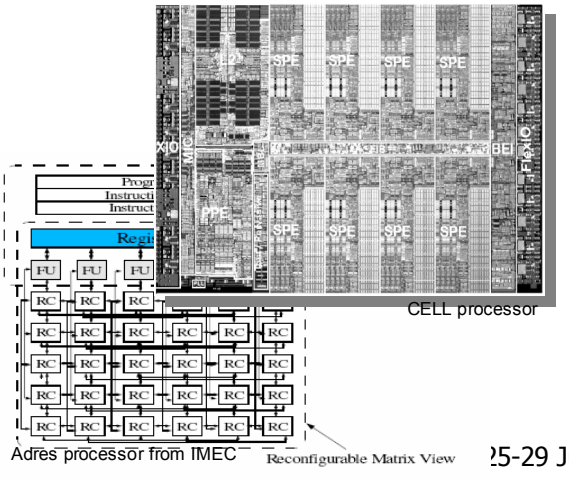
Regular fabrics



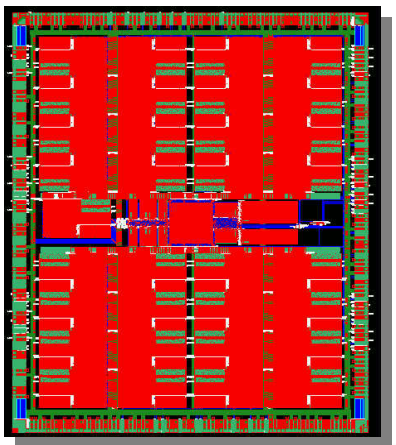


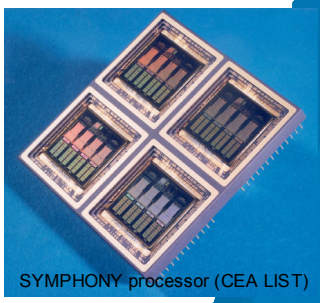
Reconfigurable component

Source: R. David, S. Pillement and O. Sentieys– Low-Power Electronic Design, chapter 20: Low-Power Reconfigurable Processors. CRC Press edited by C. Pillet



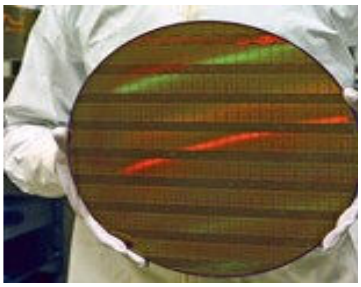
CELL processor

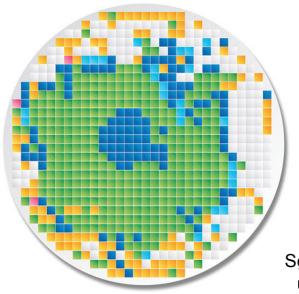


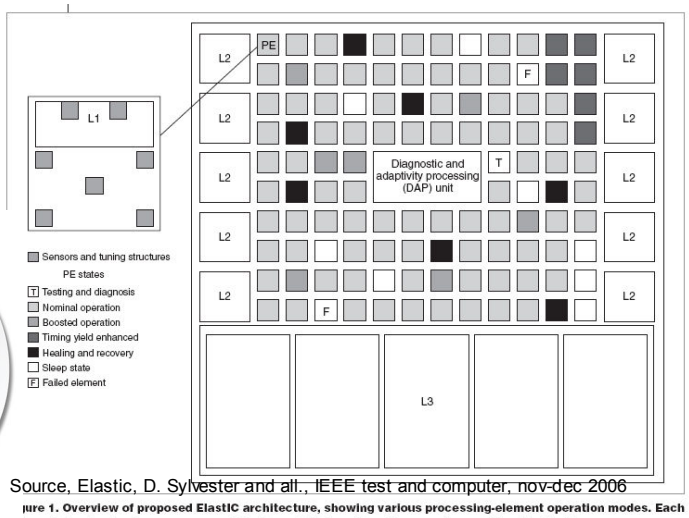


SYMPHONY processor (CEA LIST)

Reliability aware architecture





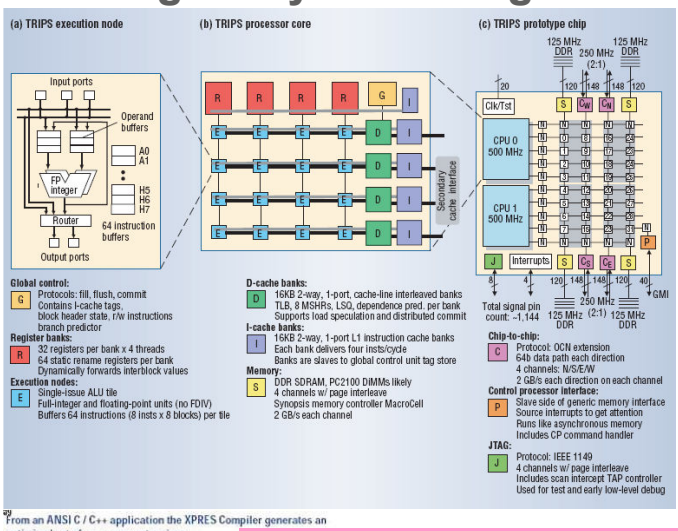


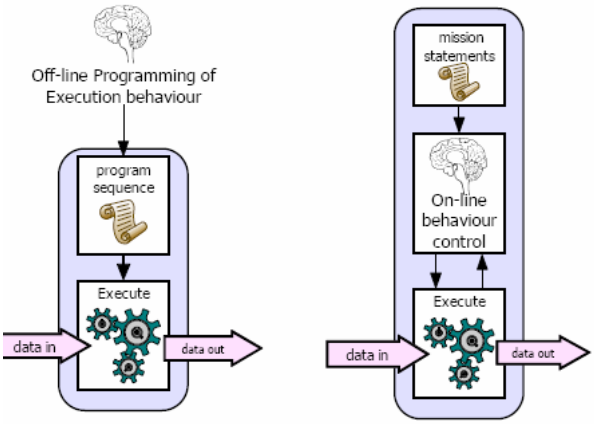
Source, Elastic, D. Sylvester and all., IEEE test and computer, nov-dec 2006

ıure 1. Overview of proposed ElastIC architecture, showing various processing-element operation modes. Each PE consists of a simple processor architecture with dynamic voltage scaling and tunable flip-flops.

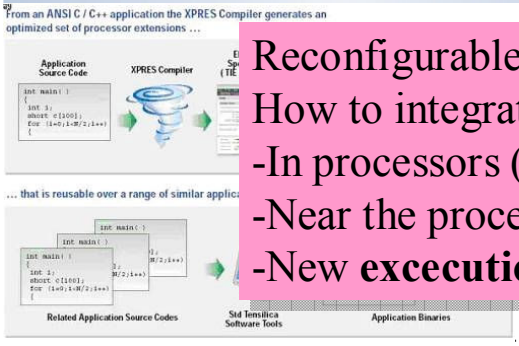
Due to randomness of the technology, the cost depend more on the yield rather than the area.
Design for reliabilty at the architecture level

Heterogeneity inside regular component





Courtesy, C. Gamrat and all Aether project



Reconfigurable techniques allow the heterogeneity.
How to integrate these reconfigurables modules?
-In processors (Tensilica)?
-Near the processor (Adres, TRIPS)?
-New **excecution model and processor** (SANE) ?

How to propose new architectures?

Appli. SW 1 | **Appli. SW 2** | **Appli. SW 3** | **Appli. SW 4** | **Appli. SW 5** | **Appli. SW n**

1. Defin odel
2. Defin g model
2. Defin itecture
able t n model

MPSoC

Processor 3	**Mem**	**Processor 2**
RPU	**IP**	**Processor 1**

(Unreliable) Technology platform

Definition of the Execution Model

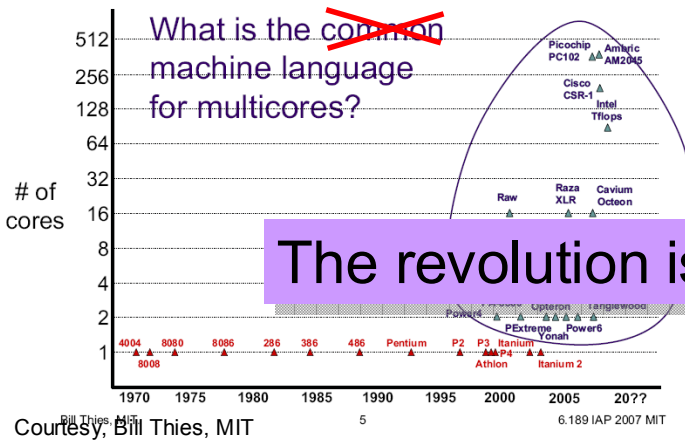
- **Not only one generic Execution Model : depends on the characteristics of the target applications in term of capabilities of :**
  - ✓ Computation,
  - ✓ Communication,
  - ✓ Memorization,
  - ✓ Control,
  - ✓ I/O,
  - ✓ Real time,
  - ✓ Safety and security,
  - ✓ Debug, etc…

- **Must include the architectural concepts (regularity, reconfigurable computing, reliability, etc…)**
- **This model give the a "reference manual" for the tool design and architecture design**

Definition of the programming model

- **Bring to C, or other sequential programming language, capabilities to express the needed parallelism to support the selected execution model**
- **Graph relevant for parallelism expression**
- **Think parallel !**

Why a New Language?



Courtesy, Bill Thies, MIT

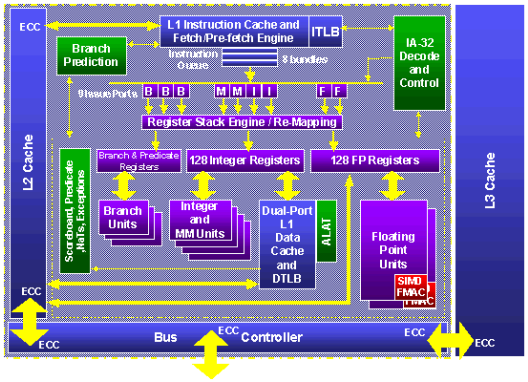
*Multicore systems-on-chip will force designers to "rethink computer architectures in a most fundamental way," said Anant Agarwal, professor at the Massachusetts Institute of Technology (MIT) and a keynote speaker at the Multicore Expo here Tuesday (March 27). Agarwal discussed how multicore technology will impact the way designers size resources and connect cores, and proposed a **new multicore programming approach**.*

Times (March 2007)

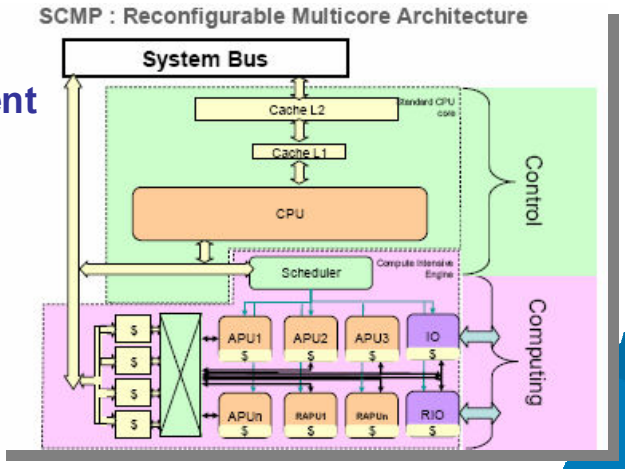
The revolution is moving !

Definition of the architecture

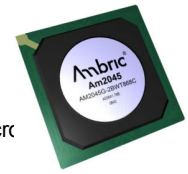
- **Bring resources inside the component**
  - ✓ Control & management
  - ✓ Computing
  - ✓ Memory
  - ✓ Communication
  - ✓ I/O



- **How to organise the component to be conform to the EM ?**
  - ✓ Processing
  - ✓ Interconnection
  - ✓ Memorisation
  - ✓ I/O



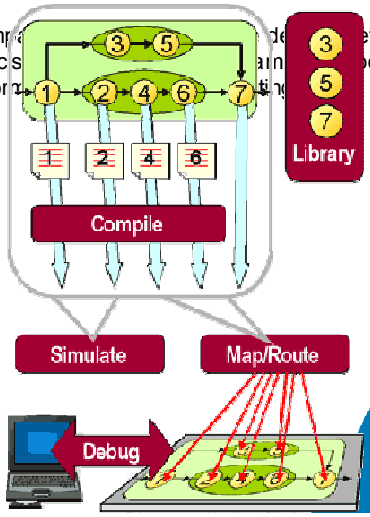
Ambric example



Ambric introduced its teraOPS-class Am2000 family of reconfigurable processing arrays (RPAs) at In-Stat's Fall Micro Forum in October, '06.

The only way to continue to deliver significantly higher levels of performance with power efficiency now and in the long run is by massive parallelism. Our solution to the architectural and programming challenges of massive parallelism clears the way to its practical adoption. The key to a practical solution for embedded computing is a relentless focus on the right **programming model first**; then Ambric **invented new hardware architectures and circuit designs to enable this programming model**.

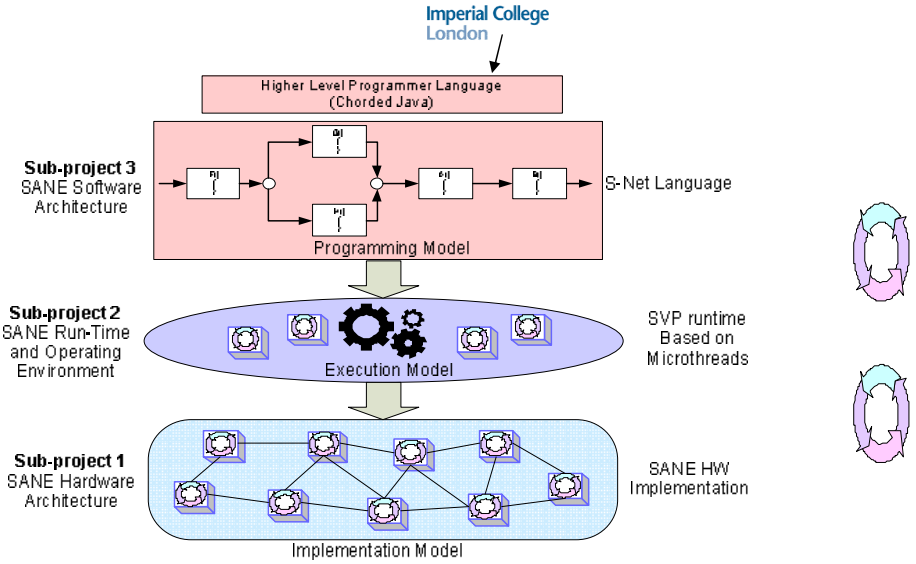
The Am2000 family of RPAs offers a profoundly easier development method comp… …ethods or the nightmarish synchronization problems of programming multiple-DSPs. Ambric's … …odel (SOPM) is the key that unlocks engineering productivity and quality for high-perfor… …ti…



Source, www.ambric.com

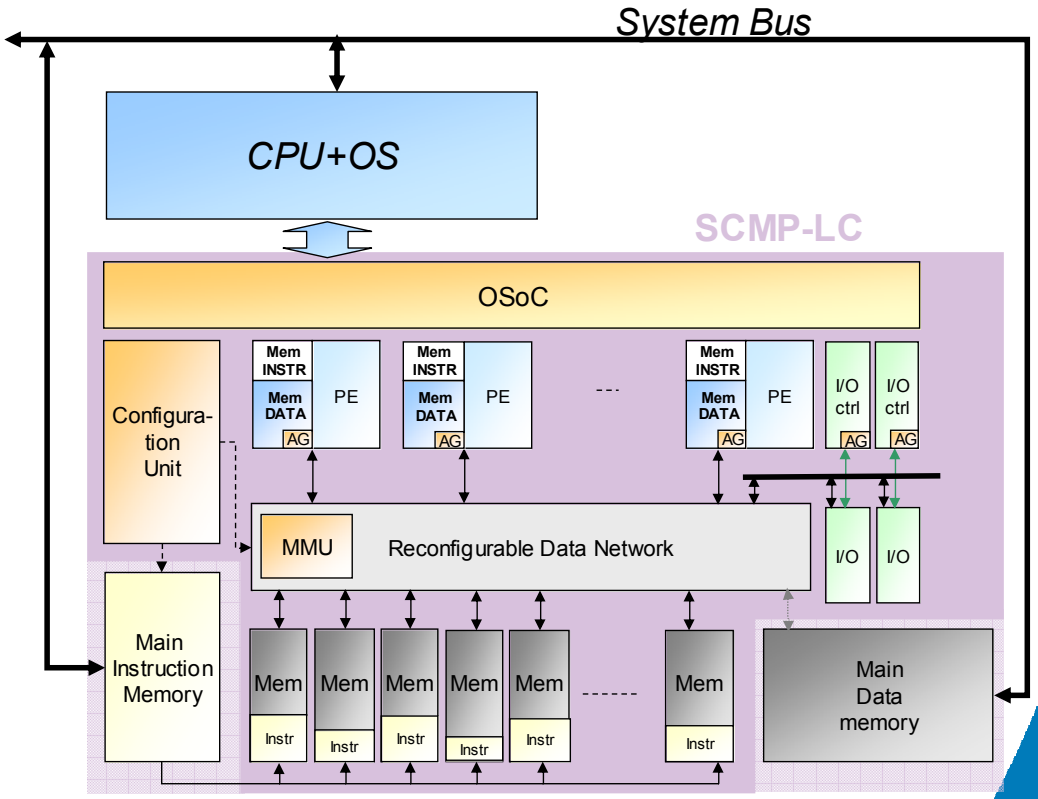
Dataflow execution model and programming model.
Specific reconfigurable NoC able to support this programming model.
Tools easier to develop.

Sane Architecture example (www.aether-ist.org)

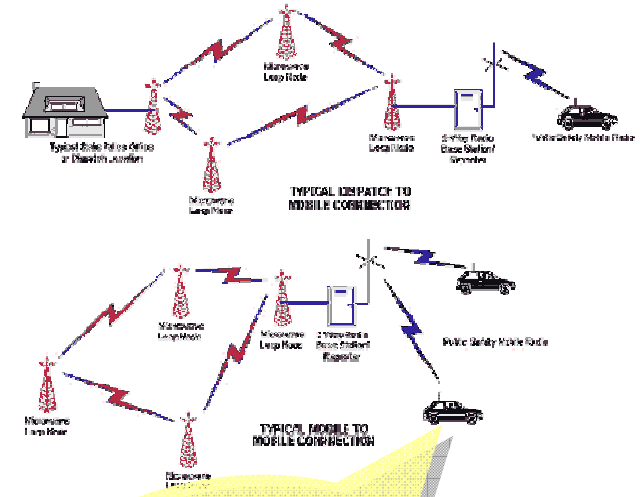


- **SANE provides an abstraction of self-adaptivity applicable at all levels of the AETHER framework**
- **The model allows for dynamic concurrency management thanks to the micro thread execution model**
- **A higher level programming environment allows for both boxes interfaces and interaction management (S-NET) and box behaviour programming (Chorded Java)**

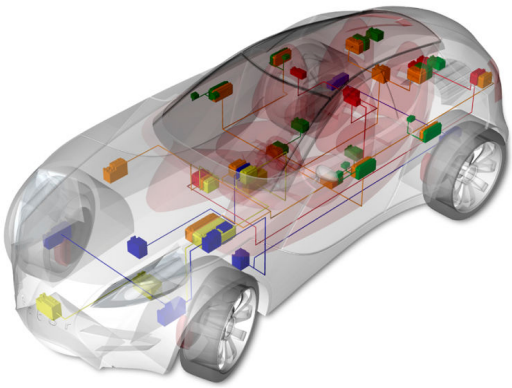
The SCMP-LC architecture example

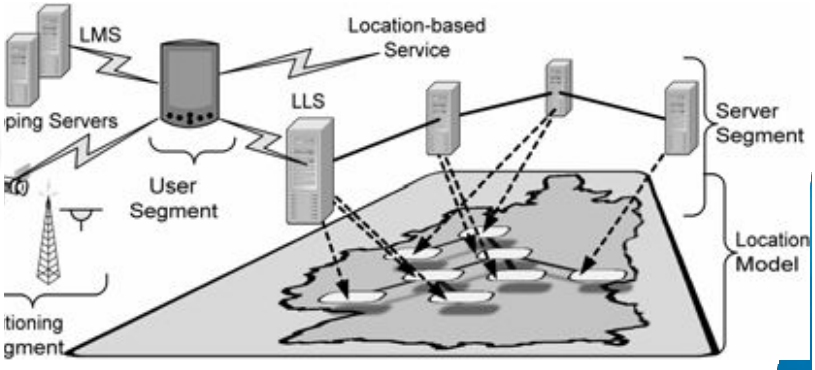


Not only the component, but think system



How to manage the whole system?

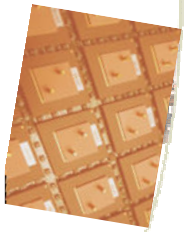




Courtesy, Thomas Hadig, Jörg Roth, '**ACCESSING LOCATION AND PROXIMITY INFORMATION IN A DECENTRALIZED ENVIRONMENT**'

Difference between limited system and open system.
New solutions could be proposed able to handle muti-component, on the fly reconfiguration, energy management, etc.

Toward performance, energy and reliability aware systems



THANK YOU !

Thierry Collette
Thierry.collette@cea.fr