iNoC: An innovative EDA flow for on-chip communication infrastructure

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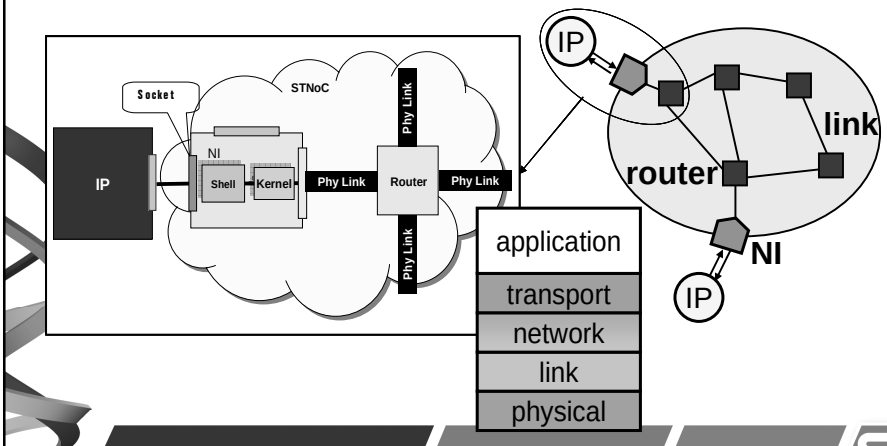
MPSoC 07

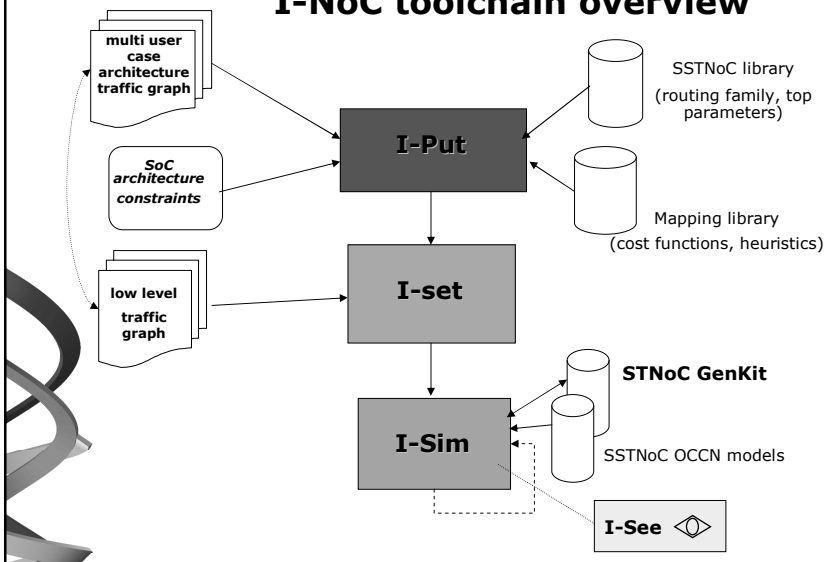
2007
1987
20 years dedicated to the future

S-STNoC at a glance

Spidergon STNoC is a set of **Network Interfaces (NI)** (layer 4), **on-chip routers** (layers 2,3) and **physical links** (layer 1)



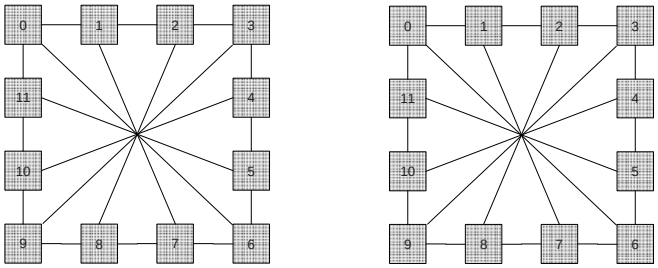
I-NoC toolchain overview



I-Put
mapping application onto Spidergon

I-Put: metrics validation

Worst mapping vs. Best Mapping

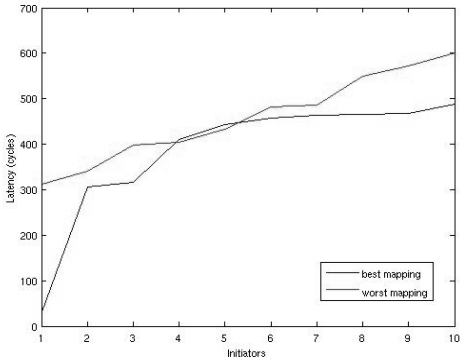


Use case description:

10 Initiators (decoder), 2 Memory slaves, uniform traffic to the targets, LRU arbitration scheme, high traffic, flit size 64, 250Mhz of interconnect freq

I-Put: max latency results

- The graph shows how max latencies obtained by simulation of the user case with best mapping are smaller than the same user case with the worst mapping



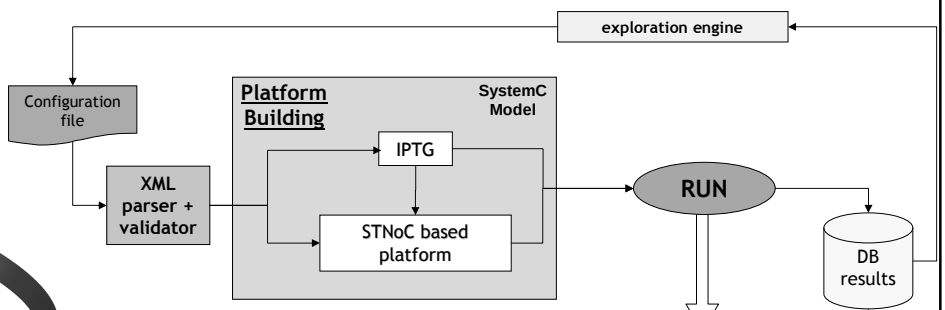
I-Set
system parameters settings

I-Set

- The goal of this tool is to set (or give a suggestion to the user on how to set) several system parameters performances/cost relevant like network interface buffers size and quality of service features
- The output is another file with a set of possible system configuration, ready to run on I-Sim

I-Sim
simulator

I-Sim



Overview picture of the framework

I-See
architectural debugger

I-See: the architectural debugger

Run time remote monitor for I-Sim (but non only!)

- it acts like a sort of « architecture debugger »

Who	How	What
SW developer	debugger	Monitor/interact (register values,…) with run time program execution
SSTNoC SoC architect	I-see	Monitor/interact (architectural parameters) with SSTNoC simulation

Run time **remote** monitor

- ~~user access through the network (client/server architecture)~~

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……Thank you for listening!!!