Ultra-Low Power? Think Multi-ASIP SoC!

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Ultra-low power SoC design

ITRS Roadmap

Table 6b Power Supply and Power Dissipation—Long-term Years

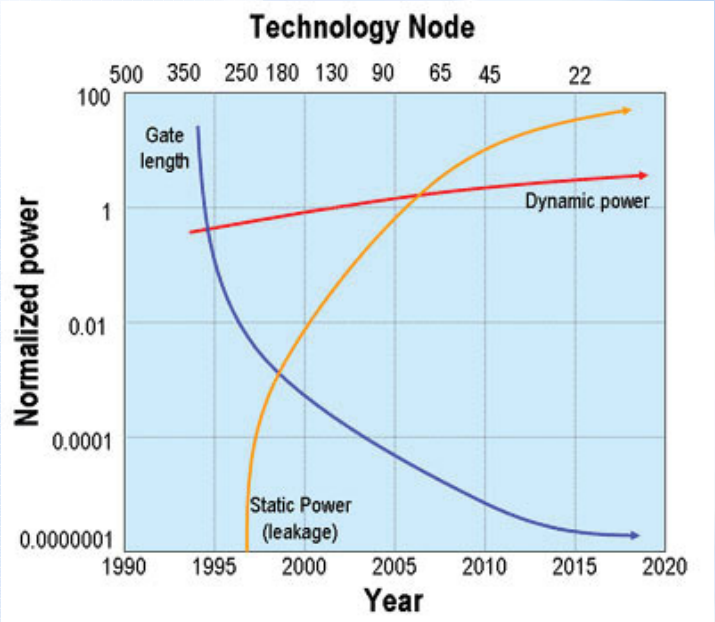
Year of Production	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
Technology Node	*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	**54**	**42**	**38**	**30**	**27**	**21**
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	**45**	**35**	**32**	**25**	**22**	**18**
MPU Printed Gate Length (nm) ††	**25**	**20**	**18**	**14**	**13**	**10**
MPU Physical Gate Length (nm)	**18**	**14**	**13**	**10**	**9**	**7**
Power Supply Voltage (V)						
Vdd (high-performance)	**1.0**	**0.9**	**0.9**	**0.8**	**0.8**	**0.7**
Vdd (Low Operating Power, high Vdd transistors)	**0.7**	**0.7**	**0.6**	**0.6**	**0.5**	**0.5**
Allowable Maximum Power [1]						
High-performance with heatsink (W)	**218**	**240**	**251**	**270**	**288**	**300**
Cost-performance (W)	**120**	**131**	**138**	**148**	**158**	**168**
Battery (W)—(hand-held)	**2.8**	**3.0**	**3.0**	**3.0**	**3.0**	**3.0**

[1] Power will be limited more by system level cooling and test constraints than packaging

[ITRS Roadmap 2003]

- Power budget (Watts) more or less constant, while chip complexity increases

Ultra-low power SoC design



["Moore's Law Meets Static Power", Computer, December 2003, IEEE Computer Society]

Dynamic power

$$P_{dyn} = C \times (A \times f_{clock}) \times V_{dd}^2$$

- Low-voltage technology, voltage scaling
- Concurrency: task-, data-, instruction-level parallelism
- Avoid unnecessary switching: clock gating, operand isolation…

Leakage power

$$P_{leak} = I_{leak} \times V_{dd}$$
$$\sim (a^{-Vt} \times N_{gates} \times W_{dev}) \times V_{dd}$$

- Multi-threshold cell libraries
- Power gating
- Minimal logic (application-specific)

Ultra-low power SoC design

Holistic approach

- **Ho·lis·tic** ***adj***

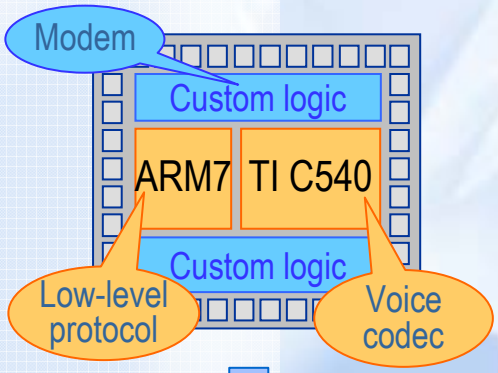
  " Emphasising the importance of the whole and the interdependence of its parts "

- Design phases considered
  - System architecture
  - Processor (ASIP) architecture
  - Logic level

System architecture

System-on-Chip becomes Sea-of-Cores

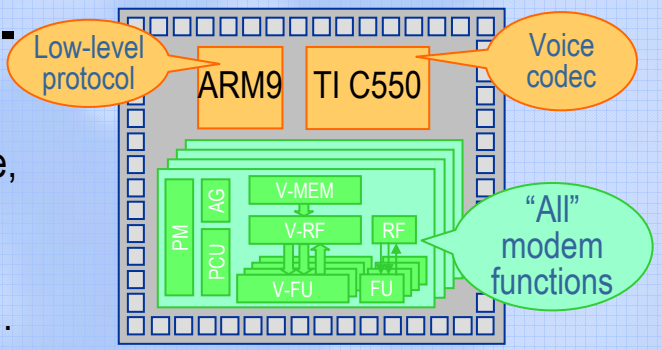
2000
2G baseband chip



2005 ~ 2010
≥ 3G baseband & radio chip
Multi-standard, SDR

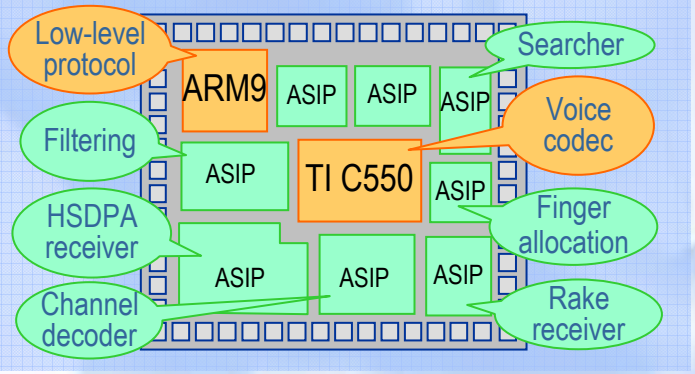
Homogeneous, multi general-purpose processors

- VLIW/SIMD: NXP (EVP), Sandbridge, Atmel (Diopsis)…
- Array processor: Morpho, IMEC…
- Processor arrays: PicoChip, Cradle…



Heterogeneous, multi-ASIP

- Configurable IP vendors: Tensilica, ARC, SiliconHive…
- **EDA vendors: Target**, CoWare, ASIP Solutions…



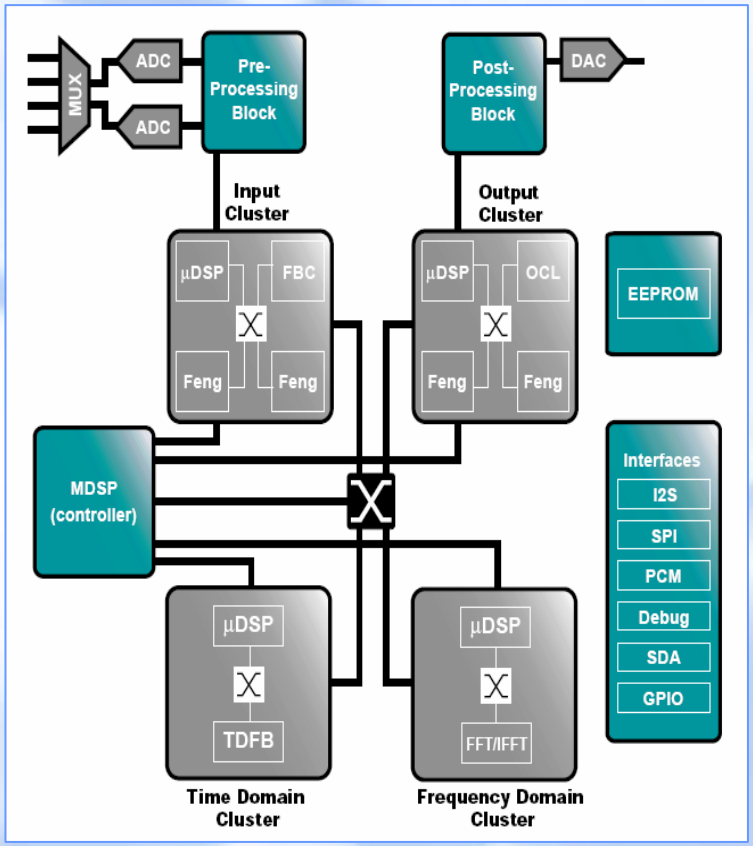
Heterogeneous best for deep submicron power challenge!

- Each ASIP optimised for its function: minimal logic, balanced parallelism
- Well suited for power gating based on system requirements

System architecture

Example: Gennum's Voyageur platform

- Used in hearing instruments and Bluetooth headsets
- Processor cores designed with Target's tool suite
- Multi-core
  - Microprocessor core
  - 4 "µ DSP" VLIW cores
  - 4 filter accelerators
- 0.04 mW/M-MAC, 42 MIPS at f_{clock} = 2 MHz (0.13µ CMOS)



Courtesy of Gennum Corporation

ASIP architecture

Concurrency

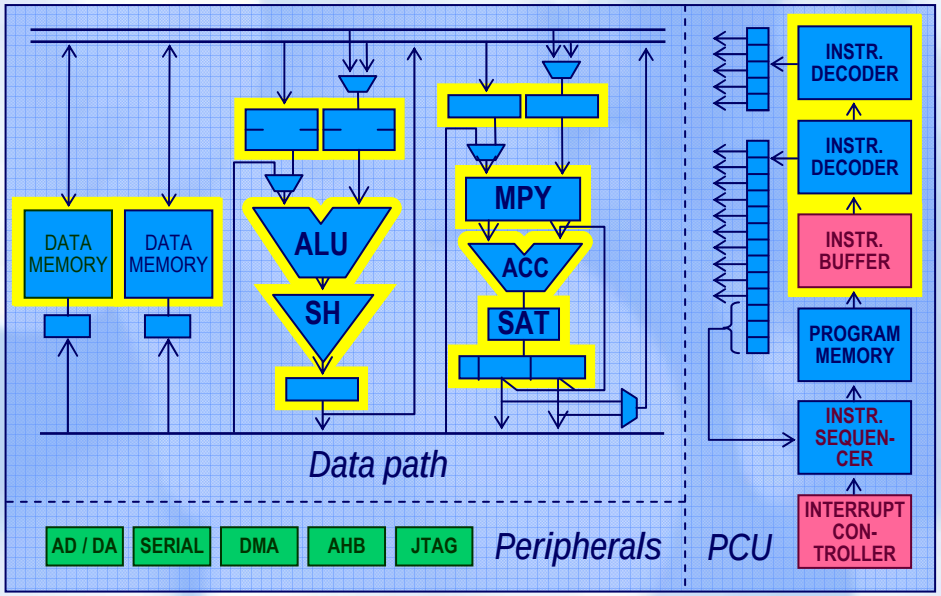
- Instr.-level parallelism (VLIW or encoded)
- Data-level parallelism (SIMD)

Reduced memory access

- Memory hierarchy: data & instr. caches, loop buffer
- Distributed reg. architecture
- Encoded instruction set

Arch. specialisation

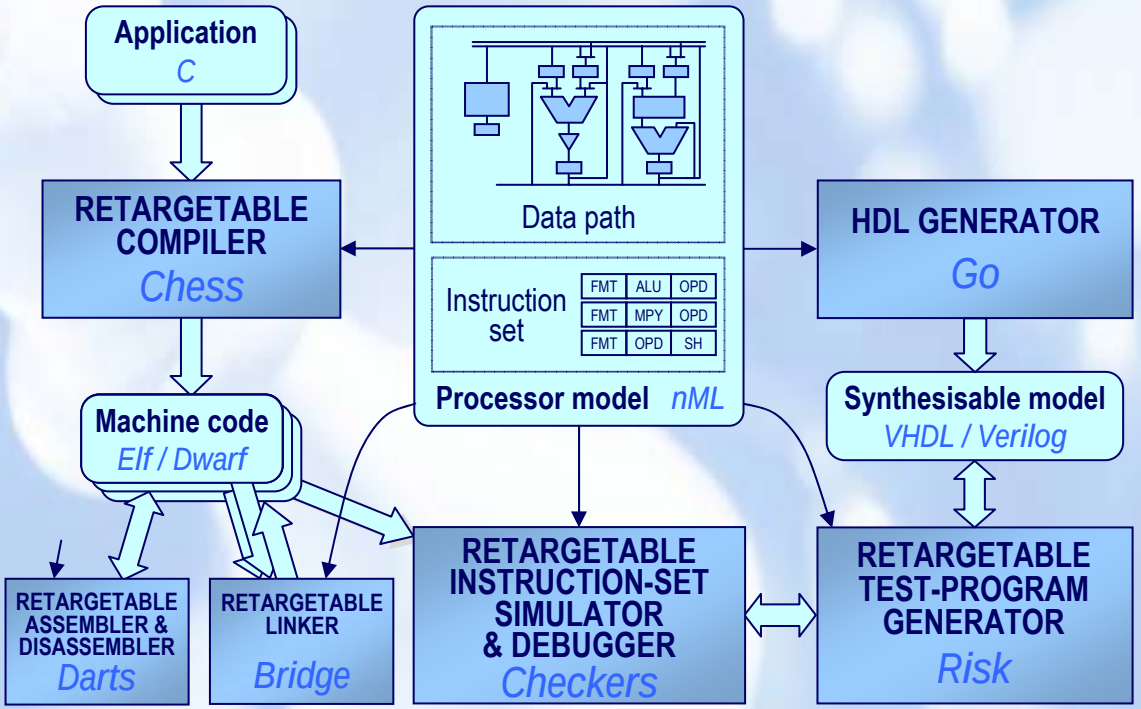
- App.-specific data types
- App.-specific functional units and instructions
- Balanced pipeline



→ Optimise beyond the limitations of configurable processor templates!

ASIP architecture

- True architectural exploration enabled by retargetable tool suite – *"Chess/Checkers"*

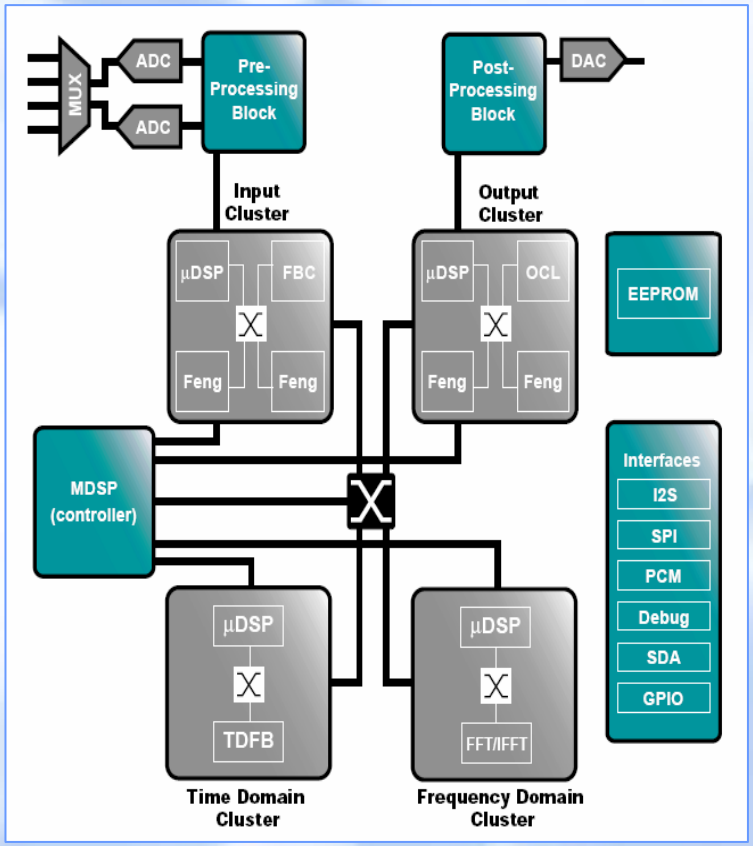


- Optimisation beyond reconfigurable processor templates
- Fast path to logic synthesis allows for accurate power estimations

ASIP architecture

Example: Gennum's Voyageur platform

- 0.04 mW/M-MAC,
  42 MIPS at f_{clock} = 2 MHz
  (0.13µ CMOS)



- µ DSP and filter engines:
  20-bit precision
- µ DSP: VLIW with dual MAC
- Filter accelerators:
  same algorithm consumes 4x less power than on µ DSP

Courtesy of Gennum Corporation

Logic level

- HDL generator adds logic to avoid unnecessary switching
  - Selective clock gating
  - Selective operand isolation
  - Latching of register file addresses in instruction decoder
- Example: audio DSP (90 nm technology, 200 MHz)

Design step	Power	Area
Go - Without low power options	91 µW/MHz	
Go - Clock gating and operand isolation for FUs	57 µW/MHz (-37%)	
Go - Operand isolation for muxes	44 µW/MHz (-23%)	
Go - Register addresses from decoder	36 µW/MHz (-18%)	36.9 kGates
Manual HDL design by low-power specialist	32 µW/MHz (-11%)	36.6 kGates (-1%)

Conclusions

- **Heterogeneous multi-ASIP SoCs best meet deep-submicron power challenge**
  - Optimally balanced task / data / instruction-level parallelism → reduce dynamic power
  - Minimal logic, power gating → reduce leakage power
- **Key is retargetable tool suite for efficient ASIP design**
  - Enables true architectural exploration, beyond configurable processor templates
  - Provides unified and efficient software development environment
- **Fast and efficient path to logic implementation**
  - Includes logic-level power optimisations
  - Enables fast and accurate power estimations