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Multiobjective Design Space Exploration of MPSOC with Direct Execution

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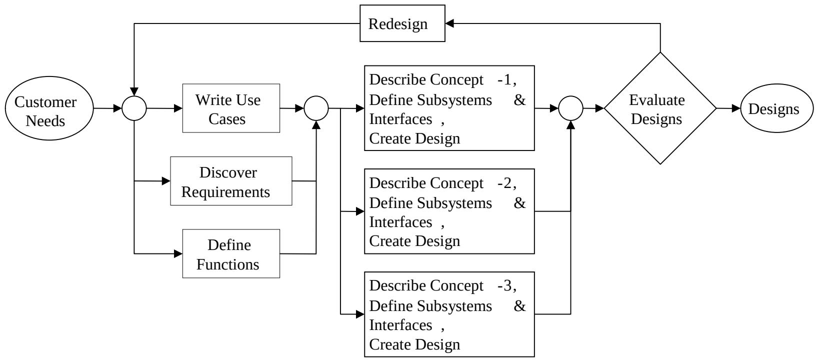
Outline

- Motivations
- System Design is NP-complete
- MPSOC automatic exploration flow with direct execution
- NOCDEX: NOC Design Space Exploration with direct execution
- Perspectives
- Conclusion

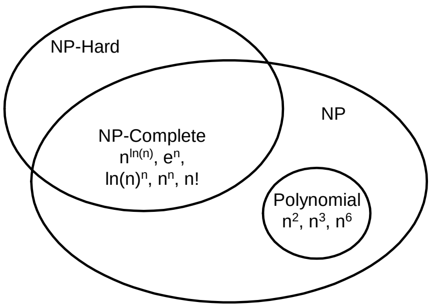
System Design Process



Source T.Bahill

Heterogeneous Systems built on parametrizable components

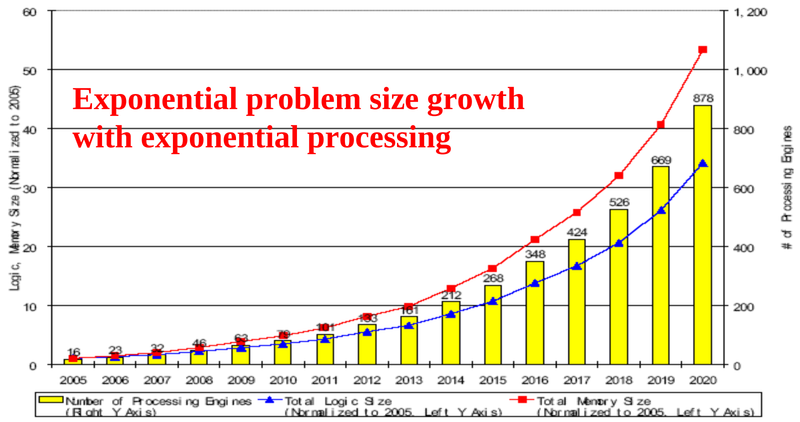
Theoretical Complexity



- System Design Problem equivalent to Knapsack Problem
- The Knapsack Problem is NP-complete.[Karp 72]
- Therefore the System Design Problem is NP-complete.
- No polynomial time algorithm for solving the problem: large search space

W.L. Chapman, J. Rozenblit, and A.T. Bahill, "System design is an NP-complete problem," ***Systems Engineering, The Journal of INCOSE*****, 4(3), 222-229, 2001.**

System Design is NP-Complete and the trend makes it worse



SOC-PE Design Complexity Trends

Source ITRS 2006

ad-hoc/manual MPSOC Design techniques do not match coming large design space

Motivations

- Deep-submicron design challenges (interconnect delay vs gate delay,increased uncertainty with process scaling,increased power constraints,clock skew and jitter,GALS)
- Tuning soft IPs for performance and area (multiobjective) with DSM constraints
- System level (TLM SystemC) simulation provide large improvement in simulation time, but design automation still decoupled with real physical implementation constraints (DSM)

EDA Tools:

- do not allow combined architecture and physical implementations analysis
- do not provide automatic multiobjective design space exploration help
- simulation based

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Design Space Exploration Optimization Techniques

- General optimization techniques
  - taboo search
  - simulated annealing
  - integer programming/linear programming
  - genetic algorithms and Evolutionary Algorithm (MOEA)
  - widely applied for various EDA problems

- Multiobjective Optimization techniques applied to DSE
  - Strength Pareto Evolutionary Algorithm (SPEA-2) (e.g.DSP (Thiele), VLIW [PaCa04])
  - Non-dominated Sorting Genetic Algorithm (NSGA-II) (e.g. LEON-2 [GhHa04])

We need automatic physical aware multiobjective optimization (perf/area/energy) techniques to reduce the design space combined with fast configuration evaluation

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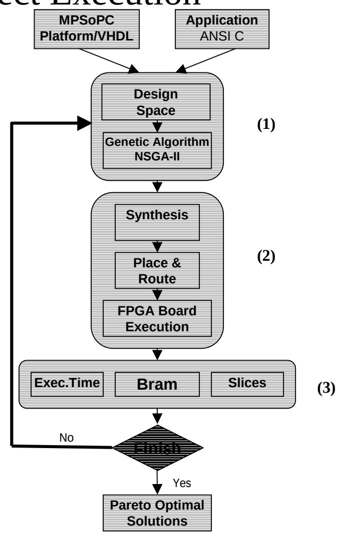
Application-specific MPSOC Automatic Exploration Flow with Direct Execution

- Inputs Step 1 are :
  - Platform architecture described in VHDL
  - C Application running on embedded soft IP processors
  - parameters
  - Number of individuals and generations
  - Feedback form Synthesis and "Place and Route" execution (Nbr BRAM, occupied slices, performance in cycles count)
- Inputs Step 2 are :
  - Individuals (different platform architecture) for synthesis and target FPGA downloadable bitstream generation
- Inputs Step 3 are :
  - Synthesis and "Place and Route" files, Performance in term of cycles



Design Space Exploration Framework

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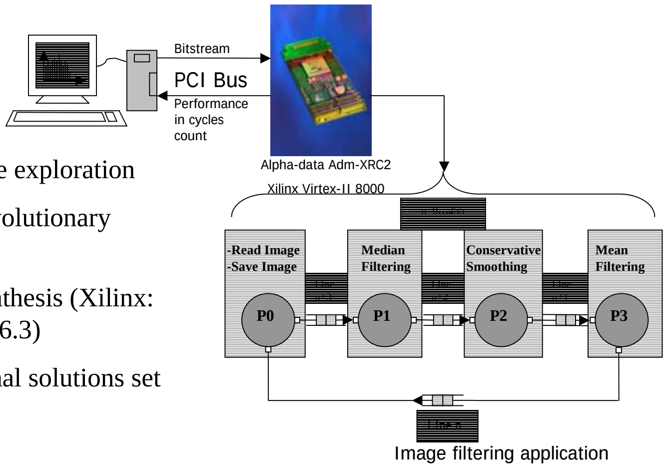
-Pentium 4 3.0 Ghz
-4 GBS main memory



-Design space exploration

-NSGA-II Evolutionary Algorithm

-Platform synthesis (Xilinx: EDK6.3, ISE6.3)

-Pareto optimal solutions set

Case study: MPSOC platform description

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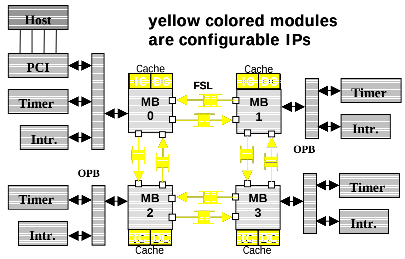
- 2x2 mesh topology MPSOC (Xilinx Microblaze)
- Instruction and data cache memory for each Microblaze
- Fast simplex link (FSL) based point to point communication scheme
- Software XY wormhole based routing algorithm
- On-chip peripheral bus for timer and interruption controller IPs



- Processor MB0 communicates with the host PC through a custom (User defined) PCI bus control IP
- 100Mhz constrained design synthesis

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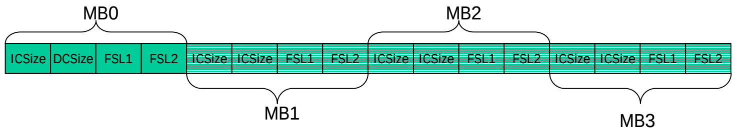
Design Space Exploration Parameters Specifications

- Embedded processor instruction and data cache sizes
- Communication FIFO sizes
- Easily extensible to other parameters
- 14,048,223,625,216

Multiprocessor Configurations

Procs	FSL1Out	FSL2Out	D-Cache	I-Cache
MB0	16..2048	16..2048	512..4096	512..4096
MB1	16..2048	16..2048	512..4096	512..4096
MB2	16..2048	16..2048	512..4096	512..4096
MB3	16..2048	16..2048	512..4096	512..4096

Exploration Chromosome



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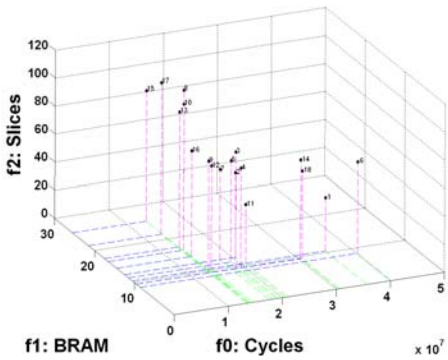
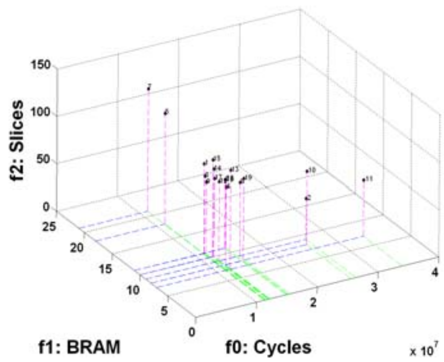
Exploration results : Pareto Optimal Solution front





Number of Generations : 10
Number of Individuals : 20
Number on individuals in 1st rank 18

Number of Generations : 14
Number of Individuals : 30
Number on individuals in 1st rank 19

Objective functions are:

FPGA Slices : To be minimized
BRAMs : To be minimized
Cycle Count : To be minimized

Simulation vs. Emulation

- 8 million gates Xilinx Virtex-II FPGA implementation
- Alpha-Data ADM-XRCII PMC development board
- Instantaneous gathering of performance results
- Exploration time improvement of:

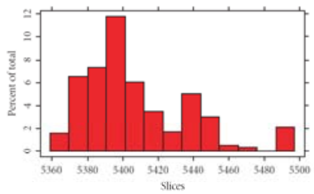
$$3.88\times10^{6}$$

EA(ms)	Indi. Gene.	190
	Obj Functions Eval.	293
	Selection	0.116
	Crossover	0.033
	Mutation	1.118
Synthesis (sec)	Synthesis	523.503
	P and R	655.174
	P/R & Bitgen	797.856
Execution	Exploration 60x30	
	Sim. VHDL PPR 64x64	2250 Days
	Direct Exec.256x256	1.39 hour

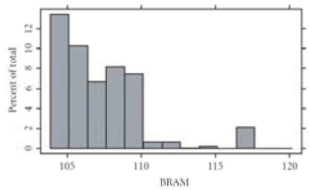
Cycle Accurate Simulation vs. Emulation

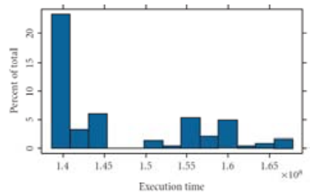
Beating The Simulation Wall Though Direct Execution

Statistical Analysis of Explored Space



Diversity of MPSOC configurations explored





Complexity of Explored Space

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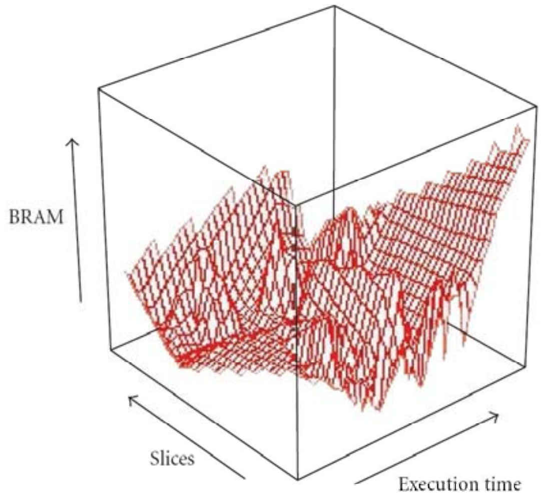

NOCDEX: NOC Design Space Exploration With Hardware Execution

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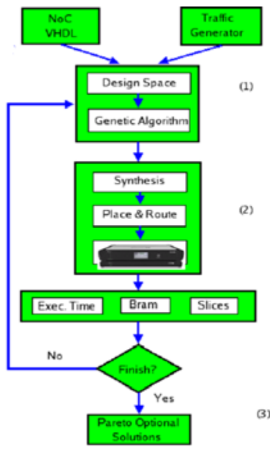

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Case Study: Arteris NOC Design Tools

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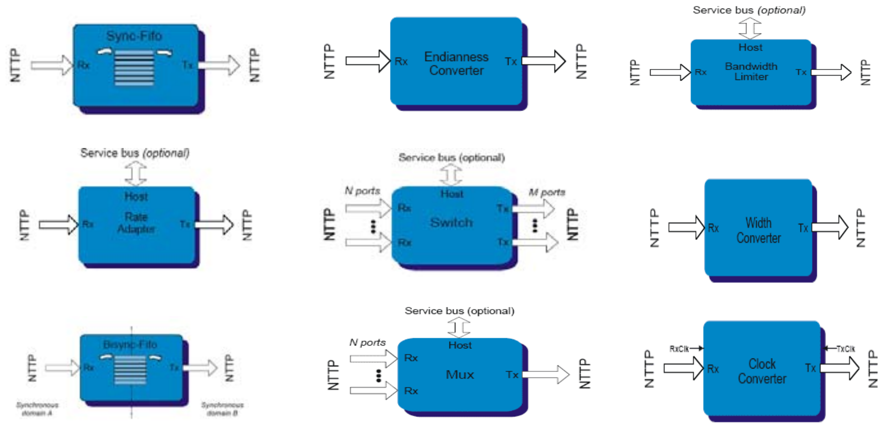
Arteris NOC Design Methodology
Danube 1.4 - Packet Transport unit



When to use which with which parameters ?

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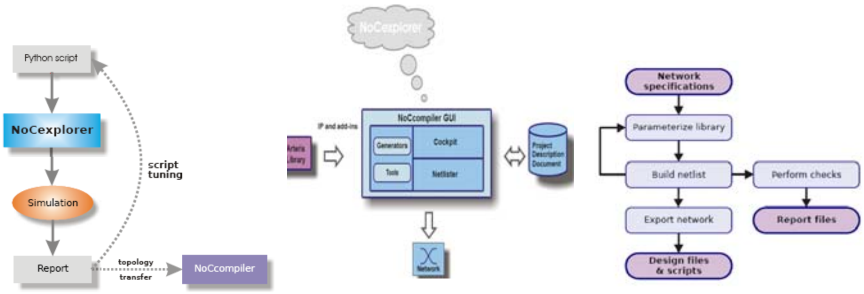
Tools for exploration



Arteris Switch options (128 possibilities)

Arbitration type	Round-Robin(0), LRU(1), Random(2), Fifo(3)
Input pipeline register	True(0), false(1)
Forwards pipeline register	True(0), false(1)
Backwards pipeline register	True(0), false(1)
Crossbar pipeline register	True(0), false(1)
Dual cycle arbitration	True(0), false(1)

What if we have N switches ?

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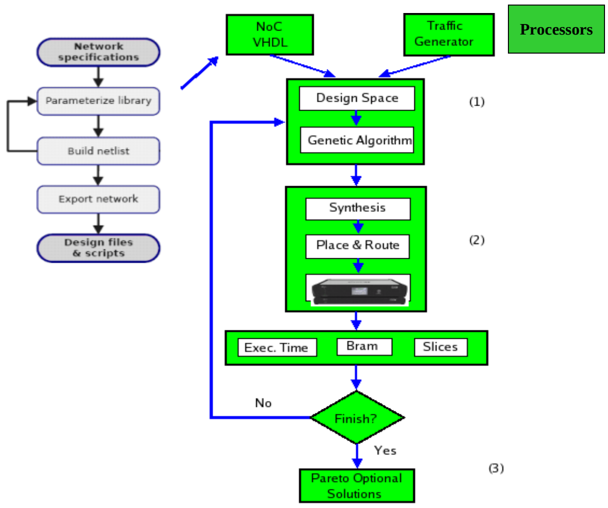
NOCDEX v1.0. :NOC Design Space Exploration With Hardware Execution on Arteris Tool



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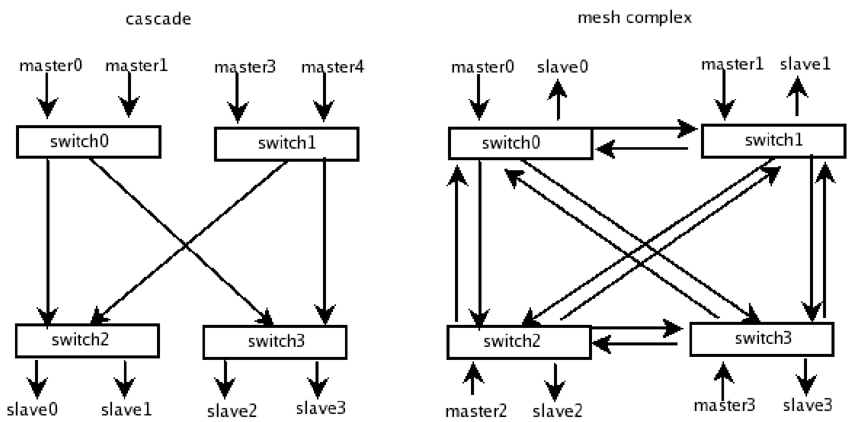
NoC case study



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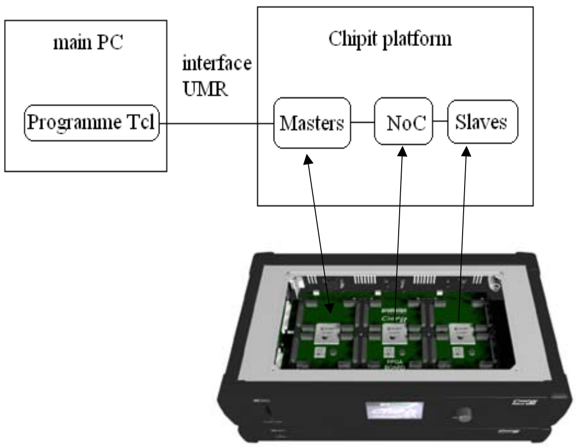
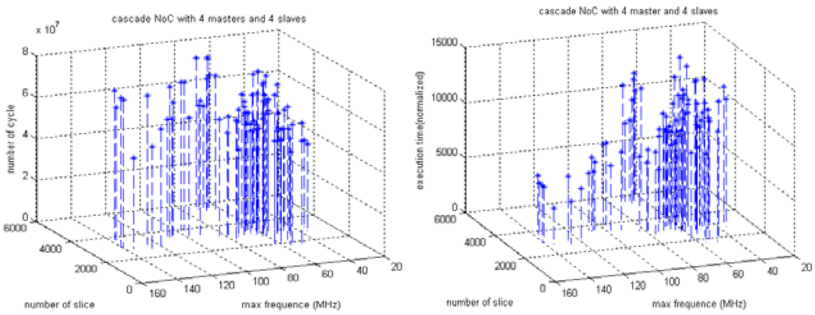
NOCDEX with ChipIt system



Results of NOCDEX: execution



Execution time not cycles (DSM) makes the difference

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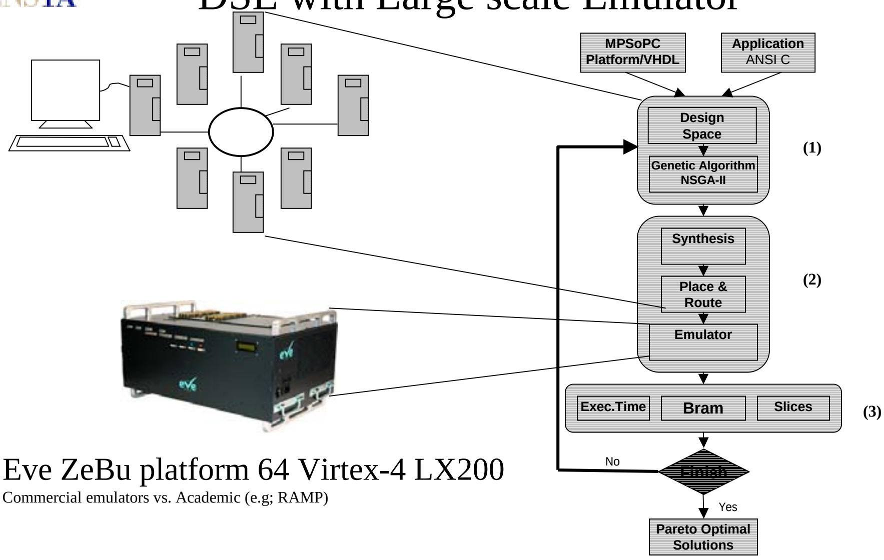
Perspectives
DSE with Large scale Emulator



Eve ZeBu platform 64 Virtex-4 LX200

Commercial emulators vs. Academic (e.g; RAMP)

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Conclusion

We propose a fully automatic tool for the multiobjective design space exploration (DSE) of soft IPs based MPSOC design:

Intelligent (non exhaustive or ad hoc) techniques for quickly exploring/pruning large design space

Exploiting the very large scale integration and the rapid reprogrammability of FPGA for real MPSoPC DSE

Beating MPSOC Simulation Wall Through FPGA direct execution

New Efficient NOC design space exploration –**NOCDEX**

Architecture design space exploration coupled with physical implementation constraints

Drastic improvement of Time-to-market

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Conclusion

- **Theoretical results:** we need more results on theoretical aspects of MPSOC design (theoretical complexity driven SLD)
- **Physical Aware:** we need an integrated methodology for MPSOC: **DFMM**

  Design **F**or **M**PSOC **M**anufacturability: many interesting research issues.
- **Parallel software:** we need Automatic Design Space Exploration of Parallel Software (concurrency semantics/formal transformations)

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Thank you

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