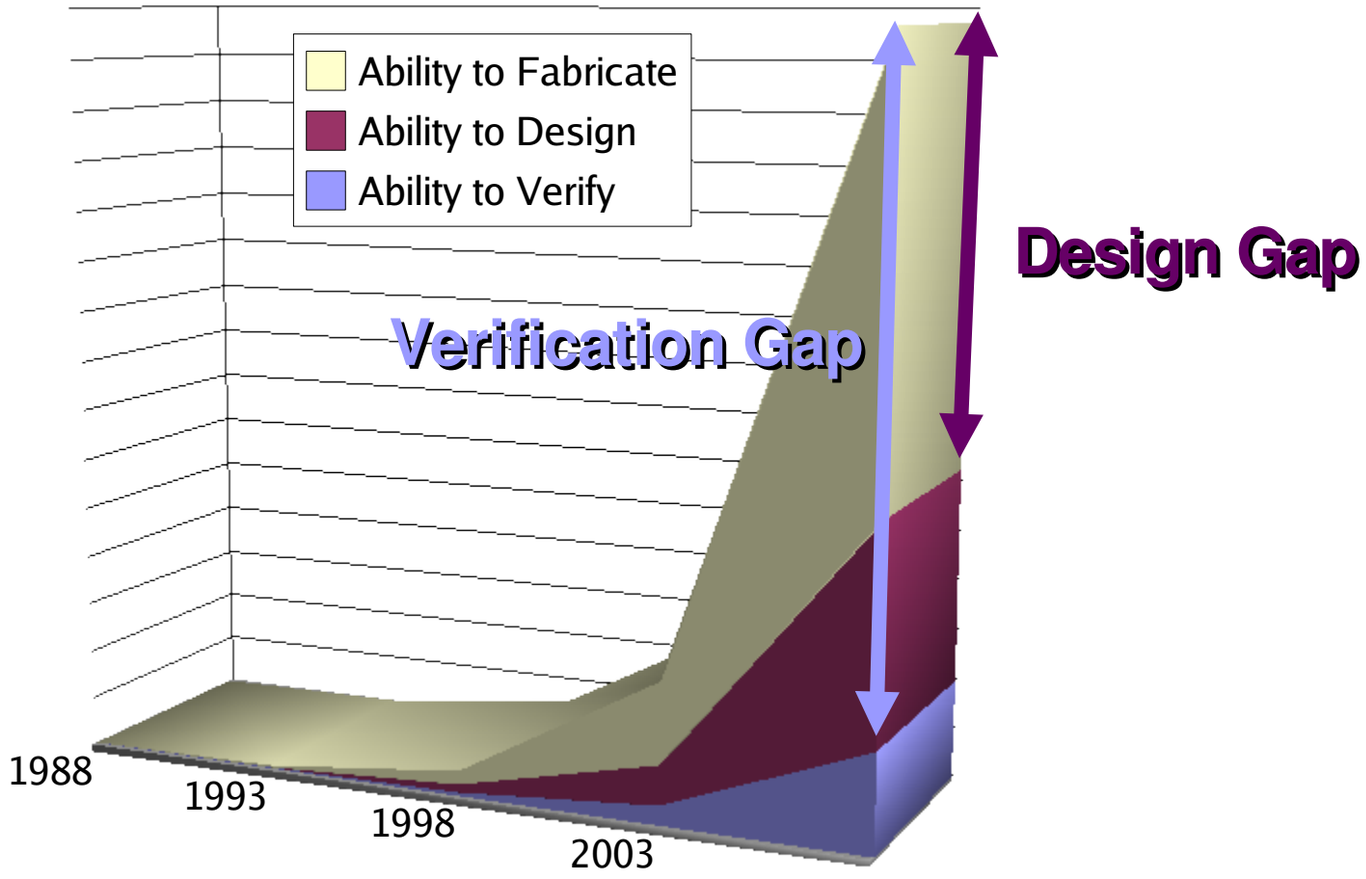
Functional Qualification

June 2007

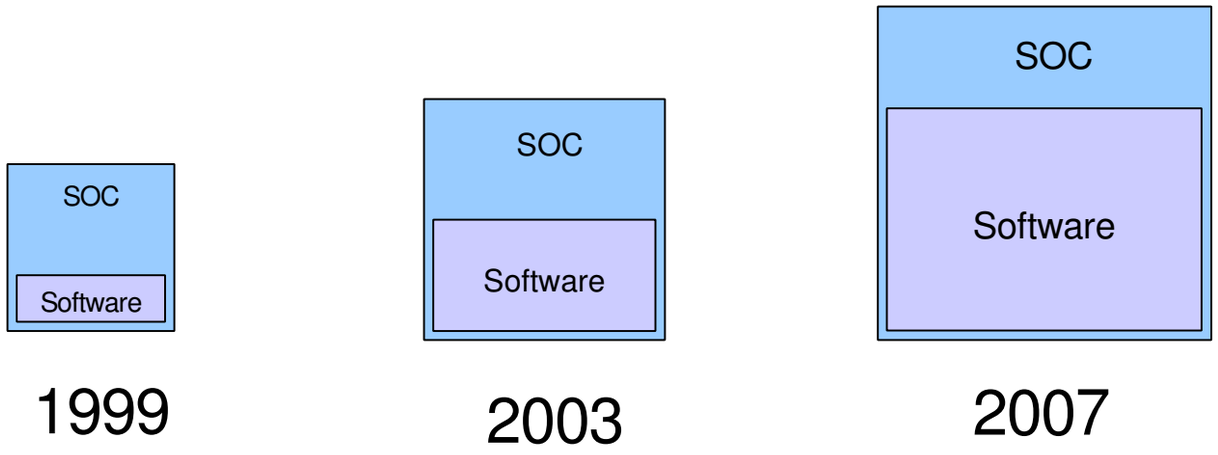
This problem is not going away



Functional verification is becoming more and more challenging

SoC

- "System on Chip" or "Software on Chip" ?
- Virtutech's Embedded Software Development Survey 2007
  - Quality was once again named the most worrisome aspect of respondents' current projects (28 percent), indicating that developers face more pressure than ever to produce high-quality products on time.

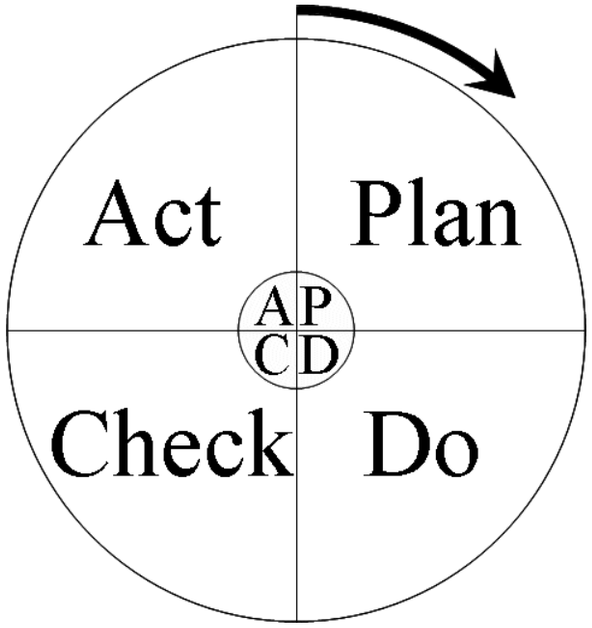


Quality = Profit

- **Moore's law calls for continual productivity gains**
- **Quality is now the bottleneck**
  - For both hardware and embedded software
  - Often consuming more resources than design
  - How to achieve “Re-use without Re-verification” ?
- **The EDA industry traditionally focused on productivity**
  - Design faster: schematic -> VHDL/Verilog -> SystemC
  - Verify faster: waveforms -> transactions -> HVL
- **Hardware & Software verification is seen as an “art”**
  - “*The Art of Verification with SystemVerilog Assertions*”, published 2006
  - “*The Art of Software Testing*”, Second Edition, 2006

Engineering vs. Art

- **Art cannot be measured – purely subjective**
- **Quality Management is a well known field**
  - Must be able to measure to manage improvement



Shewhart cycle (PDCA) for quality improvement.
made popular by W. Edwards Deming

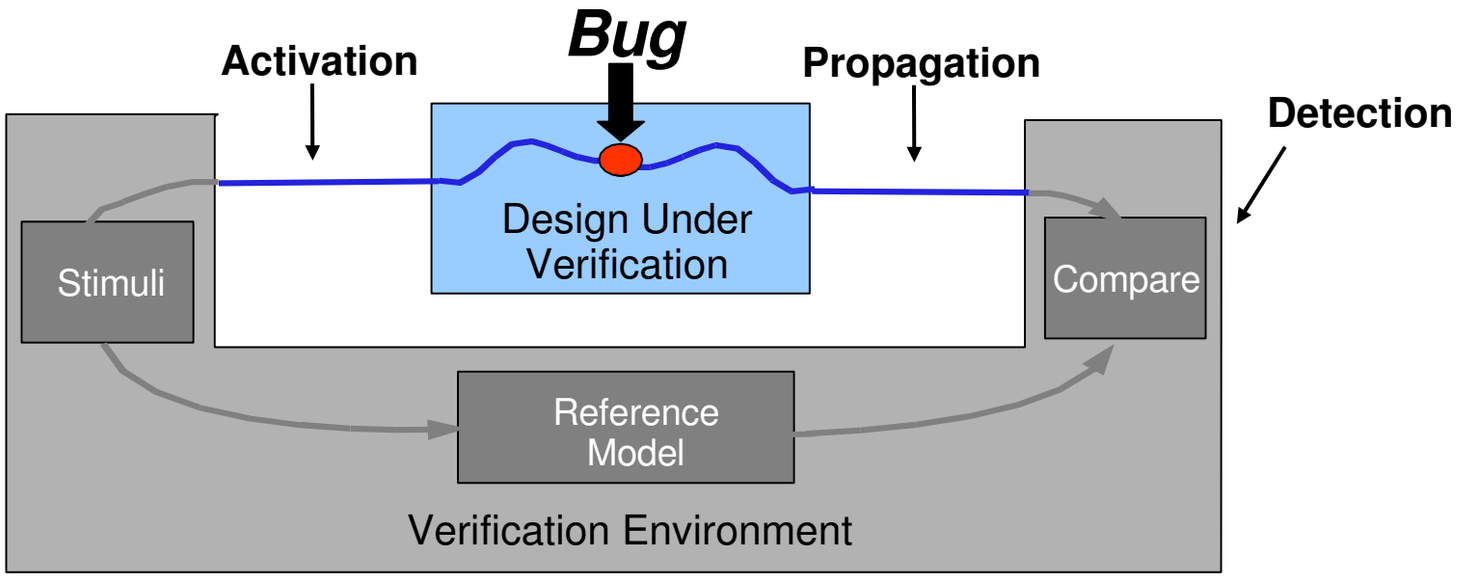
The philosophy is to keep improving the quality of an organization.
It is defined by four keys:

- Plan: Design or revise business process components to improve results
- Do: Implement the plan and measure its performance
- Check: Assess the measurements and report the results to decision makers
- Act: Decide on changes needed to improve the process

The Cost

- **No objective measure of the verification process means:**
  - Difficult to benchmark new methodologies
  - Verification engineers lack feedback on the quality of their work
  - Impossible to effectively Manage By Objective
- **Difficult to establish confidence in 3rd party IP**
  - Re-use often requires re-verification
- **Strategic opportunity lost**
  - Verification is a significant resource
  - More efficient use of this resource is a strategic advantage

Functional Verification Today



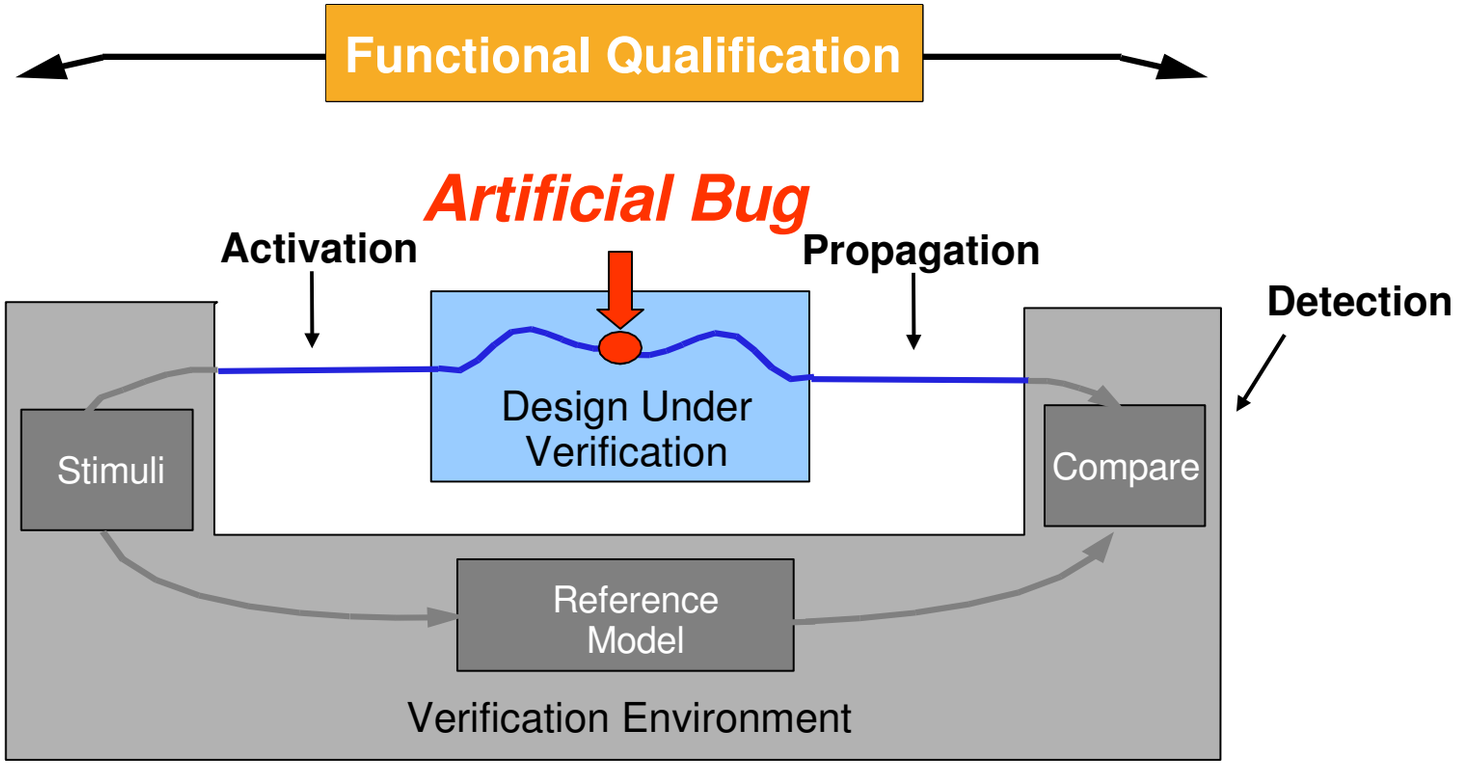
- The activation, propagation and detection phases must occur
- If there was a bug in the design, would you find it ?

Introducing Functional Qualification

➔ **Functional qualification is the ability to certify that "*if there was a bug in the design, it would be found*"**

- Provides the feedback needed to objectively evaluate functional verification environments
- Qualification is to verification what verification is to the design: the feedback tool needed to measure and improve the process

Introducing Certitude



Certitude injects artificial bugs in the design and measures the ability of the verification to detect them

Thank you