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MPSoC Approaches for Low-power Embedded Soc's

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Outline

- Approaches for Embedded MPSoC
- SH-MobileG1 : AP+BB Onechip
- SH-X3: SuperH SH-4A Quad-Core
- EXREAL Platform: Solution Platform for MPSoC
- Conclusion

Approaches for Embedded MPSoC

Embedded MPSoC

Application Specific : Optimized for the embedded systems
Low Power: Less than 5W, Less than 1W
Embedded Software: Optimized HW/SW for the embedded system

(1)Heterogeneous AMP : Integration of subsystems

SH-MobileG1 : One chip integration of Application & BB

(2) Homogeneous AMP : Hetero-OS / Homo-OS

SH-X3 : SuperH core for Multi-processor

(3) Homogeneous SMP : SMP OS

SH-X3 : SuperH core for Multi-processor

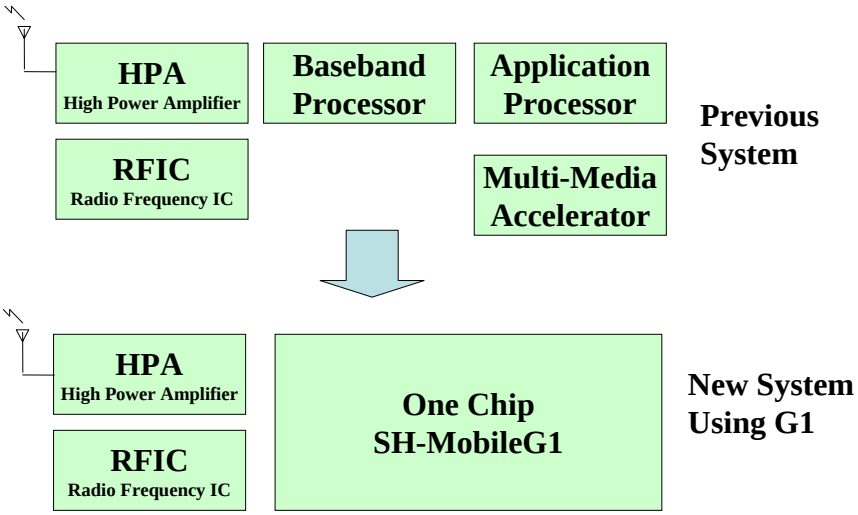
(4) Automatic Parallelizing Compiler

SH-X3 : SuperH core for Multi-processor

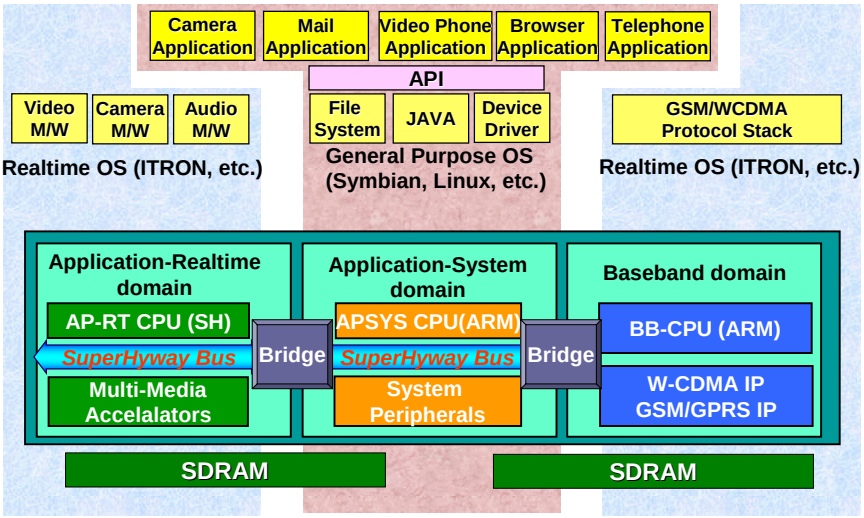
SH-MobileG1: AP+BB Onechip

ref: T. Hattori, et. al., "A power management scheme controlling 20 power domains for a single chip mobile processor." ISSCC Dig. Tech. pp.542-543, Feb 2006
M. Ito, et. al., "SH-MobileG1: A Single-Chip Application and Dual-mode Baseband Processor.", HOTCHIPS 18, Aug 2006

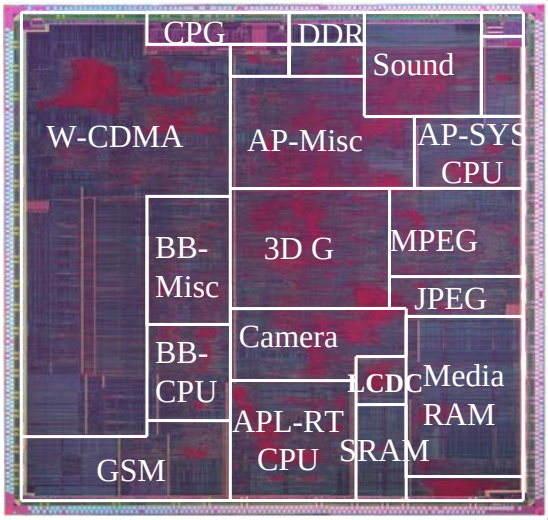
3G Multi-Media Cellular Phone System



A Sample of System Architecture using G1

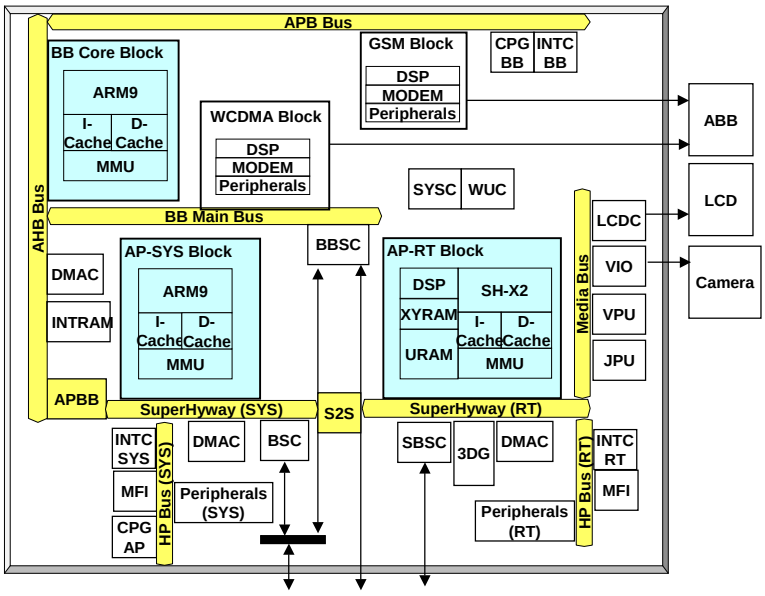


SH-MobileG1: Chip Overview



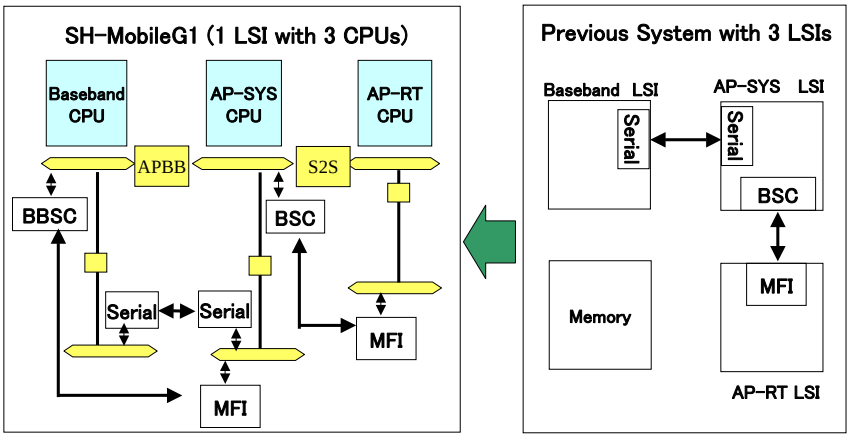
Die size	11.15mm x 11.15mm
Process	90nm LP 8M(7Cu+1Al) CMOS dual-Vth
Supply voltage	1.2V(internal), 1.8/2.5/3.3V(I/O)
# of TRs, gate, memory	181M TRs, 13.5M Gate 20.2 Mbit mem

G1 Module Diagram



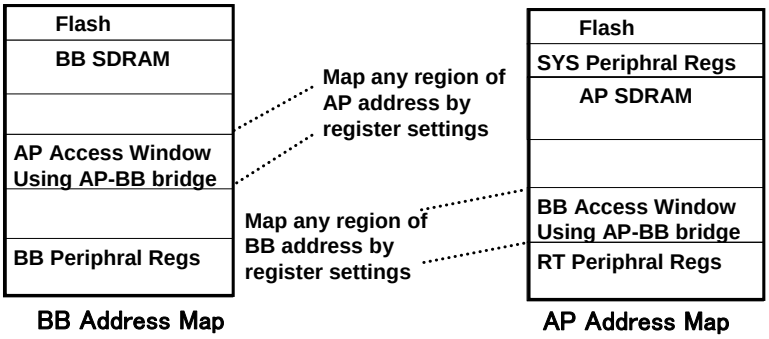
Communication Architecture

- G1 keeps the communication paths (MFI and Serials) used in the previous system for software reuse



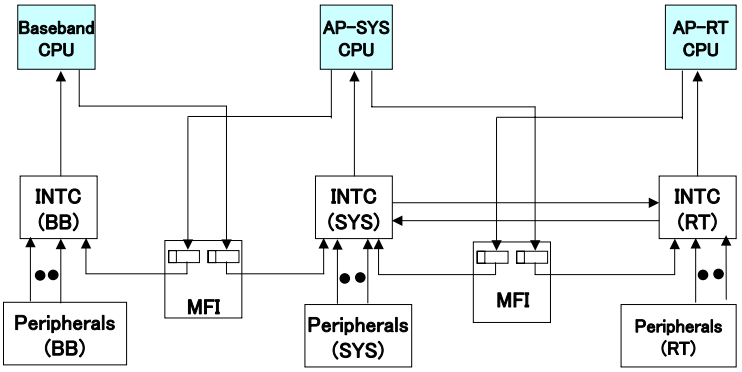
Communication Architecture (Cont'd)

- AP-SYS and AP-RT share SDRAM and memory map
- AP and BB have different SDRAM and memory map
- APBB bridge supports access window scheme to access the resource in the other memory map

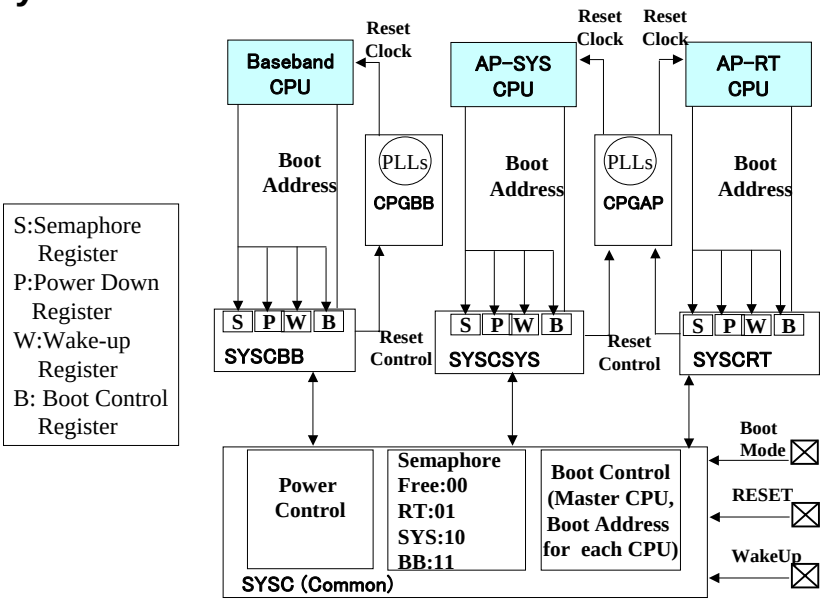


Interrupt Control

- Each CPU has its INT controller
- MFI can generate inter-domain interruptions
- Some external pins generate interrupts for each CPU



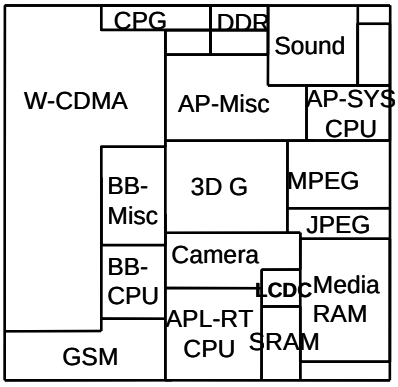
System Control



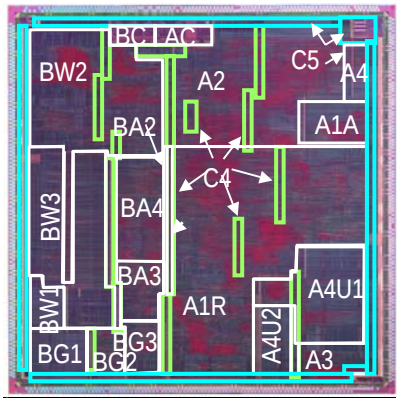
Power Domain (Cont'd)

- **20 hierarchical domains for partial power-off**

Chip Floorplan

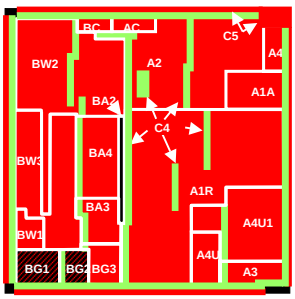


Power Domains



Leakage Current in Usage Scenes

(1) Video telephony



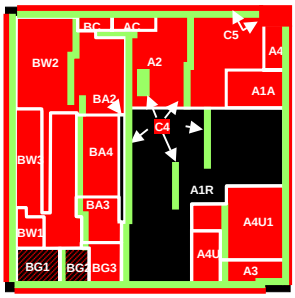
Power on

Power off

Baseband part	Control	ON
	W-CDMA	ON
	GSM	ON / OFF
Application part	System-domain	ON
	Realtime-domain	ON
Measured Leakage Current (@ Room Temp, 1.2V)		**849 μA**

Leakage Current in Usage Scenes

(2)Telephony (W-CDMA)



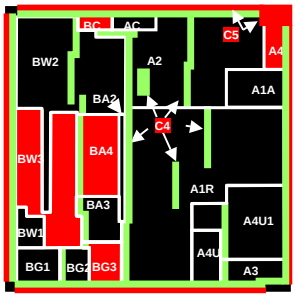
Power on

Power off

Baseband part	Control	ON
	W-CDMA	ON
	GSM	ON / OFF
Application part	System-domain	ON
	Realtime-domain	OFF
Measured Leakage Current (@ Room Temp, 1.2V)		**407** μA

Leakage Current in Usage Scenes

(3)Waiting for Calling



Power on

Power off

Baseband part	Control	ON
	W-CDMA	OFF *
	GSM	OFF
Application part	System-domain	OFF
	Realtime-domain	OFF
Measured Leakage Current (@ Room Temp, 1.2V)		**299** μA

*: Intermittent Operation

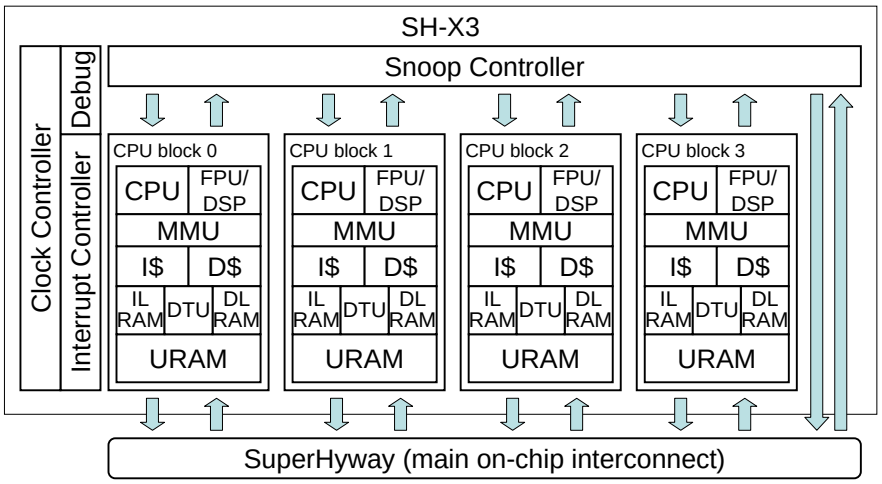
SH-X3: SuperH SH-4A Quad-Core

ref: T. Kamei, “SH-X3 An Enhanced SuperH Core for Low power MP system.” Fall Microprocessor Forum, Oct 2006
Y. Yoshida, et. al., “A 4320MIPS Four-Processor Core SMP/AMP with Individually Managed Clock Frequency for Low Power Consumption.”, ISSCC Tech. Dig. pp.100-101, Feb 2007

Design Concept of SH-X3

- Efficient for both SMP and AMP
  - Cache coherency for SMP
  - Local Memories of each CPU block for AMP
  - Data transfer function for local memories
  - Hybrid model support
- Flexible interrupt architecture
  - Interrupt distribution
  - Inter Processor Interrupt (IPI)
- Power management
  - Minimizing the power of each CPU for workload variation
- Easy implementation in standard SoC design flow
  - Fully synthesizable

Block Diagram



SuperHyway = SuperHyway Bus on-chip interconnect

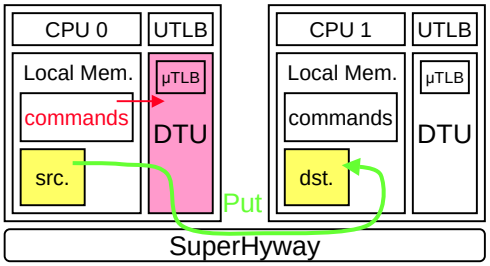
Memory subsystem architecture

Combination of coherent cache and local memories to support variety of programming models

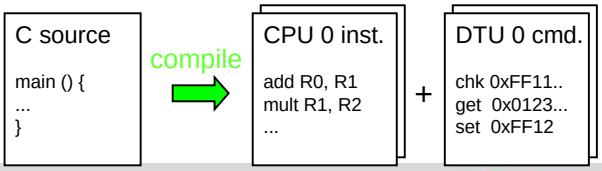
- Coherent cache
  - Implicit allocation (programmer doesn't have to care)
  - Mandatory for SMP operating systems
  - Required for multi-threaded programs (e.g. with pthread library)
- Address-mapped local memories
  - Explicit allocation (deterministic behavior)
  - Add further concurrency of computation and data transfer to ordinal DMA transfer
  - Efficient block transfer (larger than cache line size)
- Two-level local memories
  - Small but no-wait memory (I/D separate: up to 128KB)
  - Large but a few wait memory (unified: up to 1MB)

Data Transfer Unit (DTU)

- Concurrent data transfer with CPU computation
- Programmability by transfer commands on local memories
- MMU support: micro-TLB
- Max. throughput: 800 MB/s /DTU @ 300MHz SuperHyway



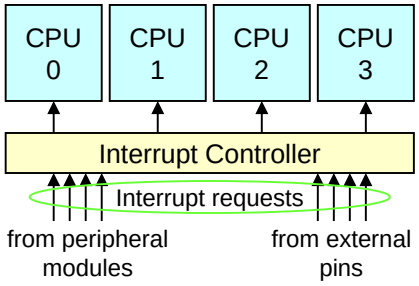
Automatic Parallelizing Compiler
(OSCAR compiler by Waseda Univ.)
•Parallelization of sequential programs
•Extraction of data transfer and generation of DTU commands
•Almost same performance as hand parallelized (MPEG2 enc.)



Interrupt architecture

Two distribution modes
- Static mode
  - bound to specified CPU (configurable binding)
- Dynamic mode (used in some SMP OSs)
  - broadcasted to all CPUs
  - serviced by CPU ACK'ed first

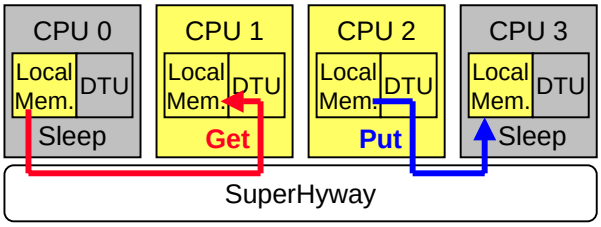
Inter Processor Interrupt
To communicate with other CPUs



Power Management

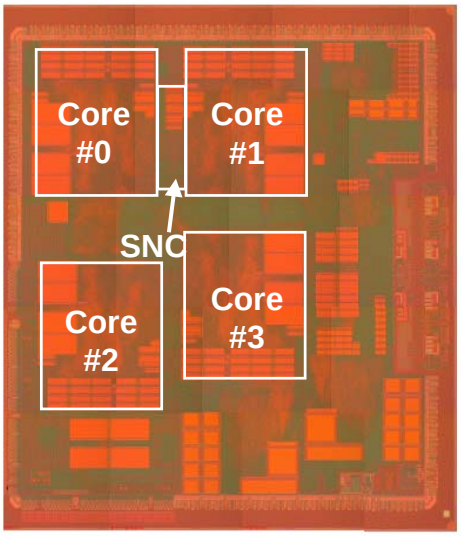
Fine power management for workload variation
- Independent clock slowing down for each CPU
- Four low power states

state	CPU	cache	local mem.
Light Sleep	Clock stop	Active	Active
Sleep	Clock stop	Clock stop	Active
Resume-Standby	Power off	Power off	Clock stop
Ultra-Standby	Power off	Power off	Power off



CPU 0: job done
CPU 1: on-going
CPU 2: on-going
CPU 3: waiting for data

RP1: Chip Overview



Die size	9.88mm x 9.88mm
Process	90nm G 8-layer CMOS dual-Vth
Supply voltage	1.0V(internal), 1.8/3.3V(I/O)
Frequency	600MHz
I/D Cache	32KB 4way(each CPU)
ILRAM	8KB (each CPU)
DLRAM	16KB (each CPU)
User RAM	128KB (each CPU)
CPU Performance	4320MIPS (Dhrystone2.1)
FPU Performance	16.8 GFLOPS
Power	0.6mW/MHz/Core

EXREAL Platform™

EXREAL Platform™

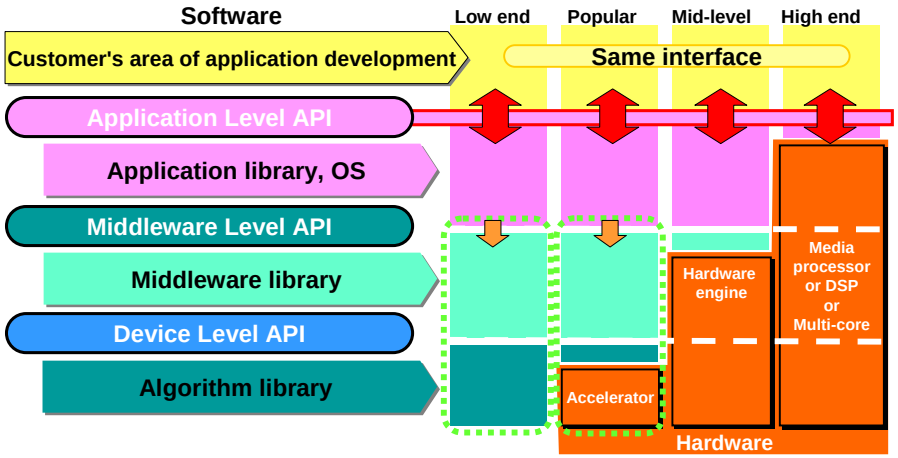
EXcellent Reliability Efficiency Agility Link Platform

EXREAL Platform™ Software Interconnect

- Promote reuse of software assets through Wrapper and standardized layer API
- Control operating frequency and power on/off through the performance scheduler

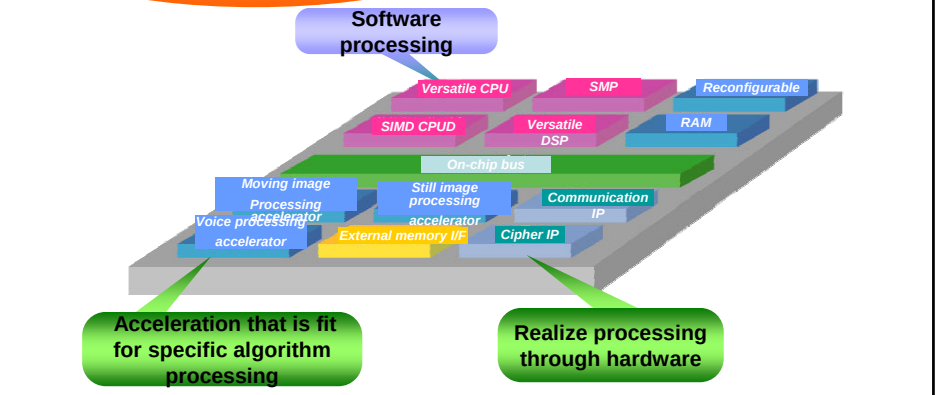
Software Does Not Need to Worry about Hardware

- Flexible replacement of hardware IP and software IP
  - IP changes in the lower layer do not affect the upper layer
  - Possible to select different implementation that possess the identical API



EXREAL Platform™: Hardware Interconnect

Implement the optimum method for the target processing = Heterogeneous multi-core



Summary

- There is many approaches for embedded MPSoC.
  - Heterogeneous AMP : Integration of subsystems
  - Homogeneous AMP : Hetero-OS / Homo-OS
  - Homogeneous SMP : SMP OS
  - Automatic parallelizing compiler
- System design which implement optimal parallelism with reasonable software design/debug cost is key.
- Renesas is ready to implement MPSoC for the application specific requirements by various approaches with SH-MobileG1 methodology and SH-X3.
- Renesas is proposing EXREAL Platform™ for embedded system design with MPSoC.

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