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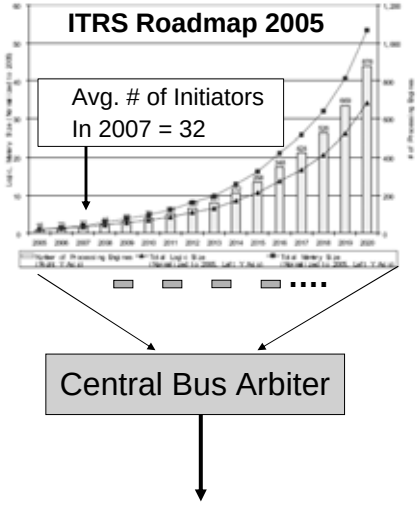
When is the use of a NoC Most Effective and Why
MPSoC, June 2007
K. Charles Janac, Chairman, President and CEO

SoC Communication Complexity Problem

Arbitration problem in an SoC with 30 initiators:
- Hierarchical due to floorplan
- Pipelined due to performance
- Arbiter becomes far too complex

Then designer makes a NoC like bus blindly (no QoS, power mgmt. etc.)

Or builds a NoC intentionally
Or acquires a NoC tool kit
Or acquires a turnkey NoC IP



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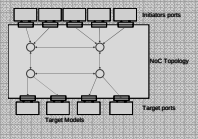
NoC Architecture Application Complexity

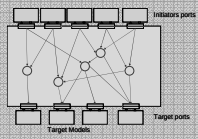
Wireless handset



Mips / mW / $

- **Power Efficient**
- **QoS important**
- **Security**

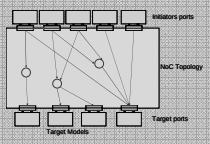
Telecom infrastructure



User Channel / $

- **Performance**
  - –High speed designs
- **Maximum integration**

Multimedia Design



Mips or MB/s / $

- **Complex QOS**
  - DRAM Centric
- **Inter-Chip link**
- **> 60 sockets**

NoCs Improve SoC Architecture Performance

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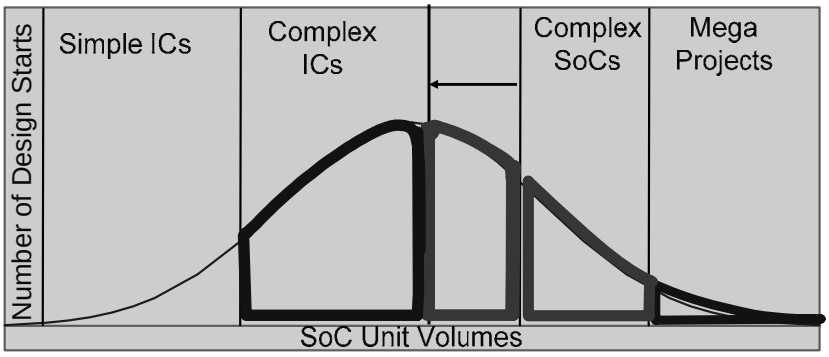
Network on Chip Project Complexity



By 2008
60% SoCs
90 or 65nm

10M units | 25M units

90 &65 nm

Source: Gartner

NoCs Help Manage SoC Complexity

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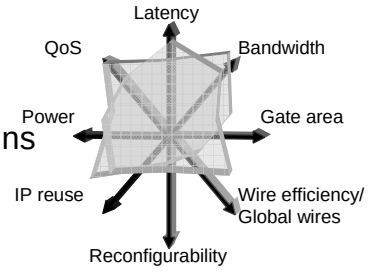
When is a NoC Most Effective and Why?

- **Handling modern SOC complexity lies in the capability to manage multiple constraints above certain thresholds:**
  - Number of Initiators, total IPs
  - Area, Frequency, Power
  - Bandwidth, Latency, QOS
  - Clocks / Power & Voltage domains
  - Floorplan
  - Reuse & Interoperability



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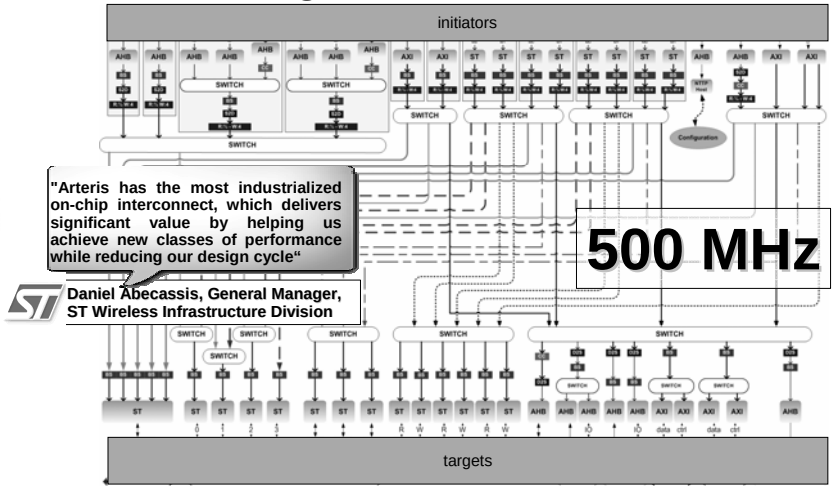
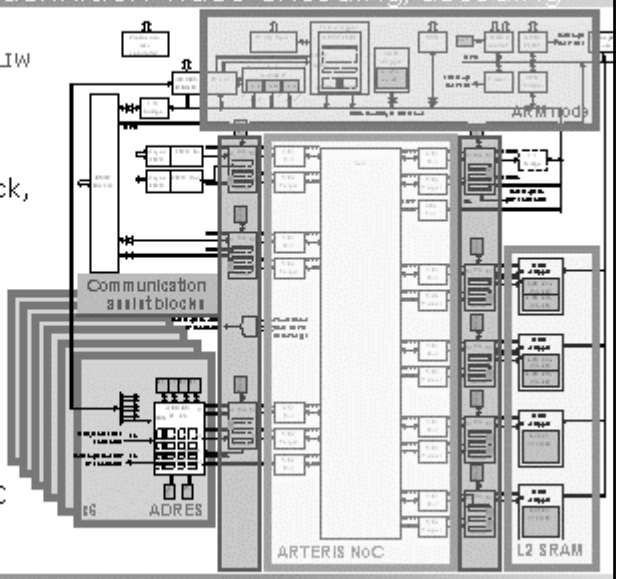
Customer Design: Telecom Infrastructure



Courtesy STMicroelectronics

Multi-processor platform for set-top boxes:
multi-format high definition video encoding/decoding

- 13 nodes
  - ARM926, 6x 25GOPS 2D-VLIW with local L1
  - 2x L2-I$, 2x L2-D$
  - EMIF, Asynch. I/O
- 300MHz processor clock, 150MHz 5Gbps NoC
- 90 nm, 1V, 60mm2, 700mW
- Communication assist for supporting software that guarantees services (throughput, latency)
- Impossible for bus, on the low end for NoC



imec

Courtesy IMEC

Rudy Lauwereins
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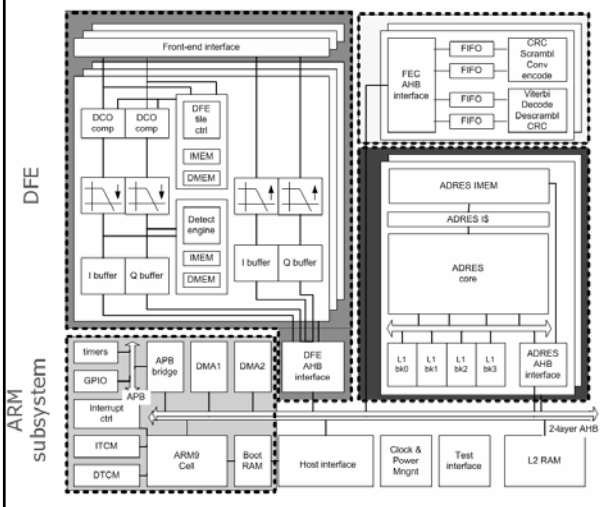
Software Defined Radio baseband platform evolving to cognitive radio



- **Up to 200Mbps SDR**
  - 8 nodes
  - 90nm, 24mm2, 3mW standby, 2nJ/bit 11n-40 2x2, 400MHz
  - Complicated segmented busses
- **Up to 3Gbps Cognitive Radio**
  - >13 nodes
  - 45nm, 50mm2, 3mW standby with sensing, 2nJ/bit, 1GHz
  - NoC

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Courtesy IMEC

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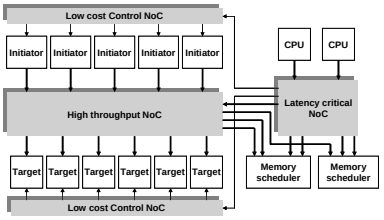
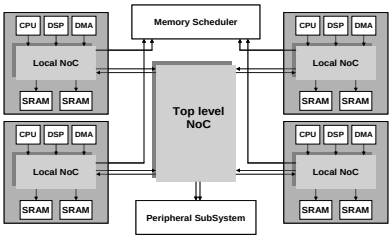
NoC Examples – Architectural Complexity & Variety

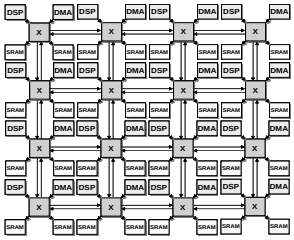
Separated traffic Classes



Clustered design



2D mesh design



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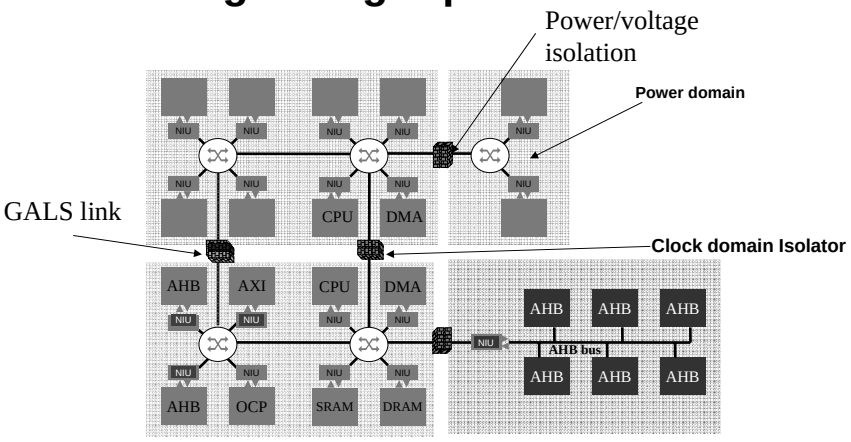
Partitioning timing & power



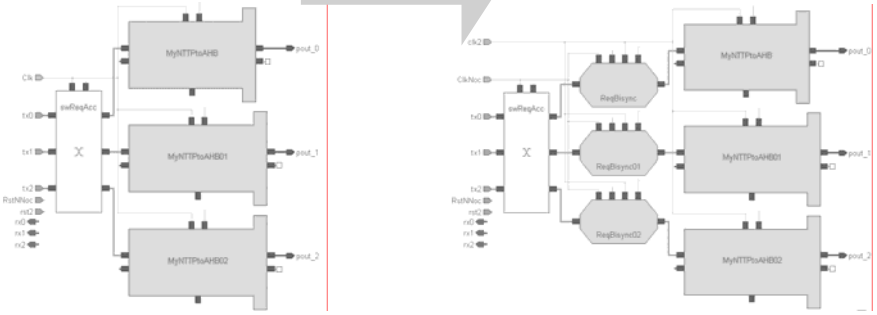
Modular NoC provides ideal boundaries to power and/or clock domains independently

Accommodating Design Change - Quickly

NoC extract V1

Derivative change
New clock
Different PLL

NoC extract V2



The NoC Effectiveness Space

- ≤90nm process
- ≥20 IPs
- >200 Mhz

- Low Power
- Multi IP protocol
- Multi QoS data flows
- Many initiators/many targets

- Fast time to Mkt
- Lower Unit Costs
- Lower Project Costs
- Higher Unit Revenue (telecom)
- Lower Risk for Complex SoC Projects