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An open platform to build MPSoC from Components

Ahmed Jerraya

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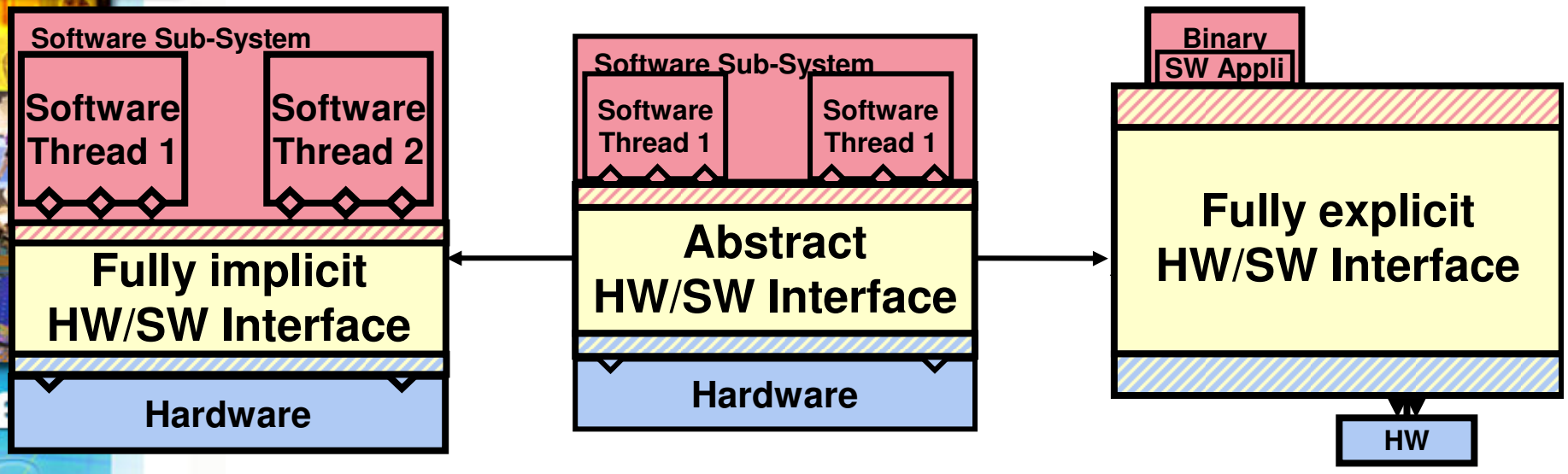
Summary

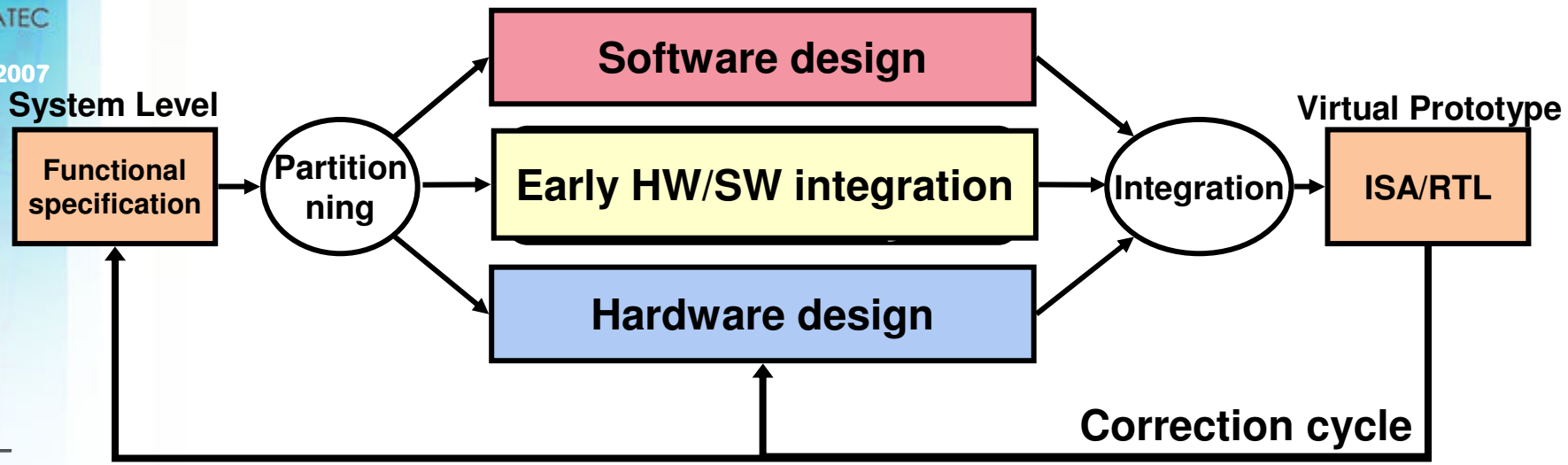
- **Problem: MPSoC too much time, efforts**
  - No low cost MPSoC design solution
  - Hard separation between front end (TLM, Simulink, C) and back end (circuit) Architecture exploration using TLM, still far from circuits
  - Hard Separation between Hardware and Software design
  - Keep System level Model as the reference model during the design process
  - Redesign of derivative solution still very expensive
- **Objectives: Mitigate the problem**
- **Related work:**
  - Virtual prototyping of MPSoC, Multiple ISS platforms for mixed HW/SW Simulation
- **Contributions: Structuring the flow to separate system design and circuit design**

Challenges

- **Affordable and flexible front end for MPSoC end users**
  - Easy to prototype new application by end user
  - Based on an innovative system design automation
- **Seamless HW-SW Integration**
  - Architecture exploration and Application SW mapping
  - Flexible and scalable composition model for both HW and SW
- **Quality Proven HW and SW IP Modules**
  - Ensure better design success using proven IP

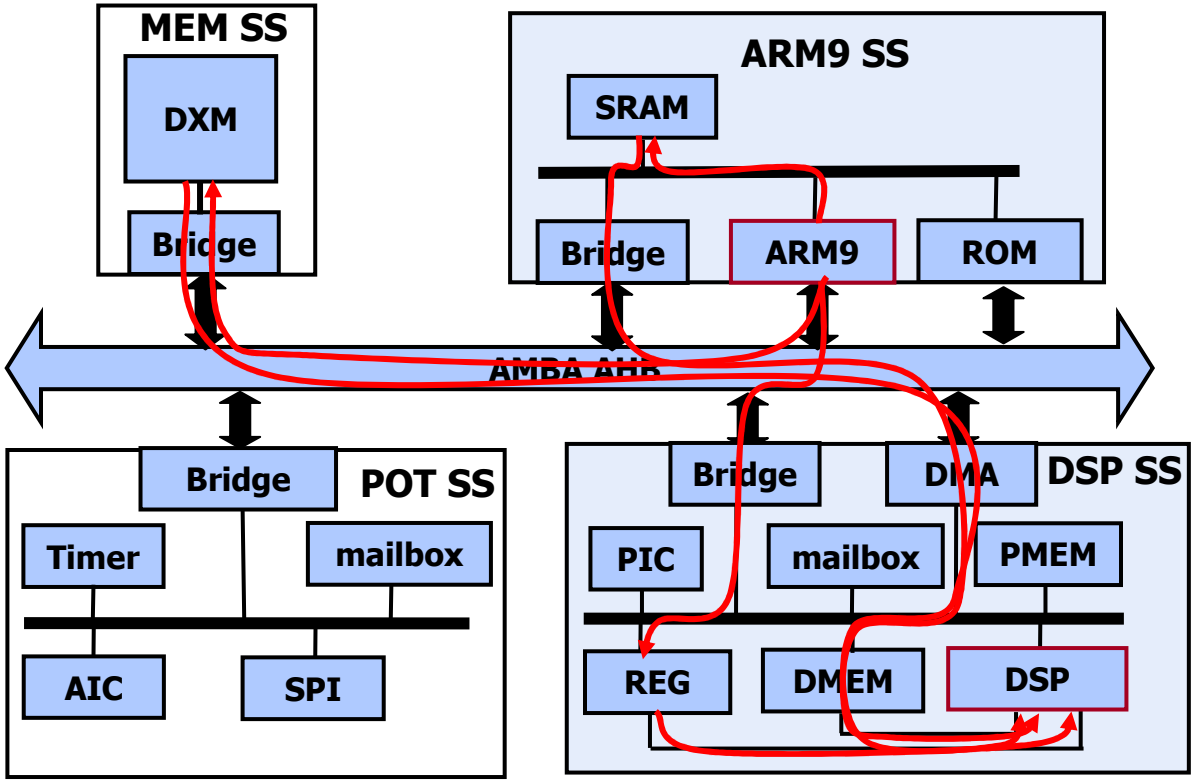
Classical HW/SW Design : The GAPS





Example of Heterogeneous MPSoC Architecture, The Diopsis Tile

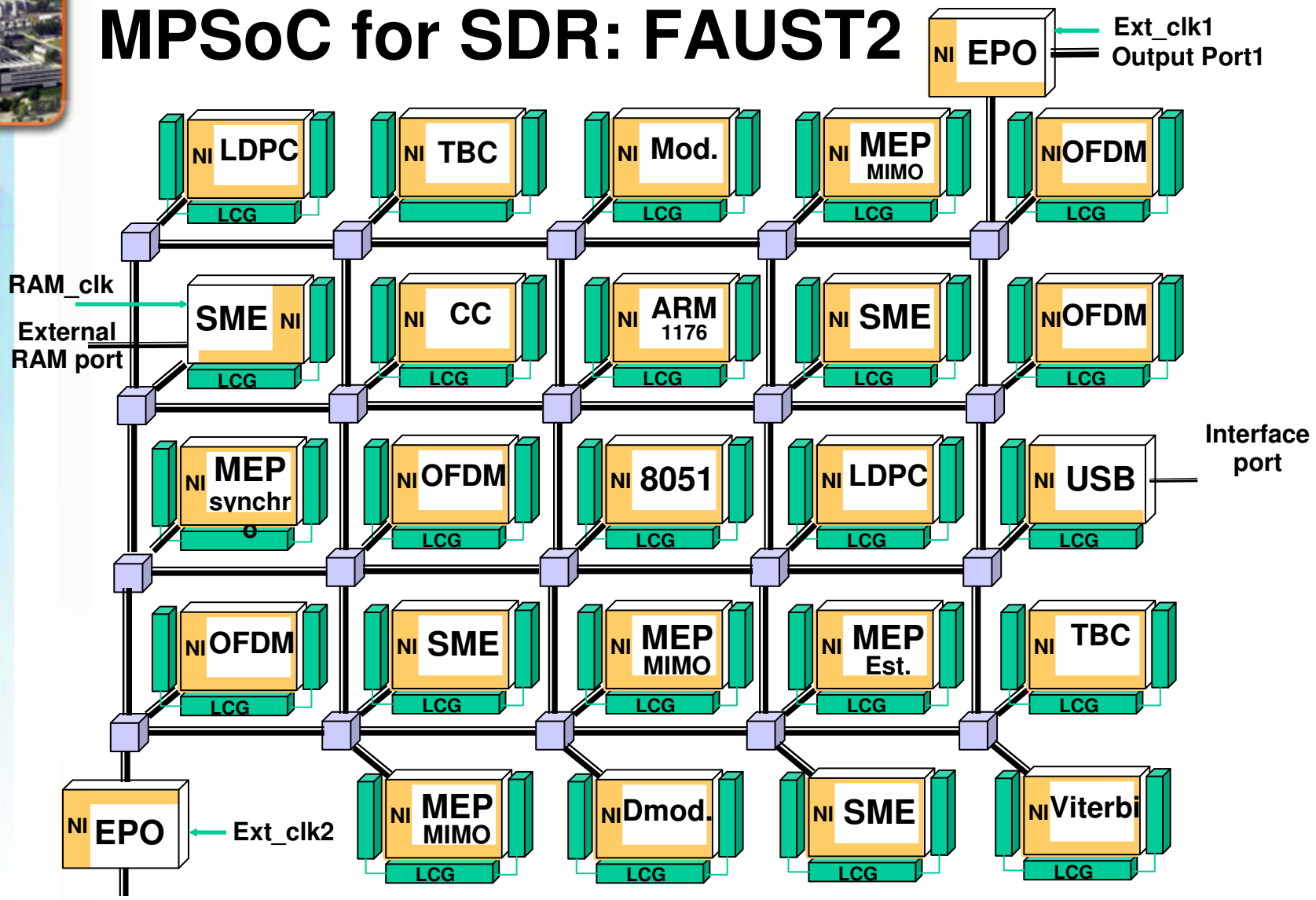
- **ARM9 SS**
- **DSP SS**
- **MEM SS**
- **POT SS (Periph. On Tile):**
  - I/O peripherals
  - System peripherals
- **Interconnect: AMBA bus**



- ***Local & global memories accessible by both processing units***

➢ **Different communication schemes between CPUs**

MPSoC for SDR: FAUST2



MEPHISTO reconfigurable cores

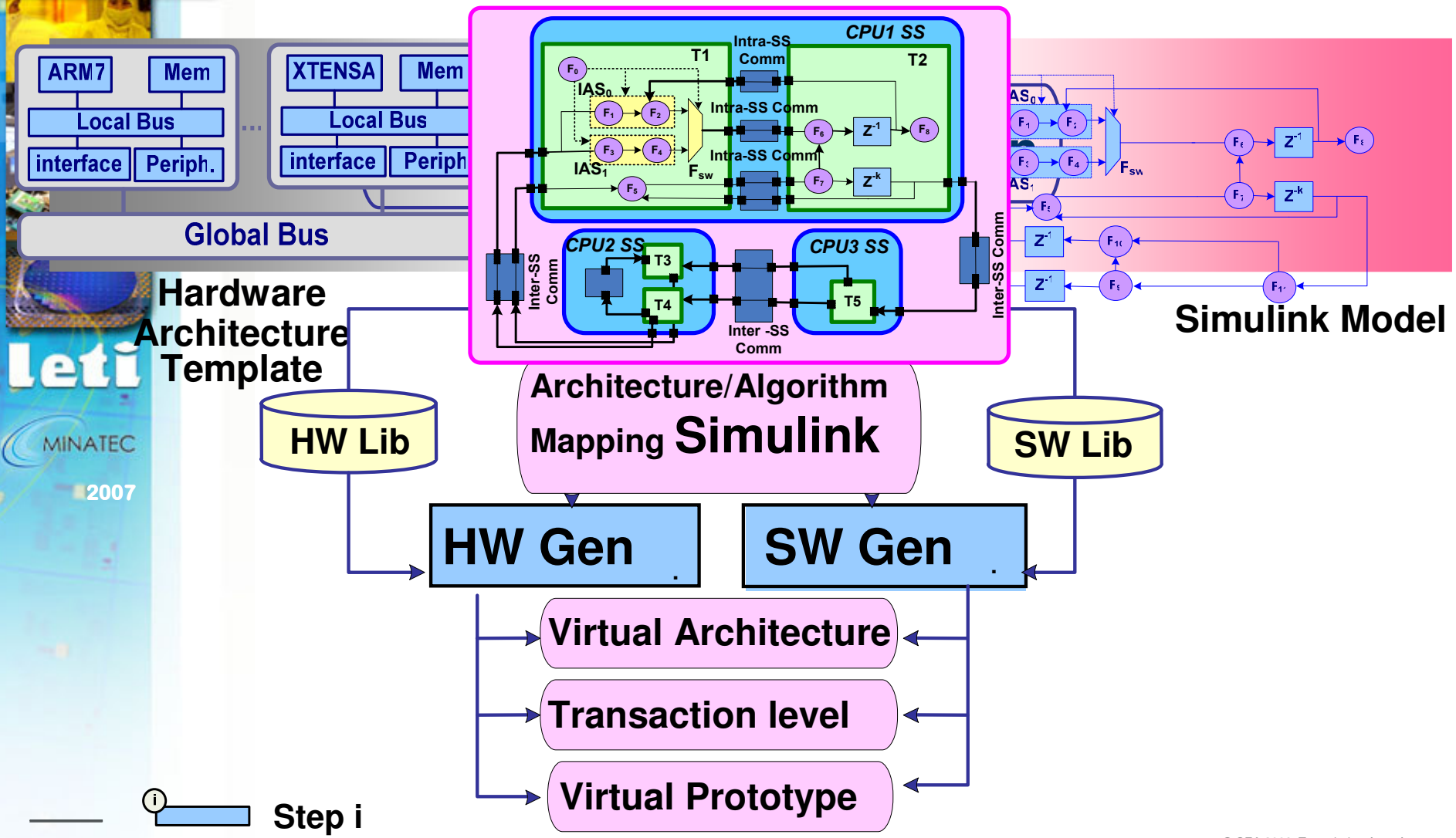
Smart Memory Engines cores

IP programmable cores

Low-power general controler

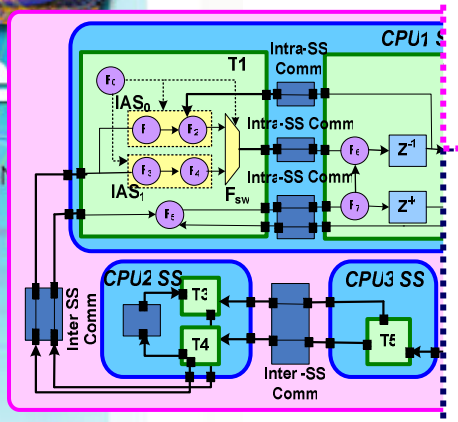
CPU core (MAC support)

Ideal Design Flow



HW and SW Mixed Models

- Seamless refinement at four abstraction levels:
  - Simulink Combined Algorithm and Architecture Model (Simulink CAAM)
  - HW/SW Interfaces refinements



Software Design

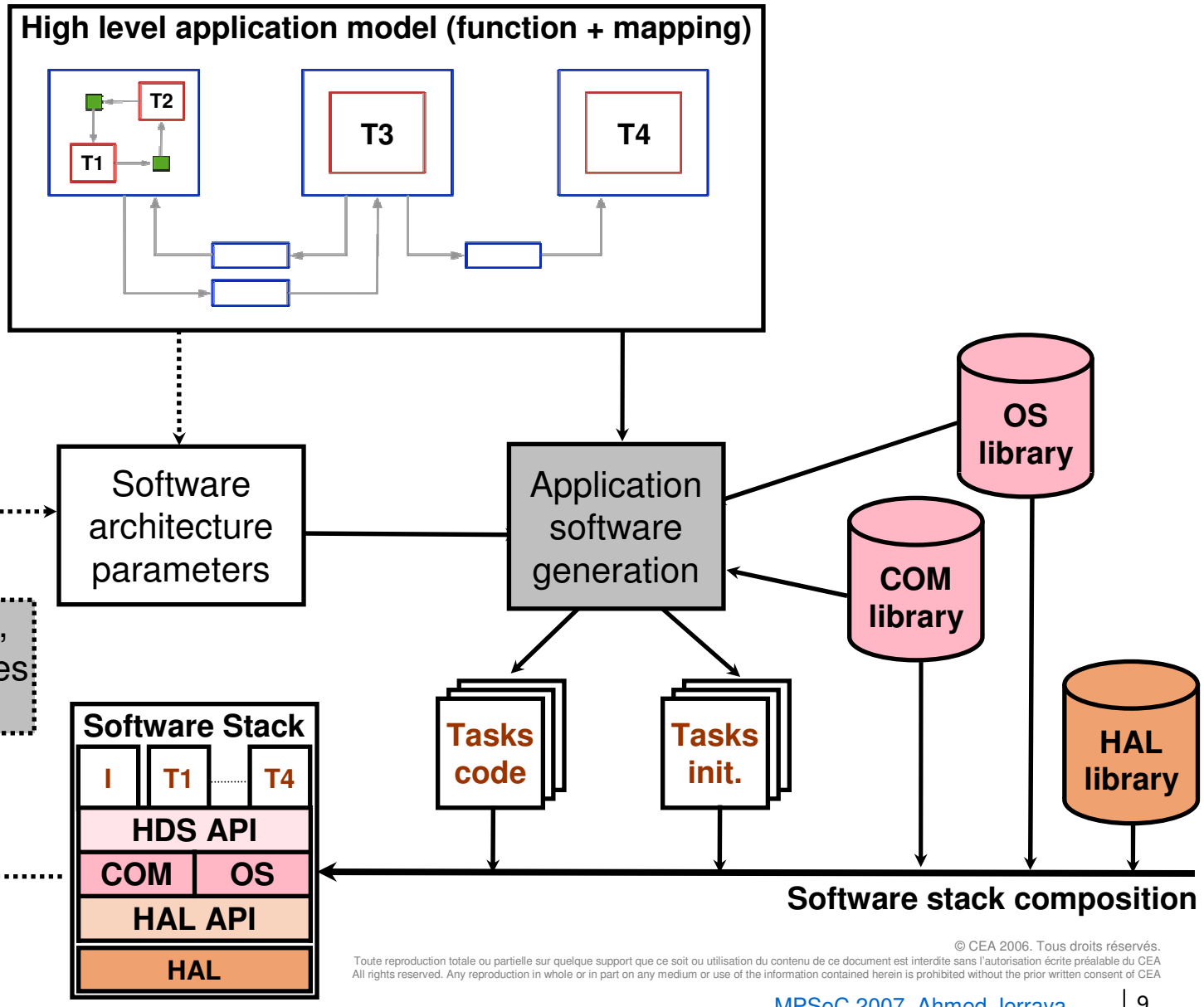
Automatic Code Generation

Hardware Design

Platform based Generators

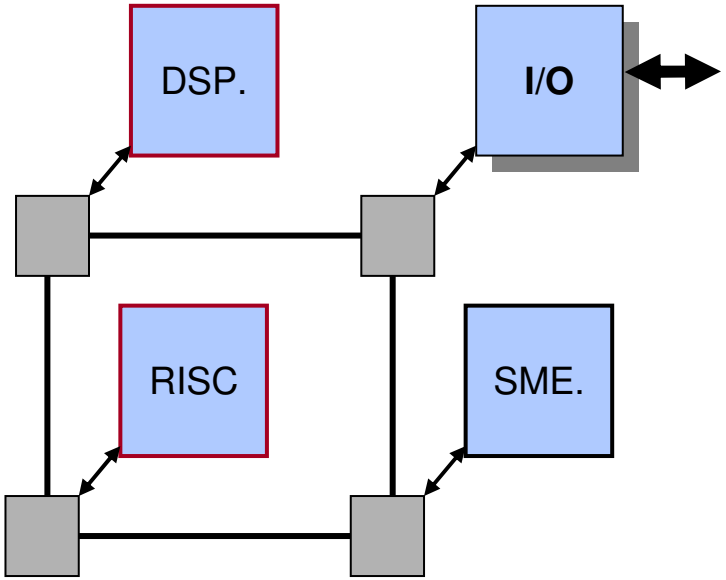
System level model (Simulink CAAM)	Virtual architecture Model (SystemC)	Transaction accurate (SystemC)	Virtual prototype (SystemC)

Software generation environment



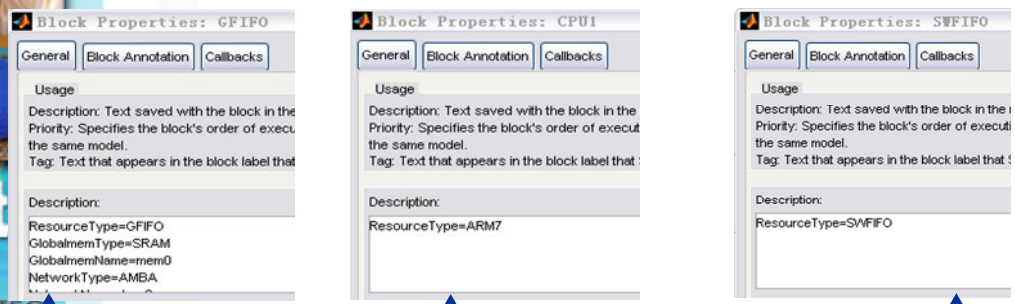
Generic Architecture

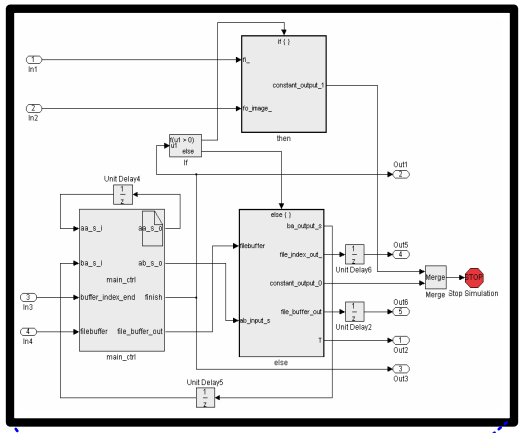
- **Heterogeneous architecture based on NoC**
  - **Flexible: Kind of Modules fixed by application**
  - **Scalable: Number of Modules fixed by application**
- **Proven Modules**
  - **DSP subsystem**
  - **RISC Subsystem**
  - **Memory Subsystems (SME)**
  - **I/O Subsystem**
- **Interconnect**
  - **Network on Chip**

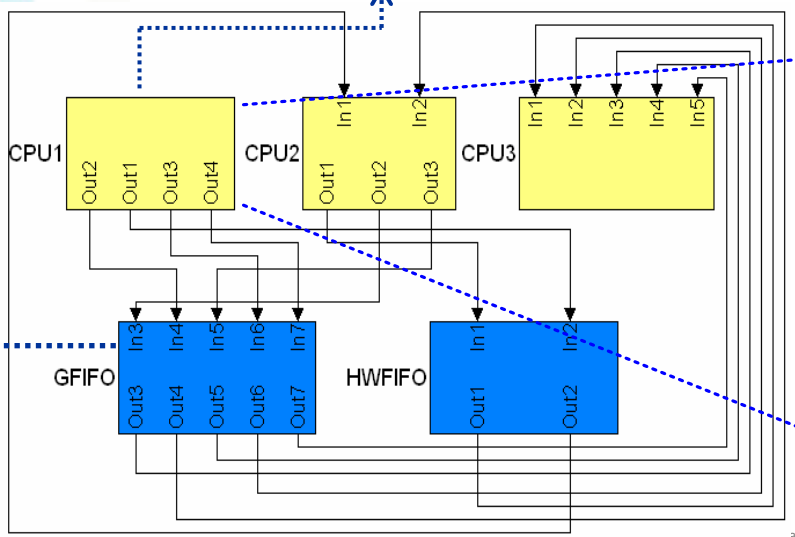


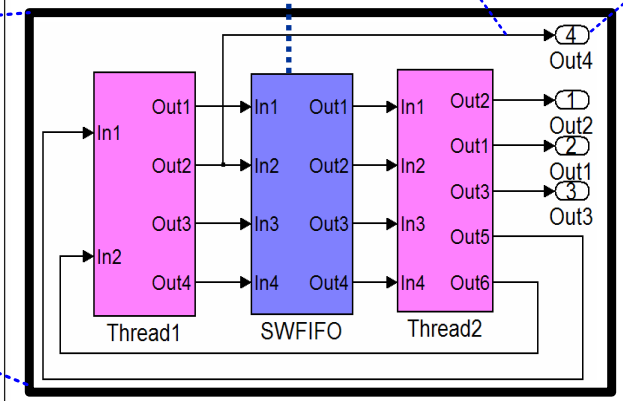
Simulink CAAM of M-JPEG Decoder

- Three CPUs (ARM, Xtensa)
- Communication Units
  (GFIFO, HWFIFO, SWFIFO)









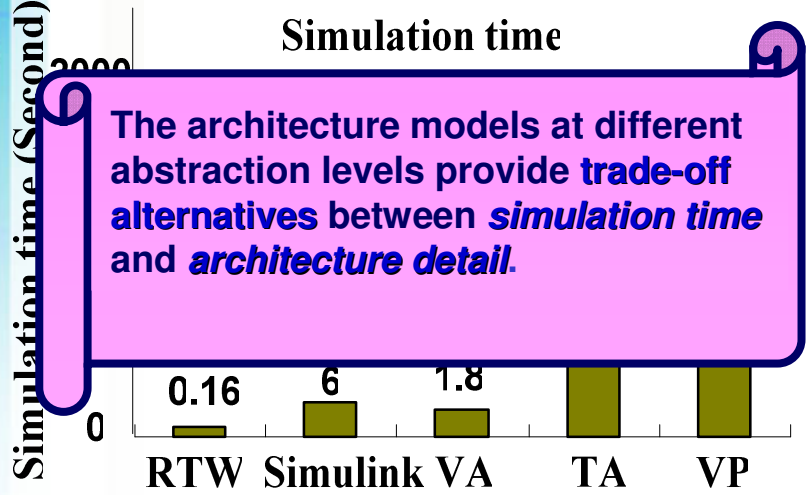
7 S-Functions
7 Delays
26 Links
4 IASs

Experiment Results of MJPEG

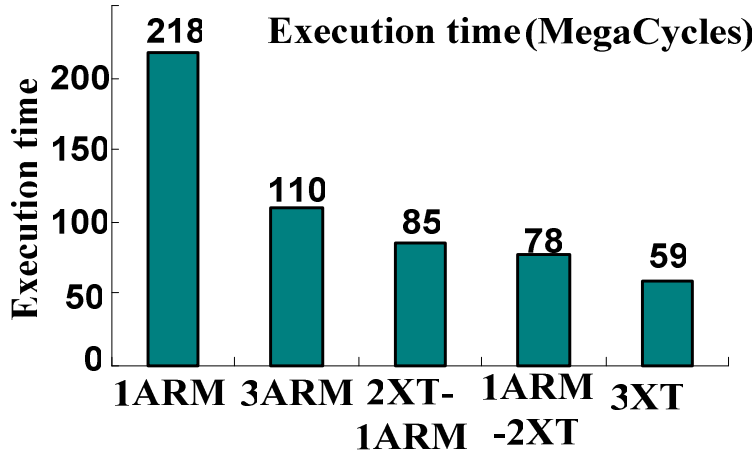
- 10-frame QVGA (320x240) JPEG stream

RTW: sequential program on the host machine
Simulink: Simulation in Simulink GUI
VA: System C model without HW information
TA: Abstract CPU + Other devices (SC TLM)
VP: Cycle Accurate ISS + Other devices (SC TLM)

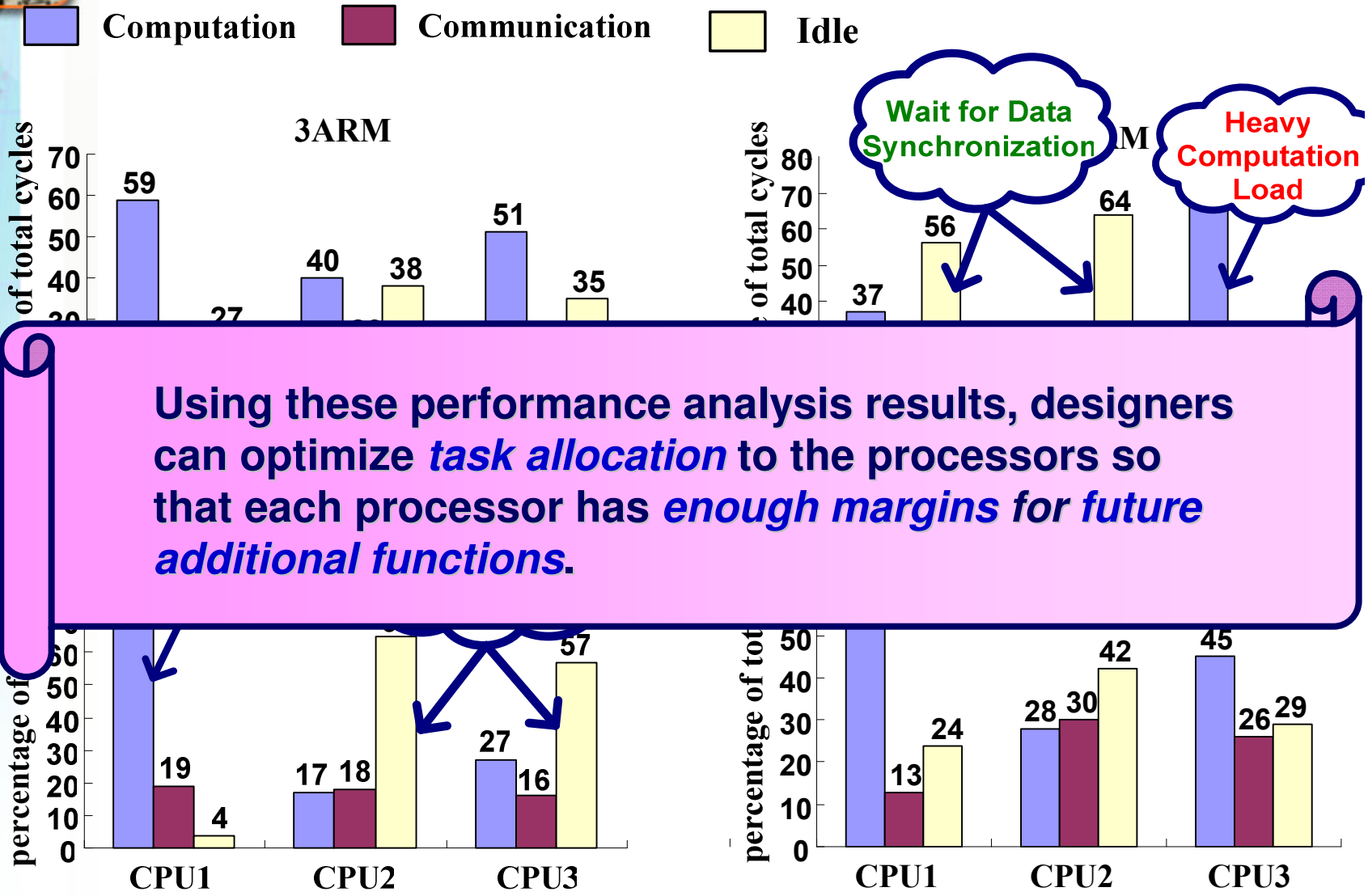
	CPU1	CPU2	CPU3
3ARM	ARM7	ARM7	ARM7
2XT1ARM	Xtensa	Xtensa	ARM
1ARM2XT	ARM	Xtensa	Xtensa
3XT	Xtensa	Xtensa	Xtensa



Three ARM7 Subsystems



Performance Analysis of MJPEG



Using these performance analysis results, designers can optimize *task allocation* to the processors so that each processor has *enough margins for future additional functions*.

Conclusions

- Facilitating the task of system designers in designing and analyzing their mixed signal systems
- Design flow
  - Fast and efficient front end flow for MPSoC designers
  - Separated from backend and IP to be supported by specialized circuit designers
- Efficient design platform: Extendable libraries, easy to integrate new IP

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  - K. Popovici (Design Flow and Abstraction Levels)
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