Design Challenge of a QuadHDTV Video Decoder

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IC Design Tecnology

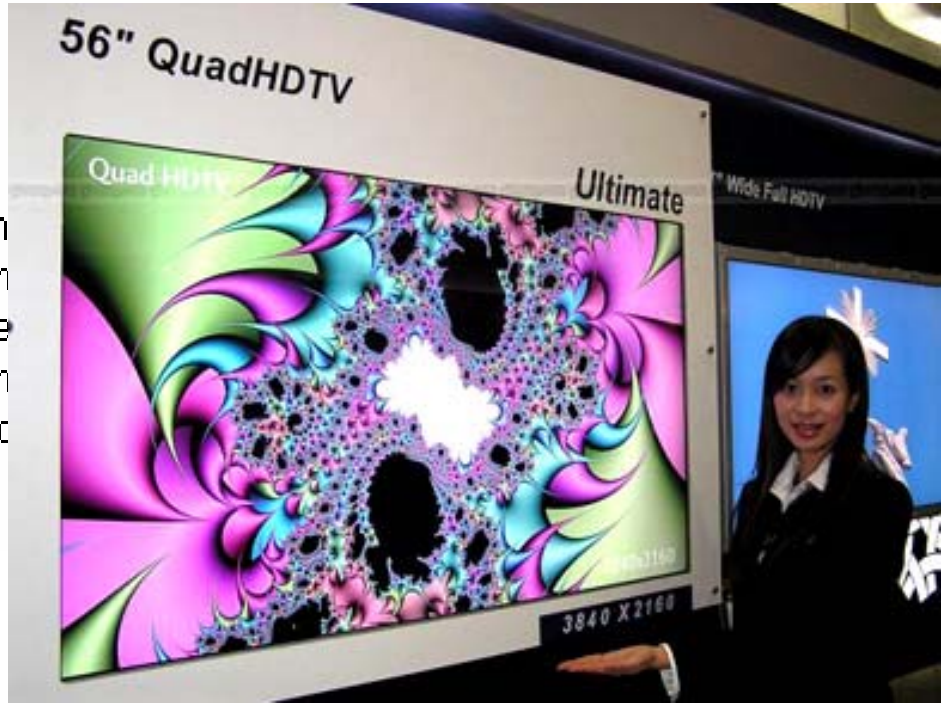
More Pixels

EE Times: Semi News

Record CCD image sensor has 111 million pixels

Peter Clarke
EE Times
(06/19/2006 9:46 H EDT)

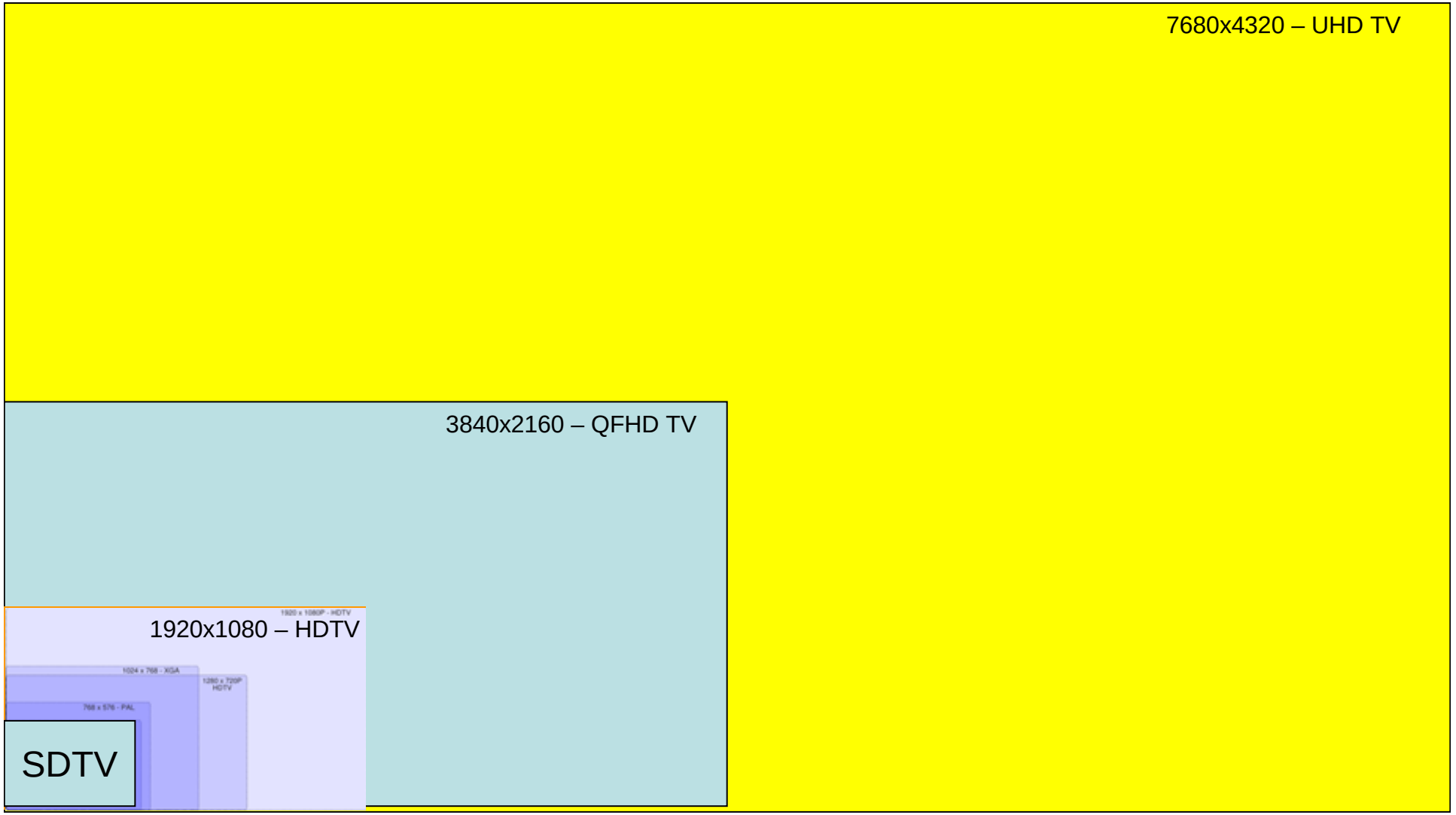
LONDON — Dalsa Semicon
sensor with more than 111 n
claims the 4 x 4-inch charge
10,560 x 10,560 pixels, is th
image sensor and the first to
barrier.



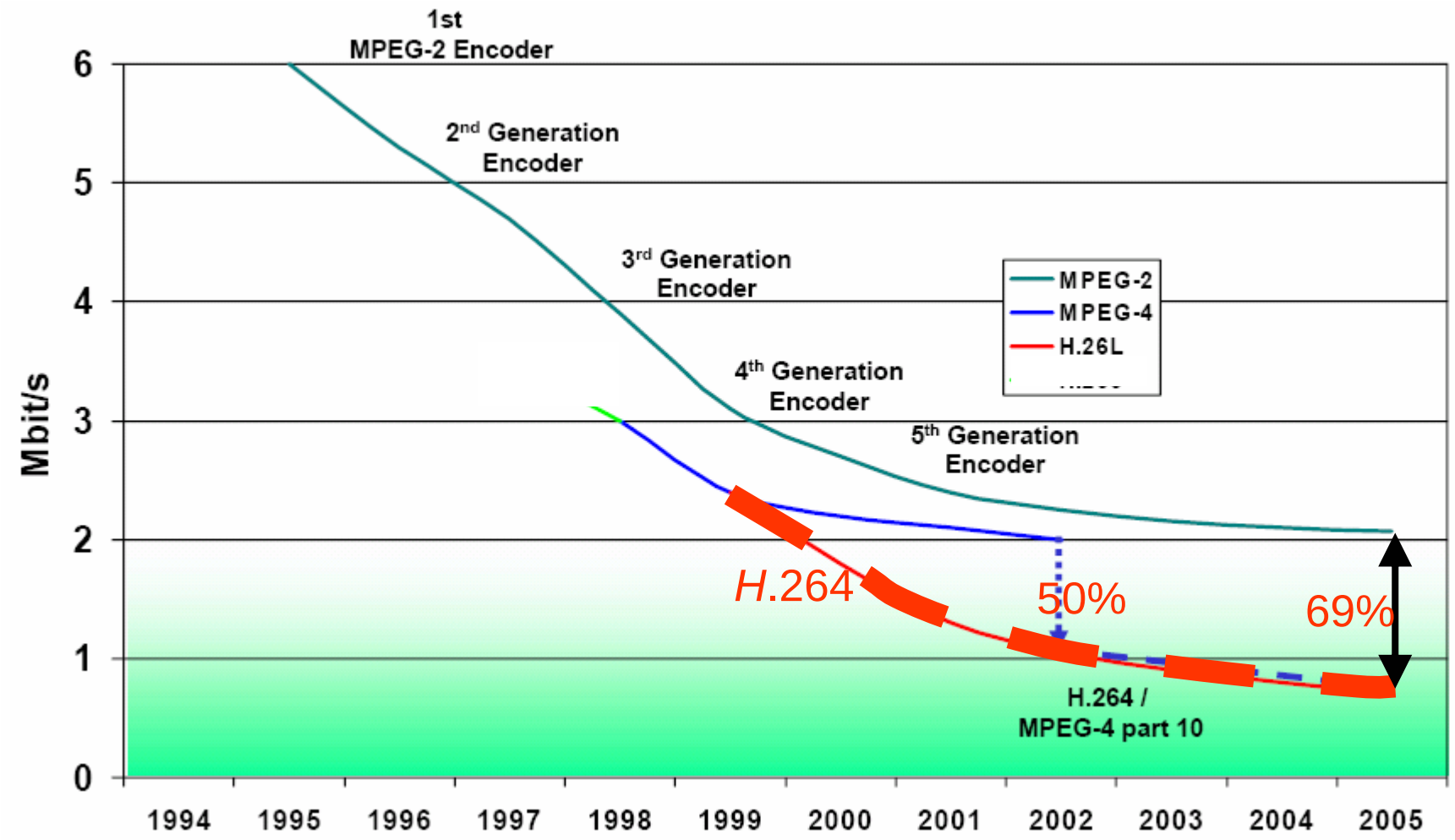
NHK Proposes UHD TV Broadcast

- Super HiVision 7680x4320 pixels at 60 fps (16XHDTV)
- Baseband signal is 24 Gbps. Using 16 MPEG-2 encoding chips, the signal was compressed to 250 Mbps for transmission.
- HDTV signals at present are 1.5 Gbps for baseband and 20 Mbps for compressed signals.
- High Performance compression / decompression and transmission / storage are needed for

  24 Gbps ←→ ~300 Mbps


7680x4320 – UHD TV
3840x2160 – QFHD TV
1920x1080 – HDTV
SDTV

Video Coding Technology Trend



Features of Video Coding Standards

Standard	MPEG-1	MPEG-2	MPEG-4	H.264
MB size	16*16	16*16(frame)	16*16	16*16
Block size	8*8	8*8	16*16, 8*8	16*16, 16*8, 8*16, 8*8, 8*4, 4*8, 4*4
Transform	DCT	DCT	DCT/ Wavelet	4*4 int transform
Entropy coding	VLC	VLC	VLC	VLC, CAVLC and CABAC
ME, MC	Yes	Yes	Yes	41 MVs per MB
Pixel accuracy	½ pel	½ pel	¼ pel	¼ pel
Reference frames	One frame	One frame	One frame	Multiple (5) frames
Picture type	I, P, B	I, P, B	I, P, B	I, P, B
Transmission rate	Up to 1.5 Mbps	2-15 Mbps	64kbps~2Mbps	64kbps ~ 150Mbps

Not all H.264/AVC systems are equal

Relative Computational Complexity

#Ref Frames	Search Range		
	8	16	32
5	16.9	24.6	55.7
1	1	2.54	8.87

Video Coding with H.264/AVC: Tools, Performance and Complexity, J. Ostermann et al, IEEE CAS Mag., Q1 2004.

Quality vs Bit-rate vs Decoding Throughput

Decoding Capability of a 600MHz CPU

QP	Bit Rate (Kbps)	Fps
16	1723	44
21	704	55
26	307	65

H.264/AVC Baseline Profile Decoder Complexity Analysis,
M. Horowitz, IEEE T-CSVT, July 2003

Our Target

- Single-Chip Decoder for QFHD (3840x2160) H.264/AVC High Profile Video
  - CABAD
  - 8x8 Transform
  - Commodity DDR External Memory
  - Platform-Based Design

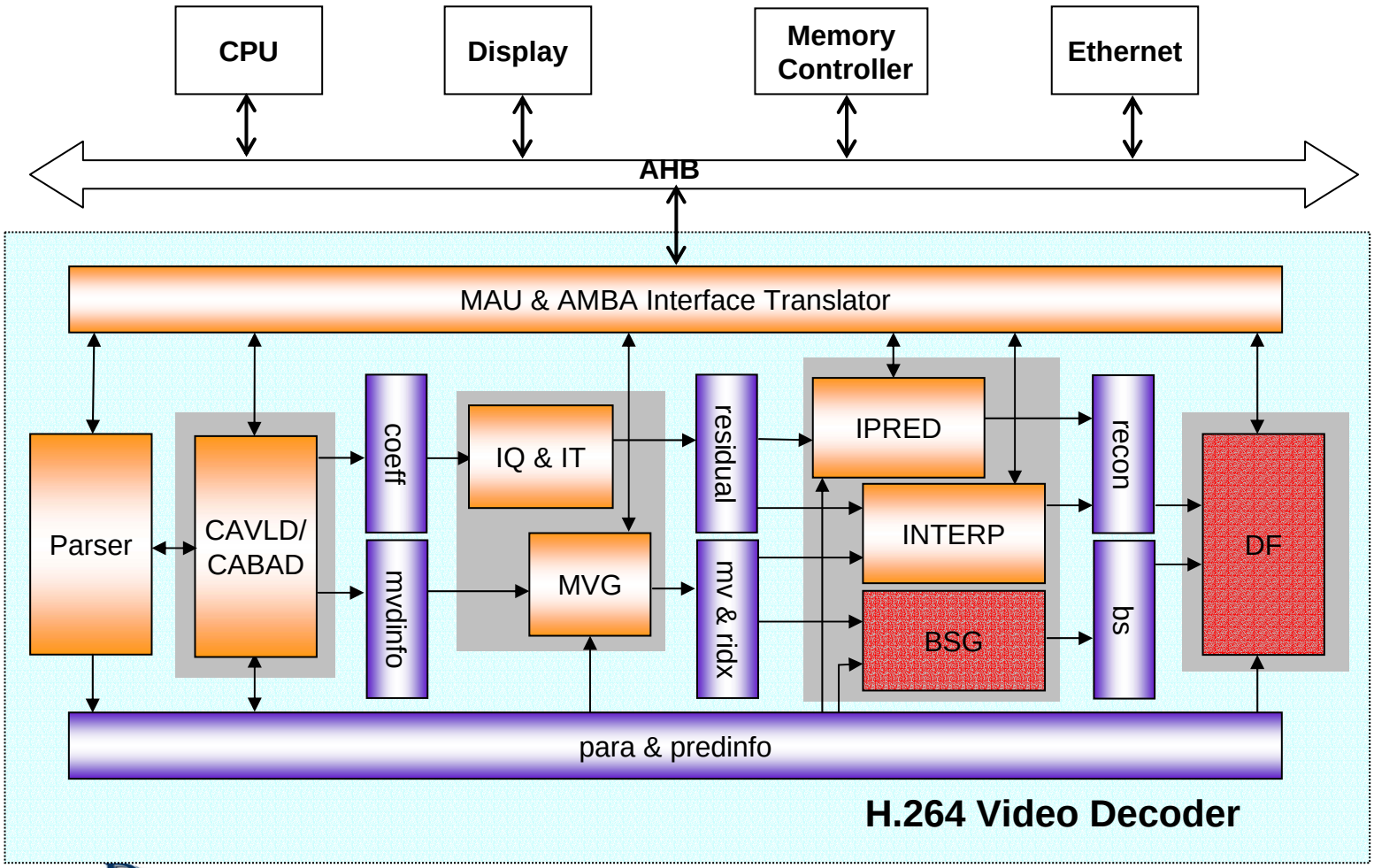
Performance

Resolution	Size	Clock Frequency	Application
SQCIF (128 x 96)	1.0	0.4 MHz	Video phone
QCIF (176 x 144)	2.0	0.8 MHz	
CIF (352 x 288)	8.3	3 MHz	Mobile TV
D2 (720 x 480)	28.1	10 MHz	Car TV、Surveillance
720HD (1080 x 720)	75.0	30 MHz	Home theater
1080HD (1920 x 1088)	170.0	62 MHz	
QFHD (3840 x 2160)	675.0	249 MHz	Digital signage、Medical video、Satellite image、Space exploration

Essential Issues

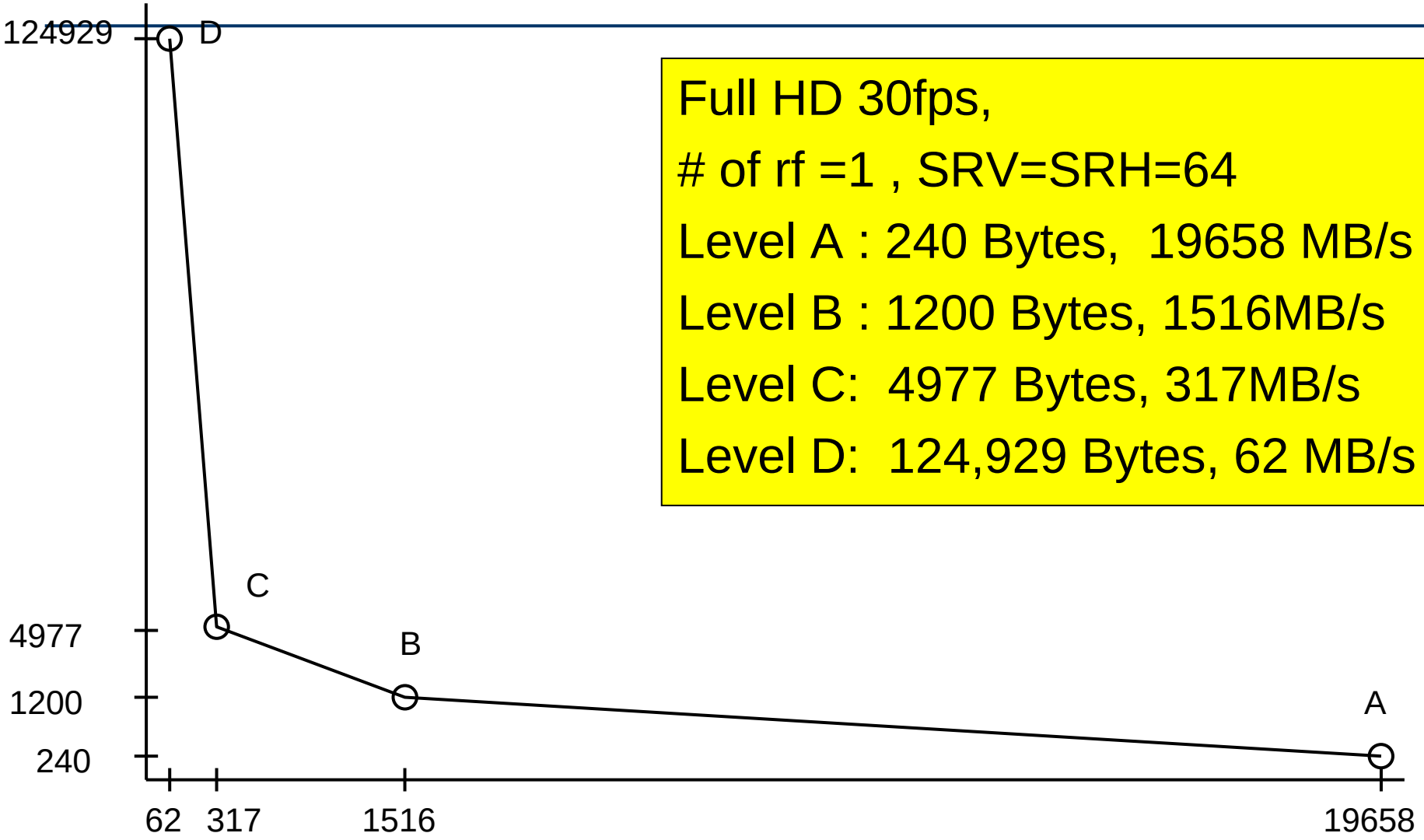
- Memory
  - Tradeoff Between the Size of Internal Memory and Bandwidth of External Access
- Massive Parallelism
- Macroblock Decoding Scheduling

NTHU H.264 Decoder Architecture



Memory

size vs. b/w in ME



Full HD 30fps,

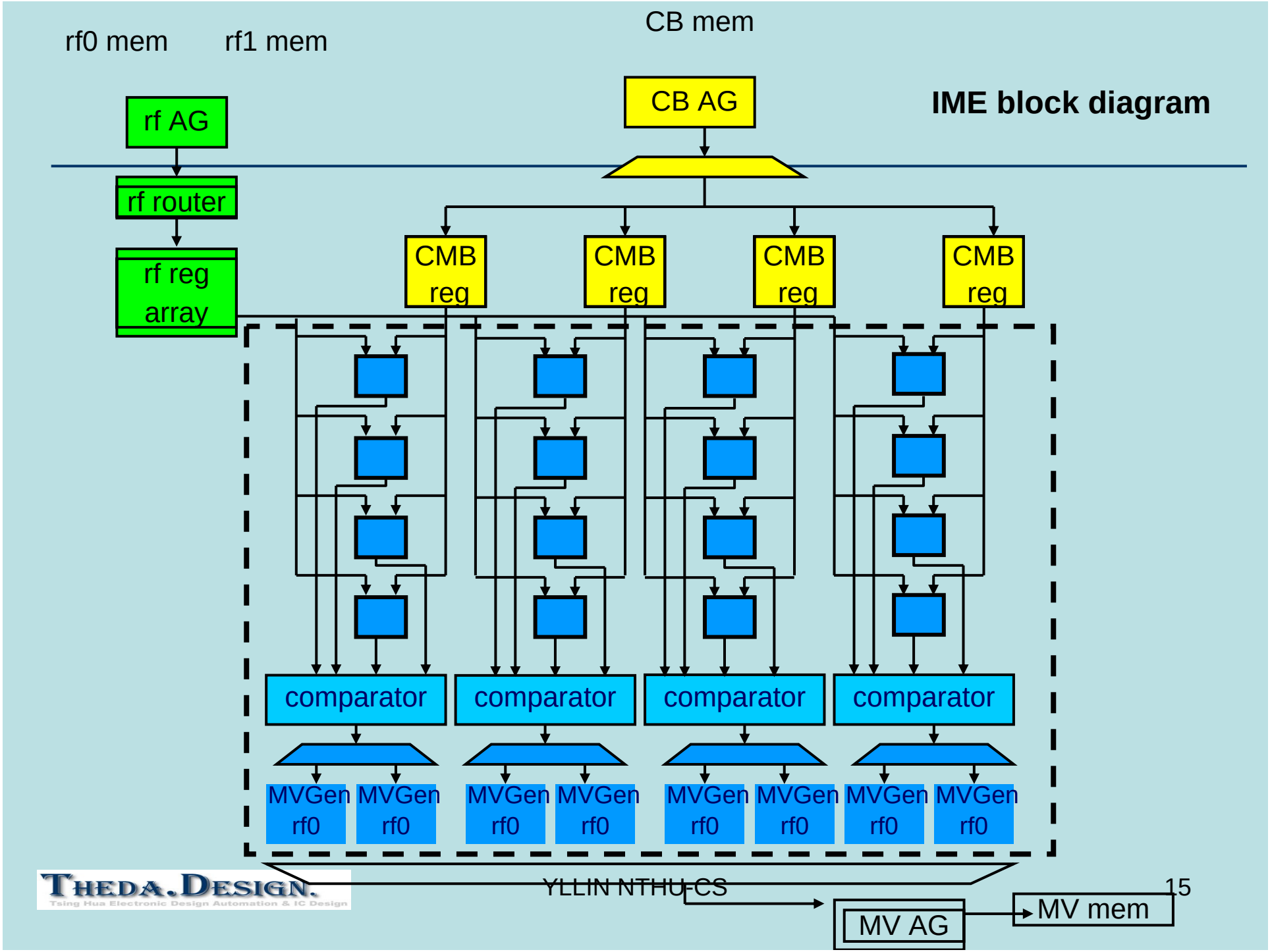
# of rf =1 , SRV=SRH=64

Level A : 240 Bytes, 19658 MB/s

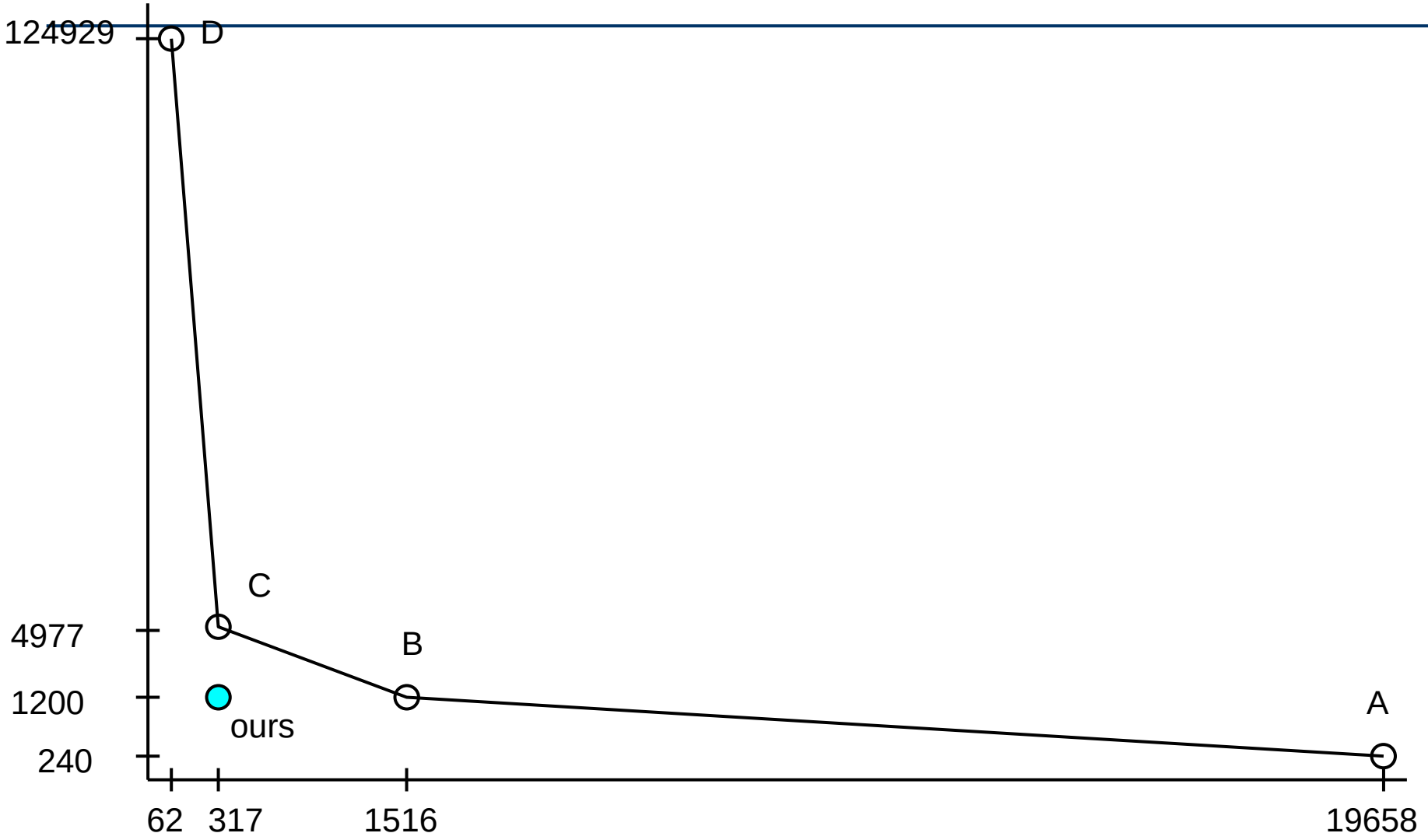
Level B : 1200 Bytes, 1516MB/s

Level C: 4977 Bytes, 317MB/s

Level D: 124,929 Bytes, 62 MB/s

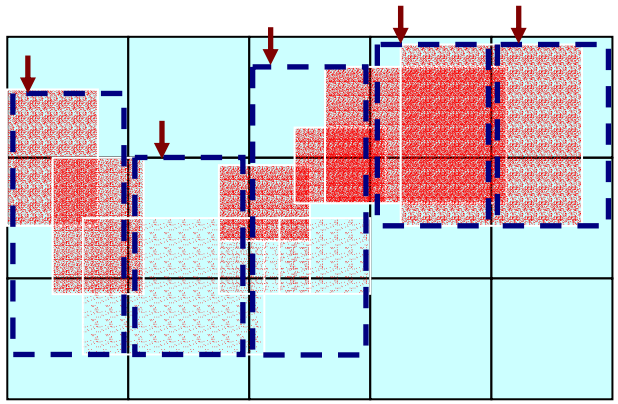

rf0 mem
rf1 mem
CB mem
IME block diagram
rf AG
rf router
rf reg array
CB AG
CMB reg
CMB reg
CMB reg
CMB reg
comparator
comparator
comparator
comparator
MVGen rf0
MVGen rf0
MVGen rf0
MVGen rf0
MVGen rf0
MVGen rf0
MVGen rf0
MVGen rf0
YLLIN NTHU-CS
MV AG
MV mem

size vs. b/w in ME



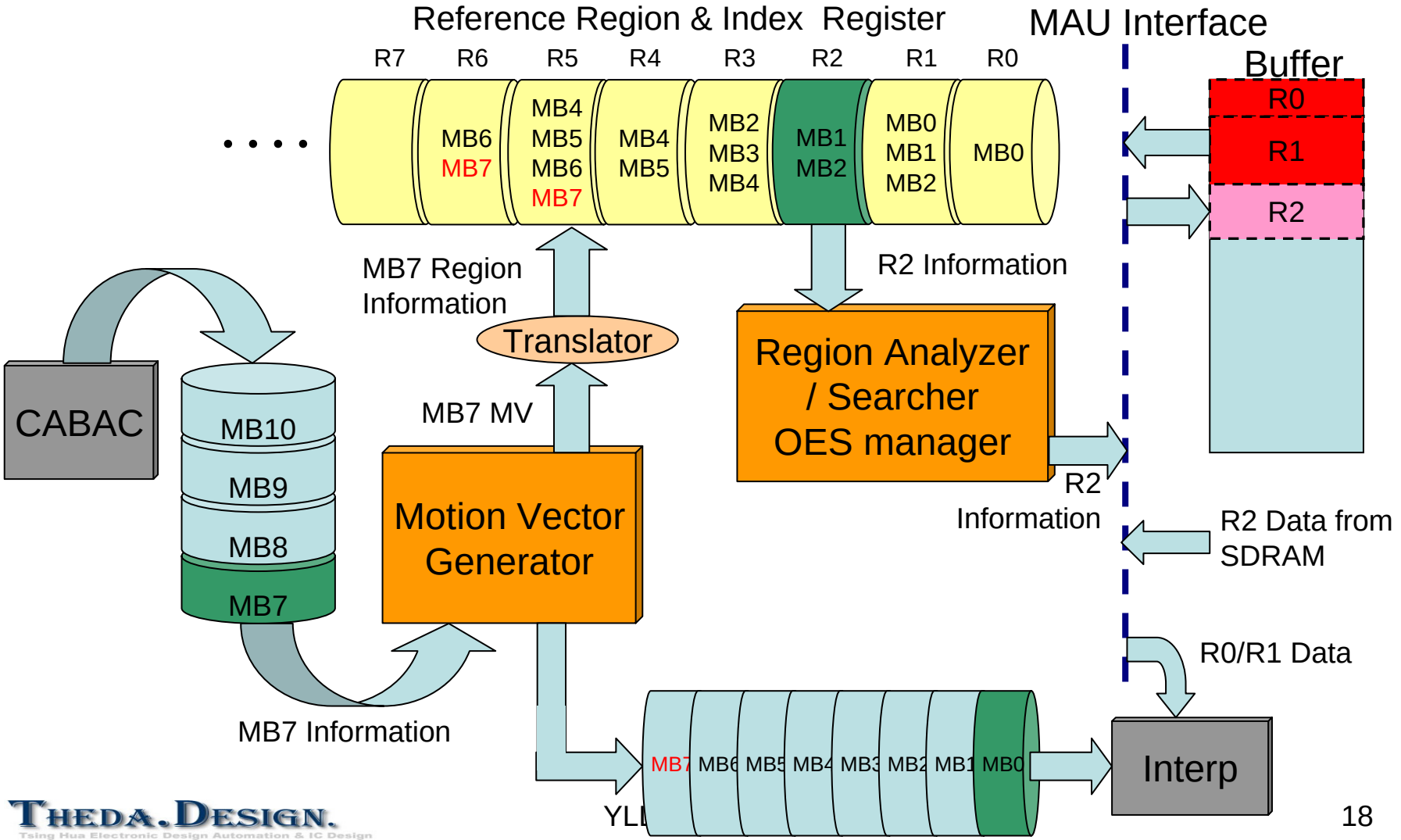
Reference-data Pre-fetch System

- No redundant fetching
  - Collecting several MB's motion vectors, and read the same place by only one single operation
- Minimize the number of burst initials
  - Averagely 2 burst initials per MB (1 for luma, 1 for chroma)



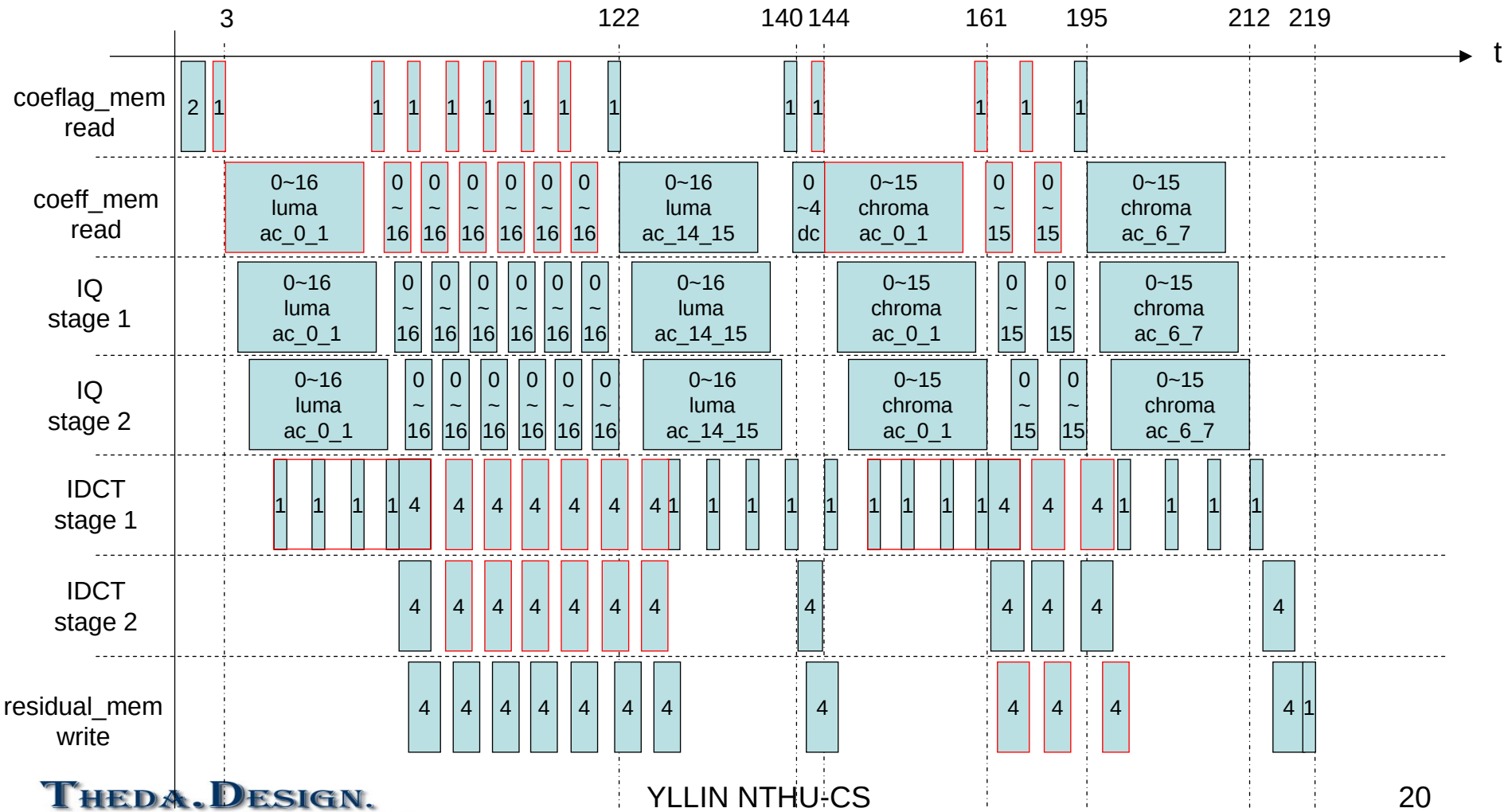
↓ : a group of sequentially read (burst read)

Reference-data Pre-fetch System (Cont)

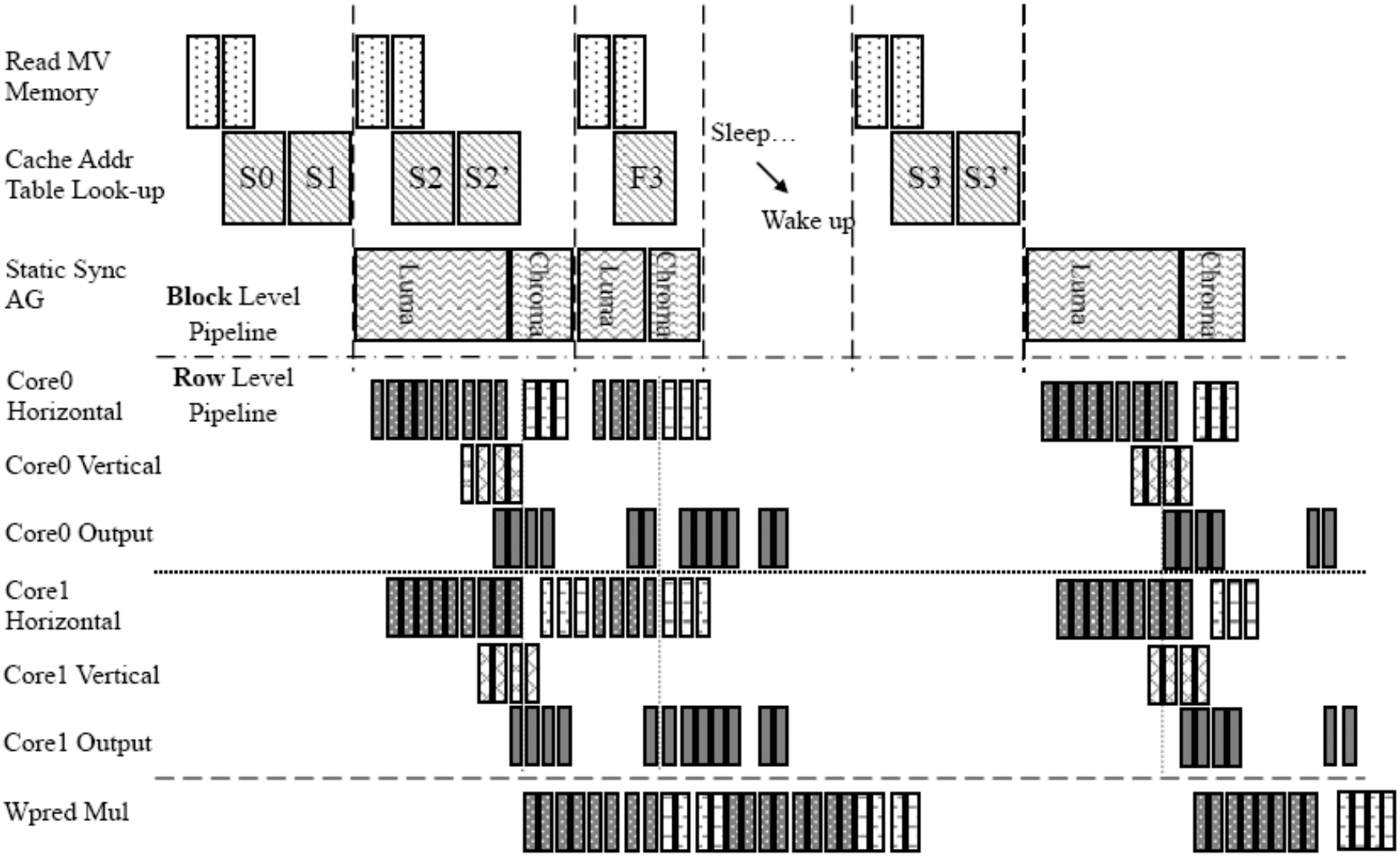


Massive Parallelism

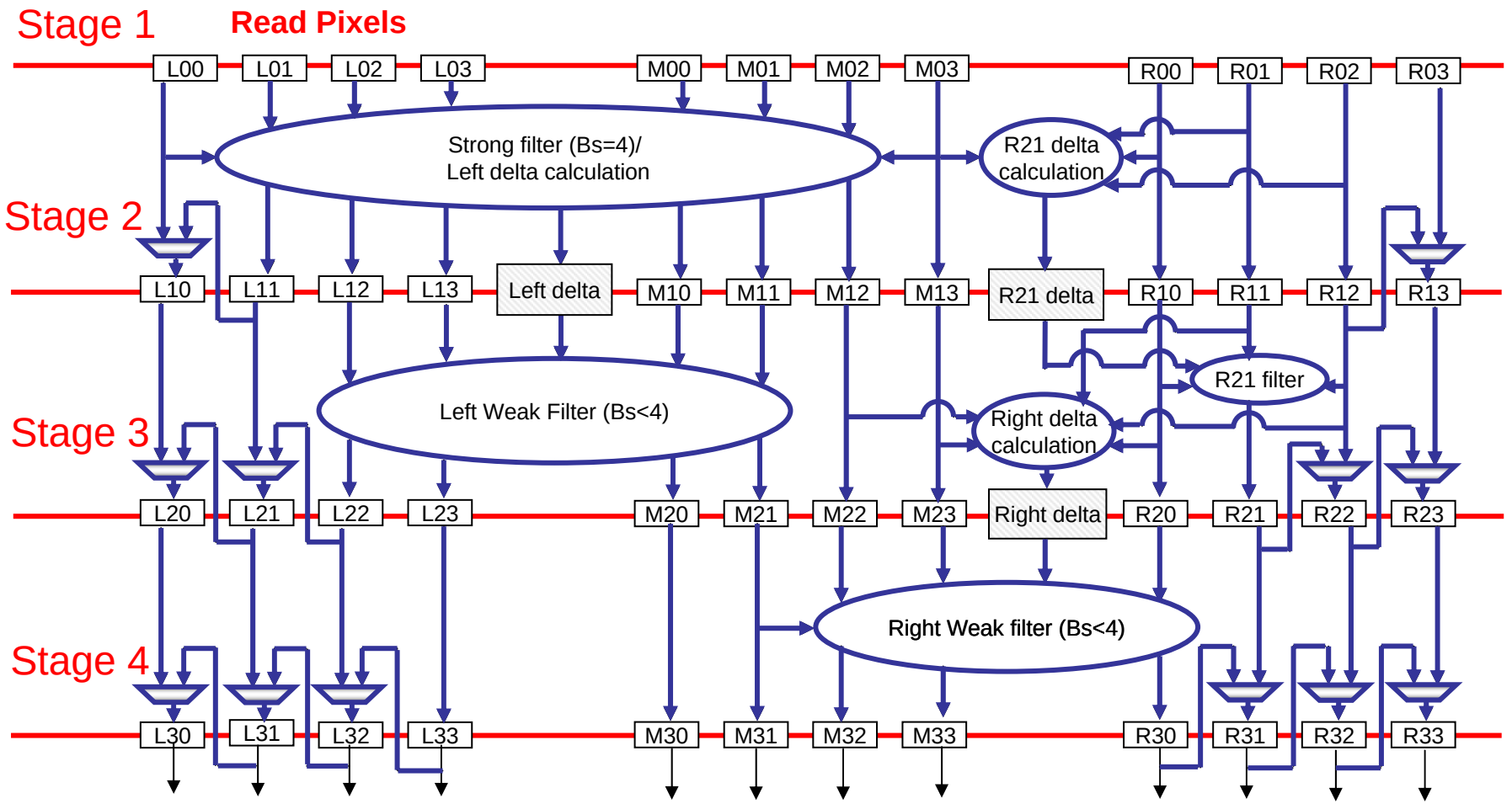
RLD/IQ/IDCT Timing Diagram



DF Timing Diagram



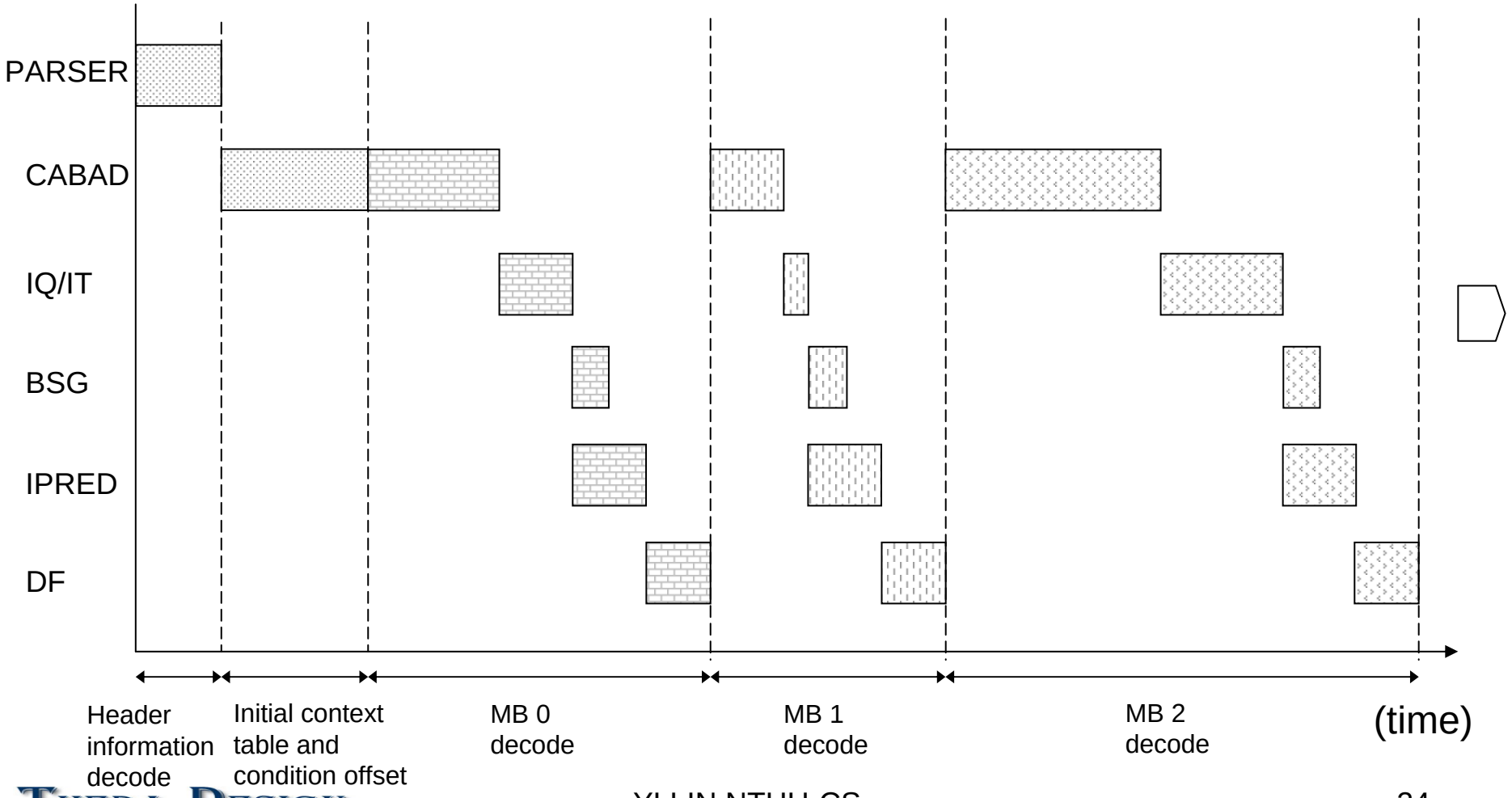
Dual Pipelined Edge Filter



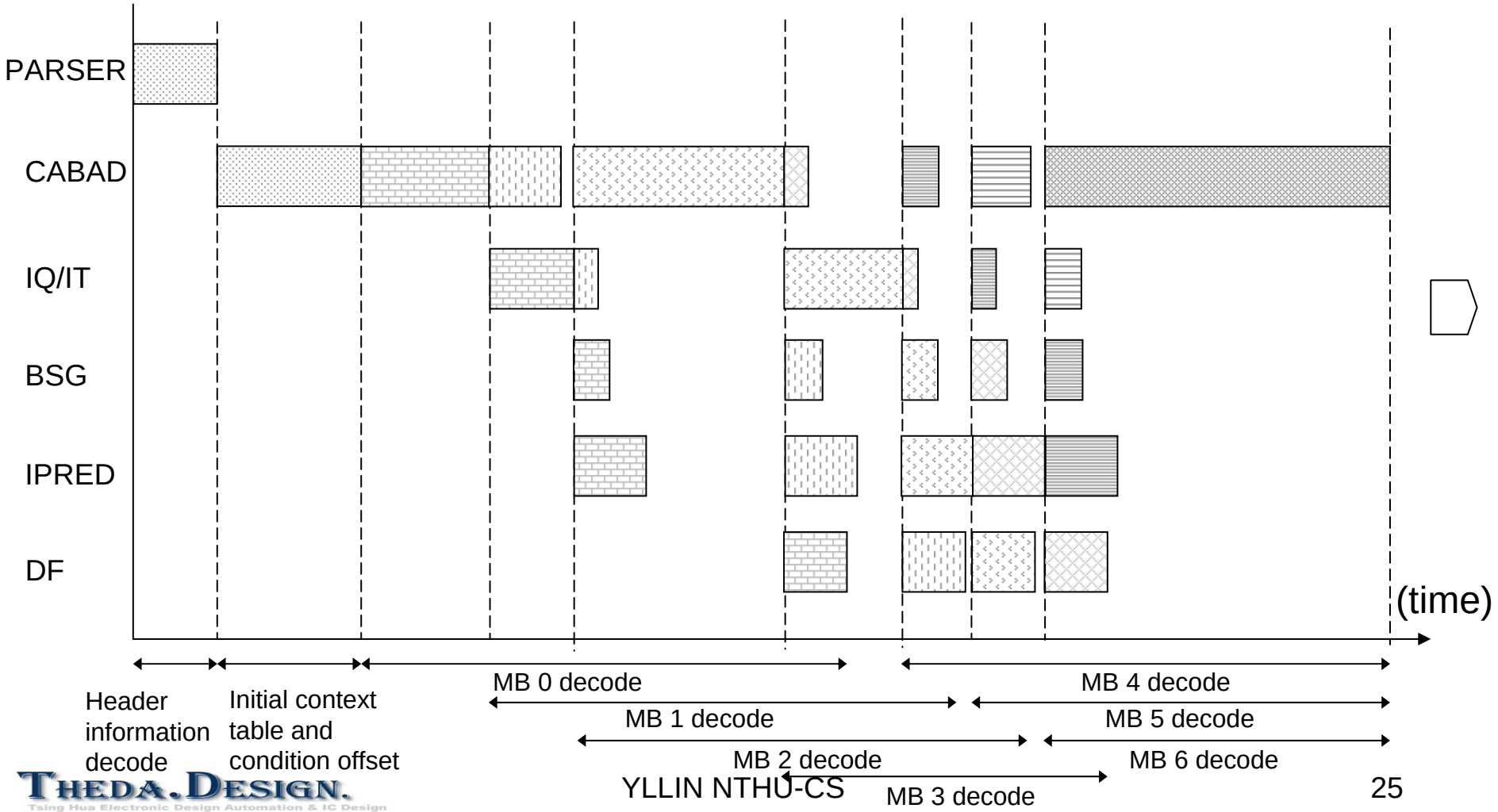
System-Level Optimization

Cyclic-Queue-Based IP Interface

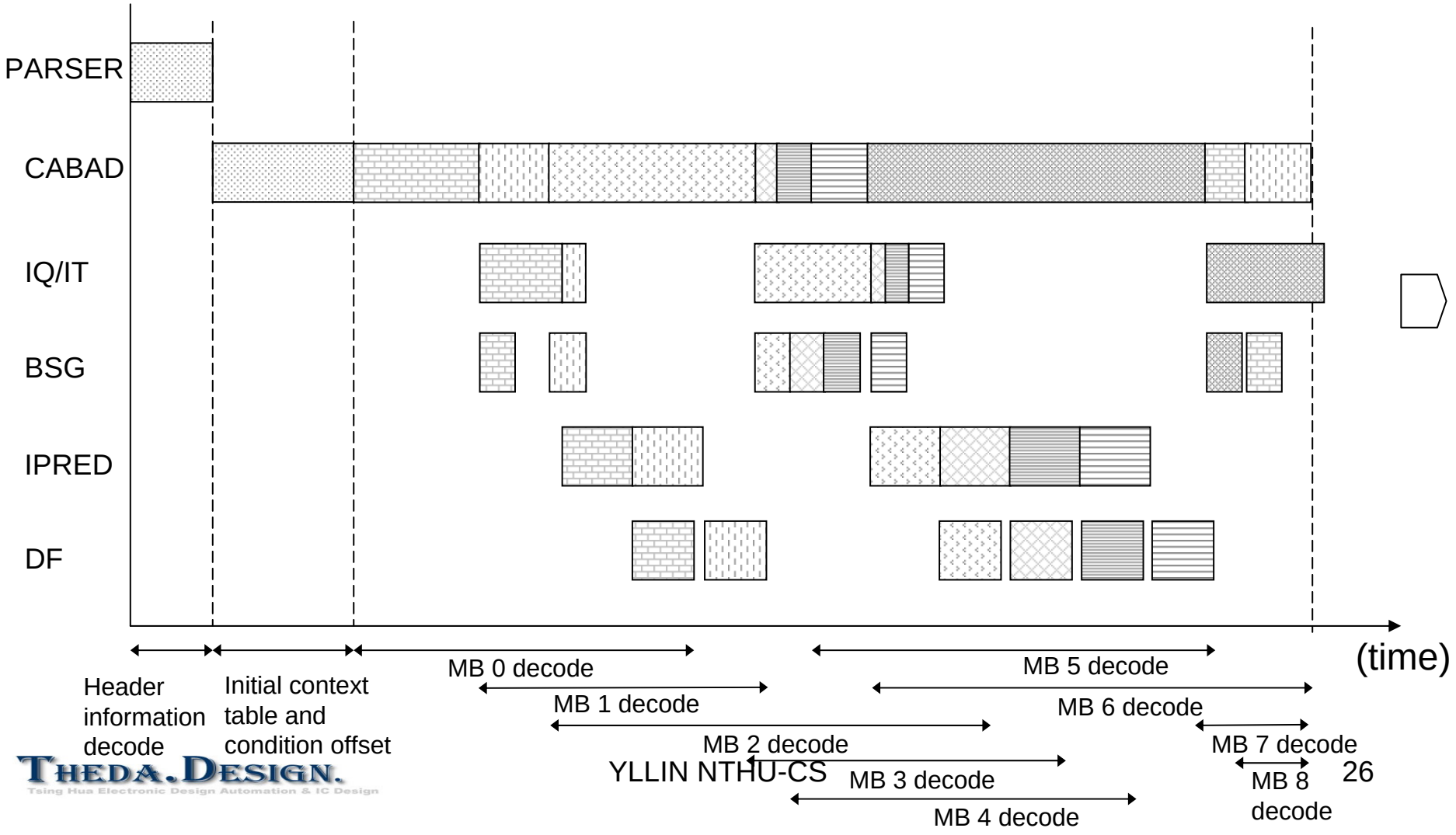
Sequential Decoder Timing Diagram (I Frame)



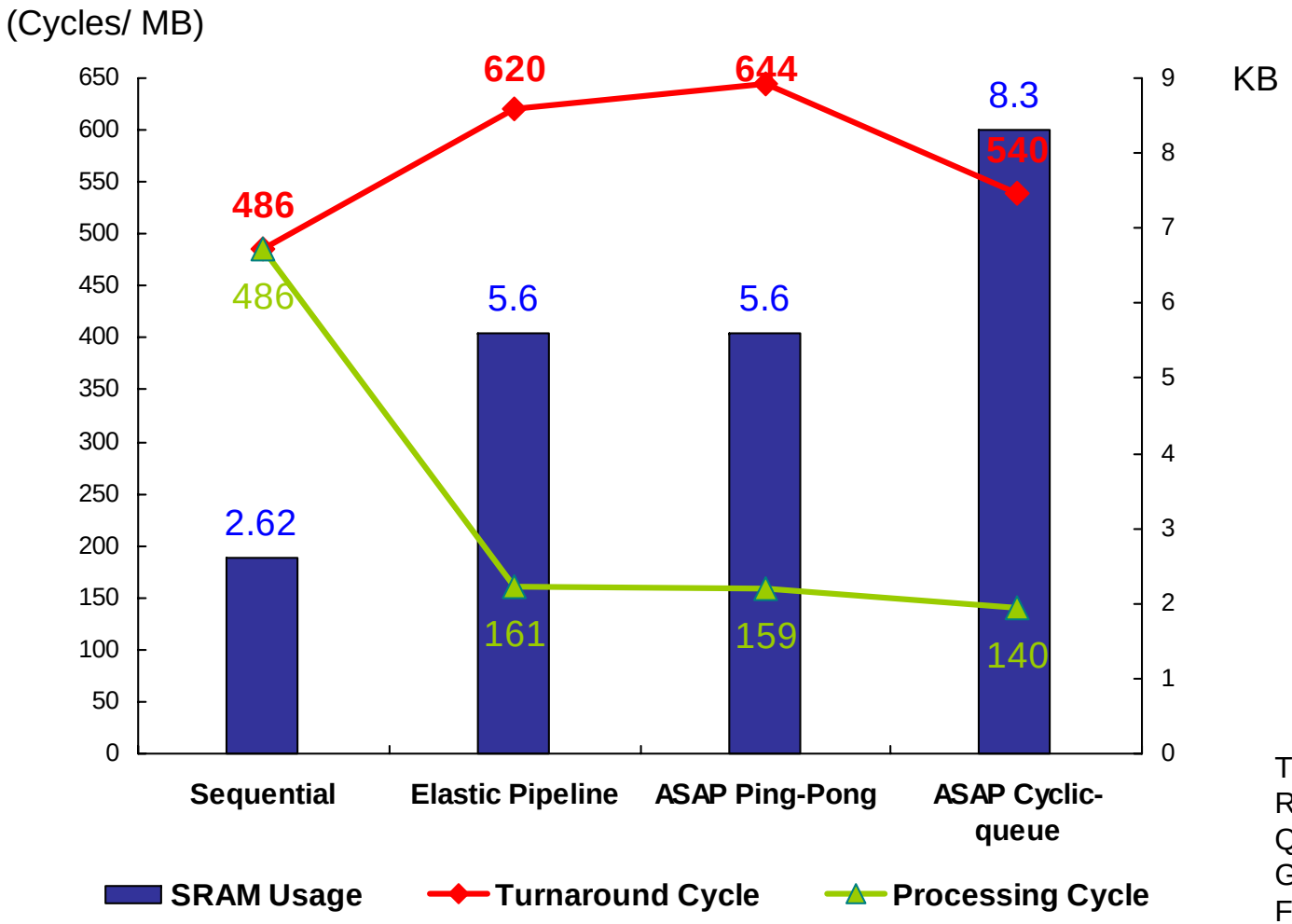
Elastic Pipeline Decoder Timing Diagram (I Frame)



ASAP Decode with Cyclic Queue Timing Diagram (I frame)

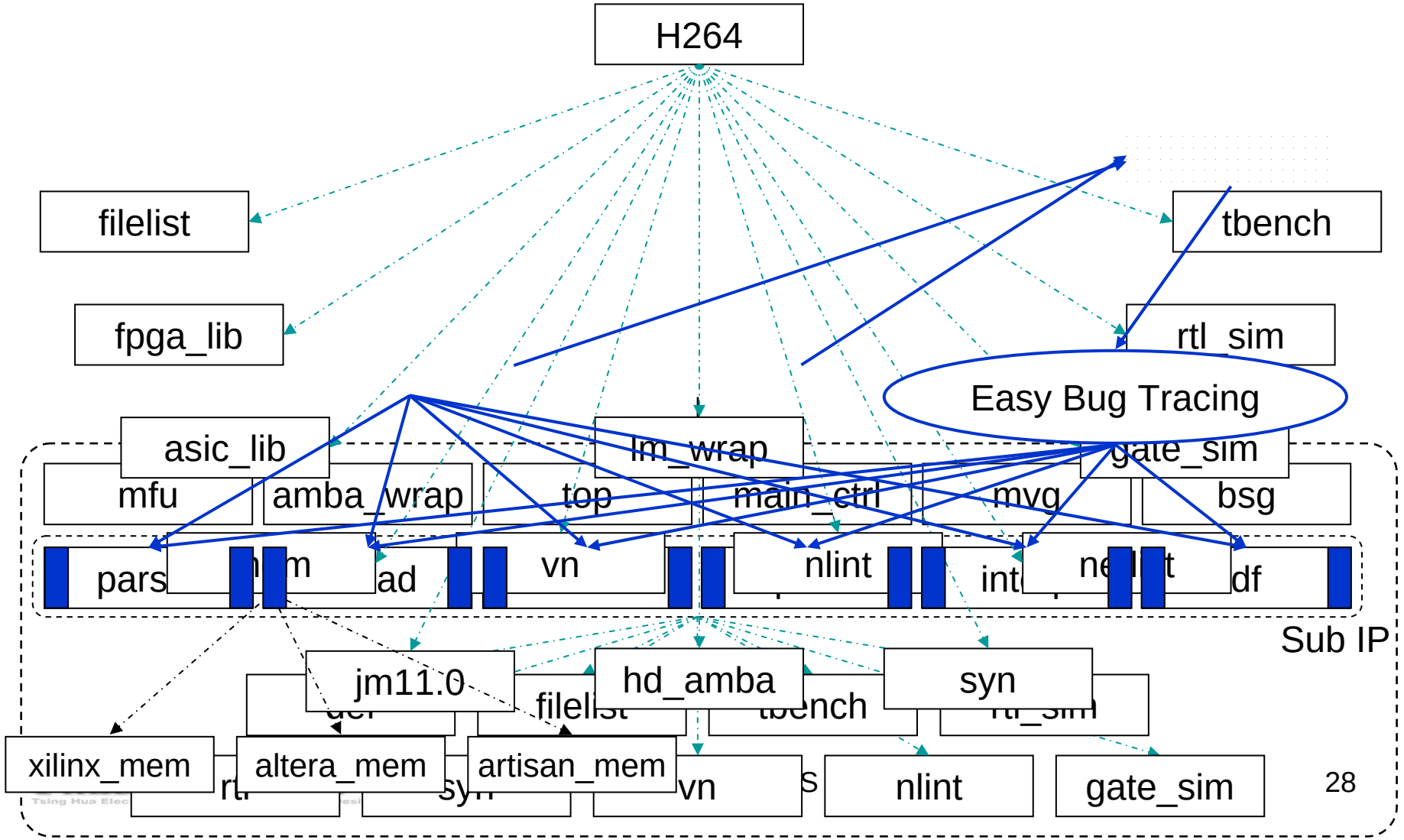


Comparison of Different Scheduling Methods

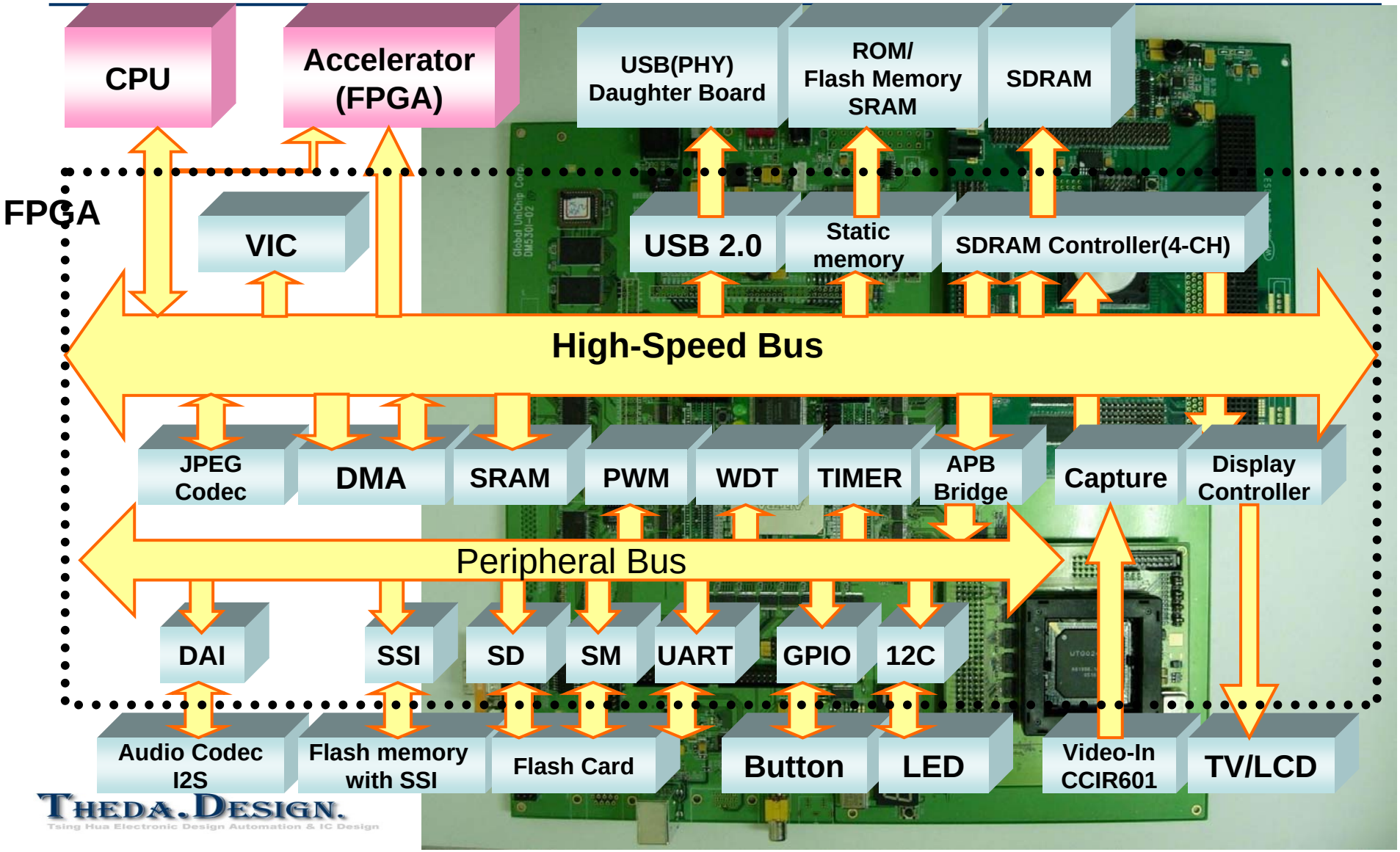


Test Pattern: “pedestrian”
Resolution: 720*480
QP: 28
GOP: III…
Frame #: 30

Verification Environment



A Multimedia SOC Platform



Summary

- Super High Definition Video Capturing, Delivery and Display are on the Horizon
- Massive Parallelism is Essential for Making Consumer Applications Possible
- Tradeoff Among Memory Usage, Bandwidth and Logic Has Profound Impact on the Overall System Performance
- System Design Should Be Adaptable to Content, Quality Variation