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Leading Innovation

# MPSoC Architecture Trade-offs for Multimedia Applications

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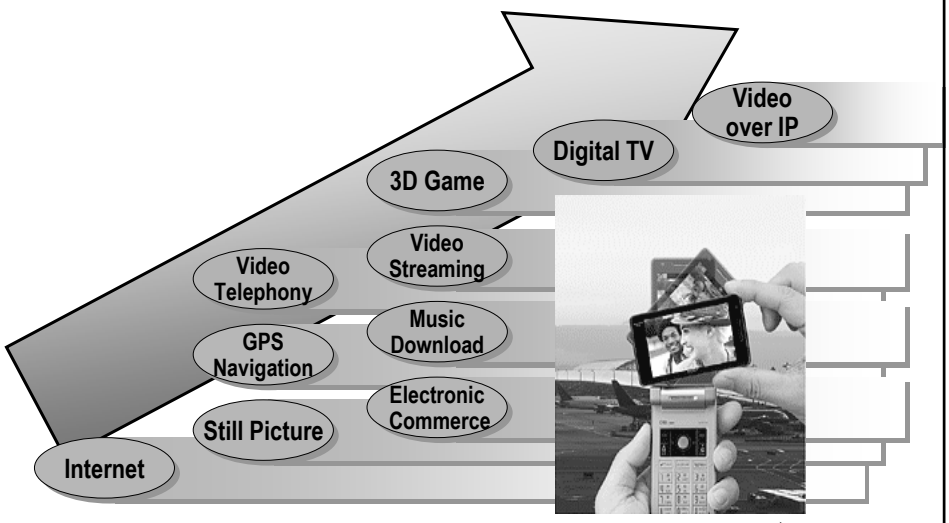
## Cellular Phone Application Trend



## MPSoC Components

- **M: Main CPU**

  Ex. ARM, MIPS, PowerPC, x86, etc.

- **D: DSP (Media Processor)**
  - Especially designed for media processing (Programmability and good cost-performance)
  - 64 or 128-bit datapath with SIMD instructions

  Ex. Cell SPE, TI C64x+, Philips TM3260, ST MMDSP+, configurable processor with extended instructions, etc.

- **A: Accelerator**
  - Highly parallel architecture
    - Reconfigurable processor, SIMD processor

  Ex. NEC DRP, IMAPCAR, IMEC ADRES, etc

- **H: Programmable Hardware Engines**
  - Specific hardware engines controlled by a small processors

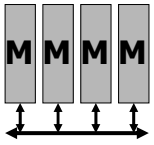
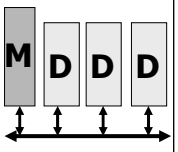
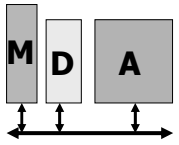
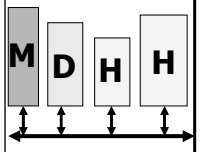
  Ex. Configurable processor with hardware engines

- **（Dedicated Hardware Module）**

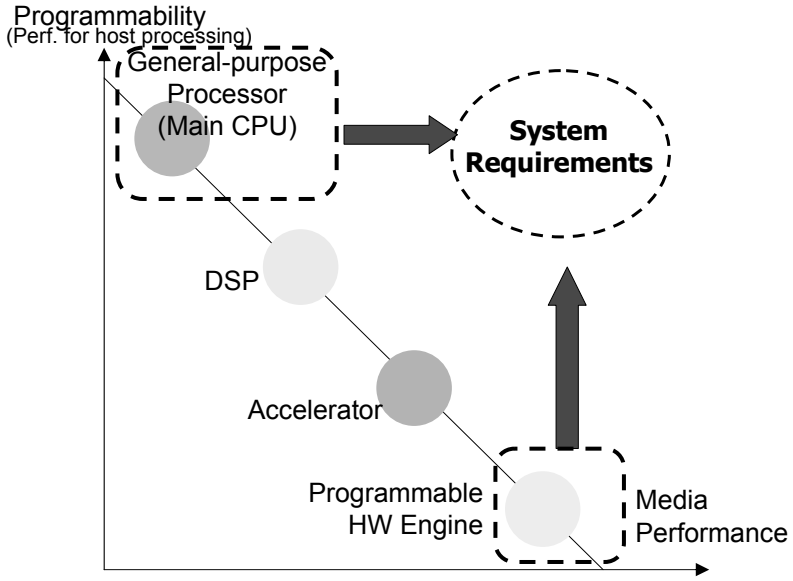
  Ex. JPEG, MPEG-2, etc.



## Homogeneous vs. Heterogeneous

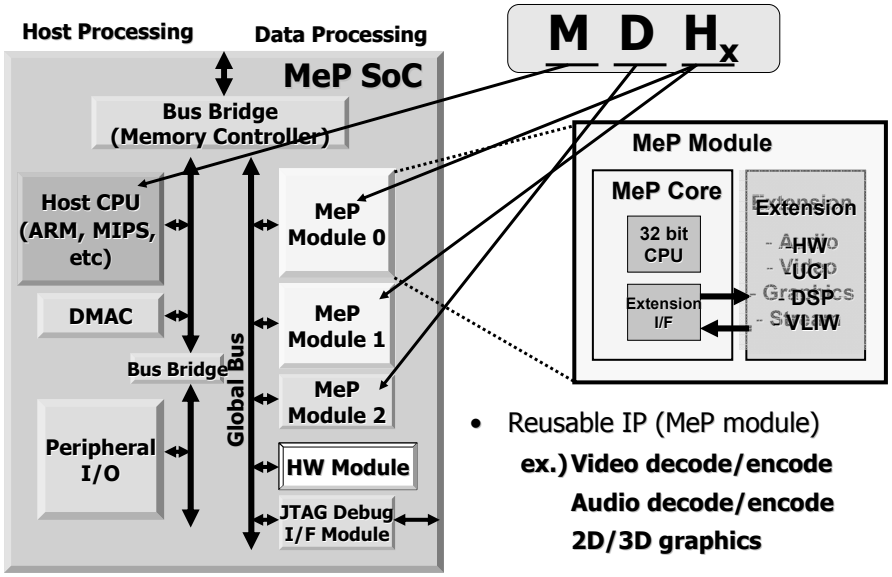
| | Homogeneous | Heterogeneous | | |
|---|---|---|---|---|
| **Architecture** | **Mx** | **MDx** | **MDA** | **MDHx** |
| |  |  |  |  |
| **Programmability / Scalability** | Very good → Good → Fair | | | |
| **Perf./Cost or Perf./Power** | Fair → Good → Very Good | | | |
| **Examples** | Core 2 ($M_2$, $M_4$), Xbox 360 CPU ($M_3$), MPCore($M_4$), Niagara($M_8$) | Cell ($MD_8$), SB3000(MD4), Philips Cake/Wasabi | Uniphier | Most of current SoCs |

# Architecture Trade-off



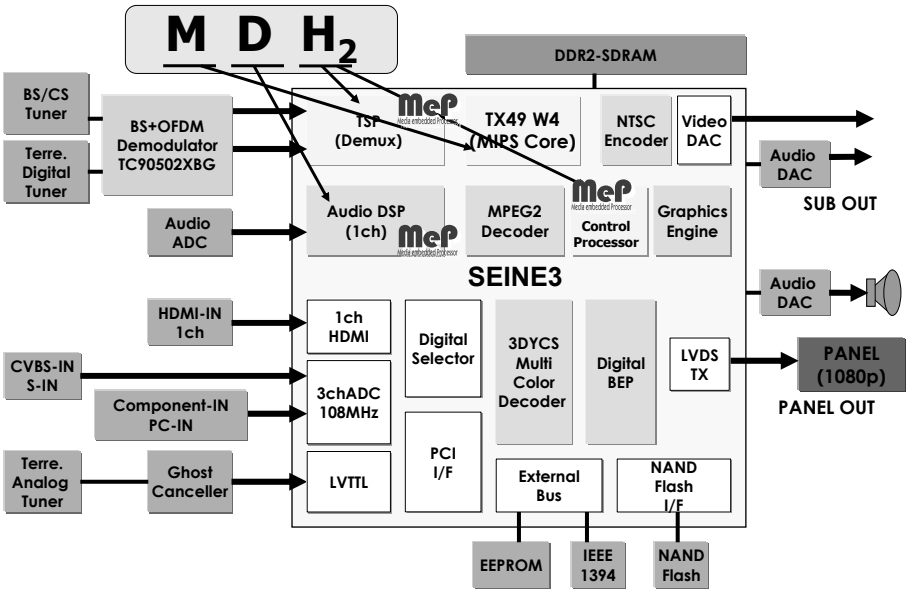



# SoC Platform based on Configurable Processor
## — MDH Type




- Reusable IP (MeP module)
  **ex.) Video decode/encode**
  **Audio decode/encode**
  **2D/3D graphics**

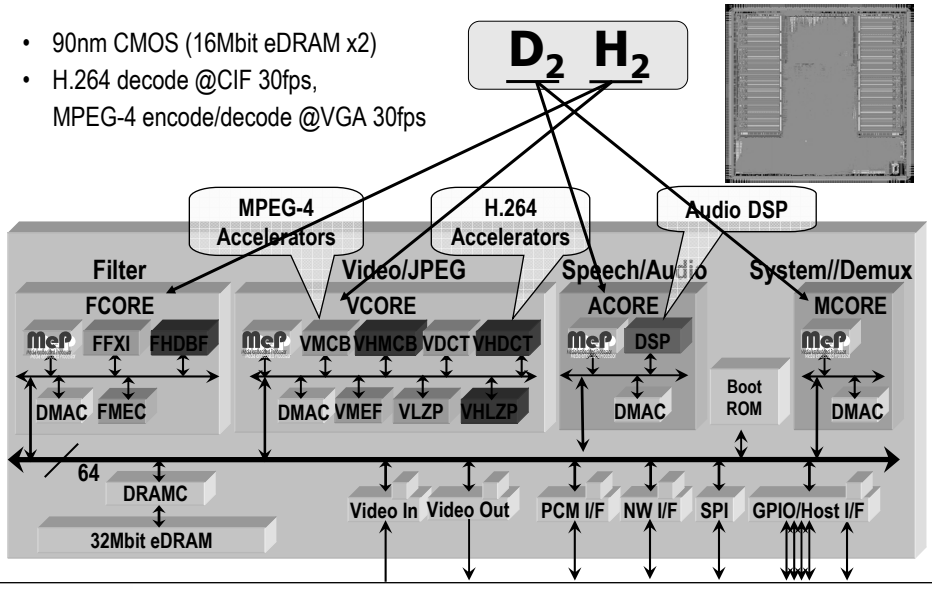
## “Seine3” SoC for HDTV



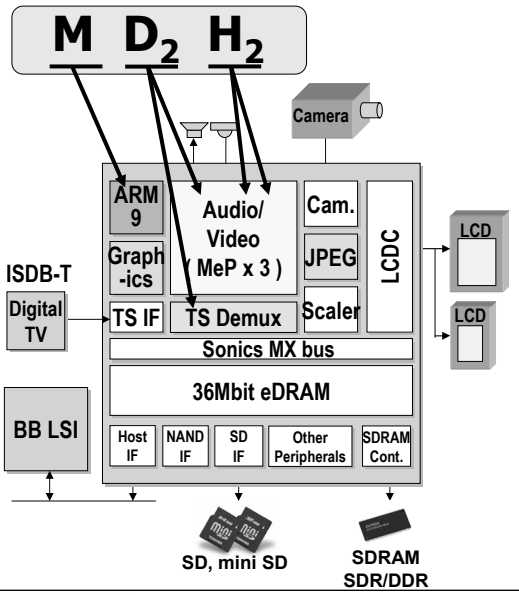


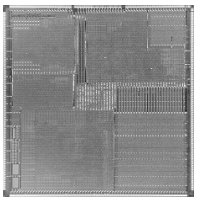

## “T5V” Mobile MM Engine (ISSCC 2005)

- 90nm CMOS (16Mbit eDRAM x2)
- H.264 decode @CIF 30fps, MPEG-4 encode/decode @VGA 30fps



## “T5G”=“T5V”+ARM+GFX



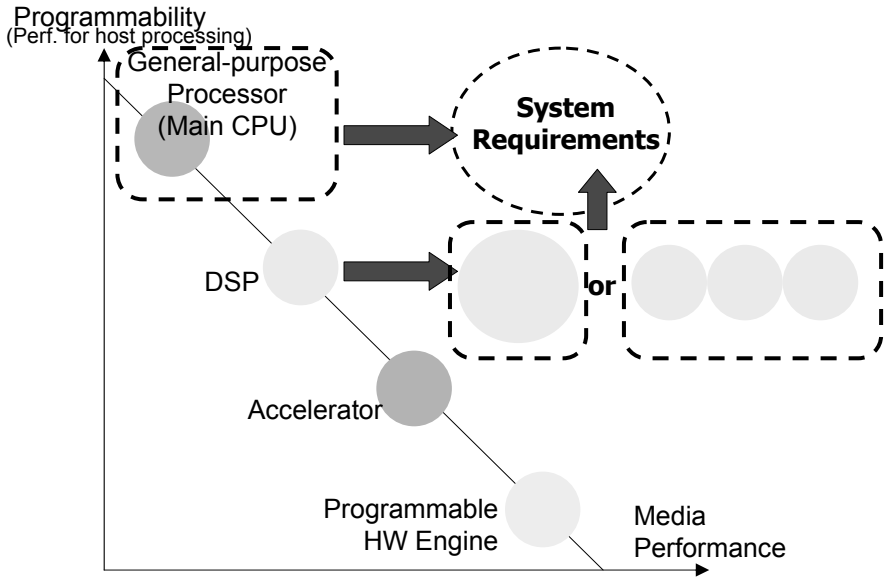



***Feature Topics***

- **MPEG4: VGA 30fps enc./dec.**
- **H.264: CIF 30fps dec.**
- **Audio: MP3, AAC enc./dec.**
- **Speech: AMR enc./dec.**
- **JPEG: 2M pixels**
- **2D/3D graphics accelerator**
- **LCD controller • Camera I/F**
- **NAND I/F • SDIO • SDRAMC**



## SW Solution for Media Processing

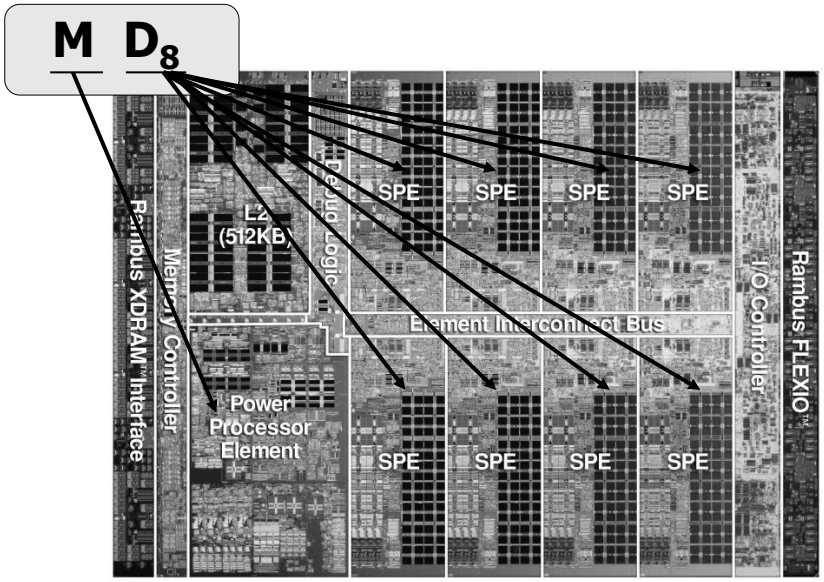


# Demands of SW Solution

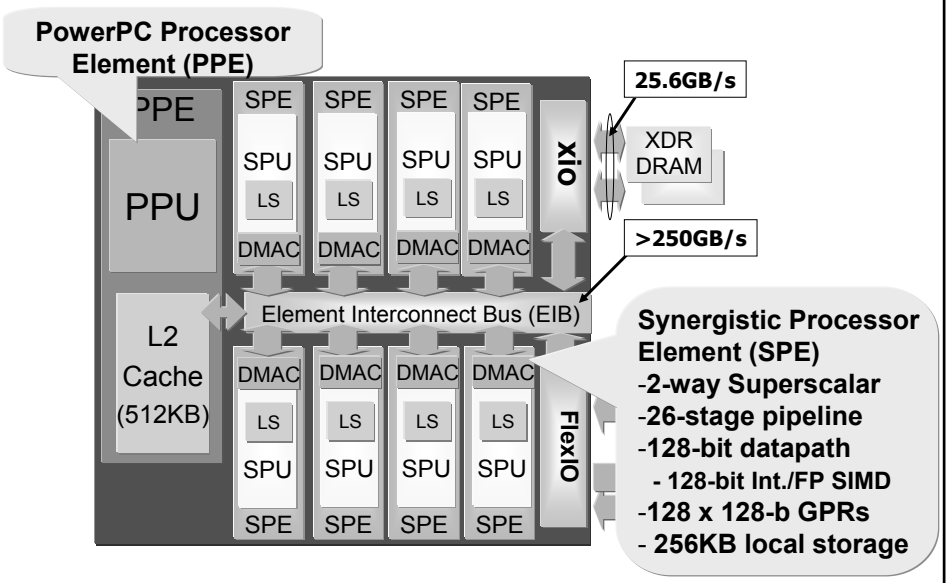
- **Support Multiple CODEC**
  - MPEG-2, MPEG-4, H.264, WMV, etc.
  - Decode, encode, and transcode
- **Scalability**
  - QVGA → VGA, WVGA, D1 → 720p → 1080i → 1080p
  - Multi-stream processing
- **New Applications**
  - Image recognition
  - High-quality video technology
    - Frame interpolation, etc.



# Example of MDx type: Cell Broadband Engine

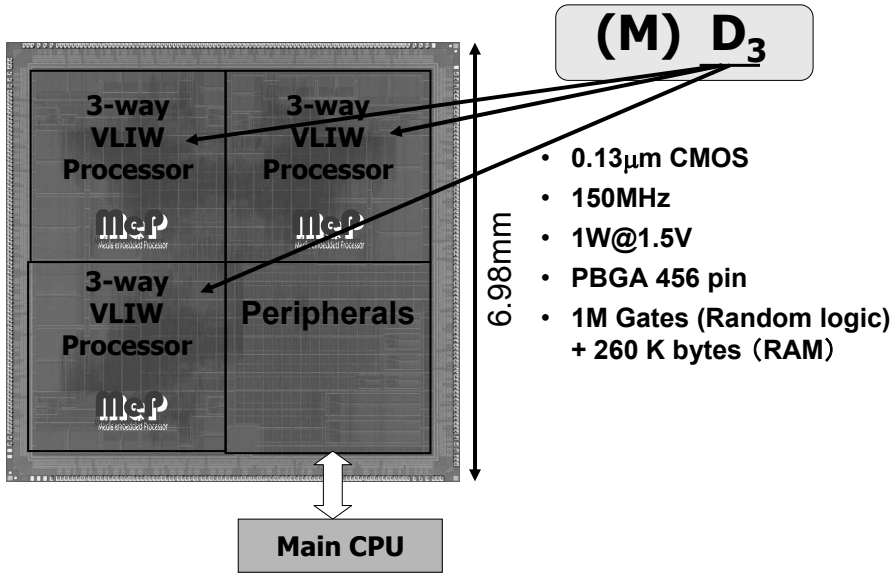


# Cell Architecture



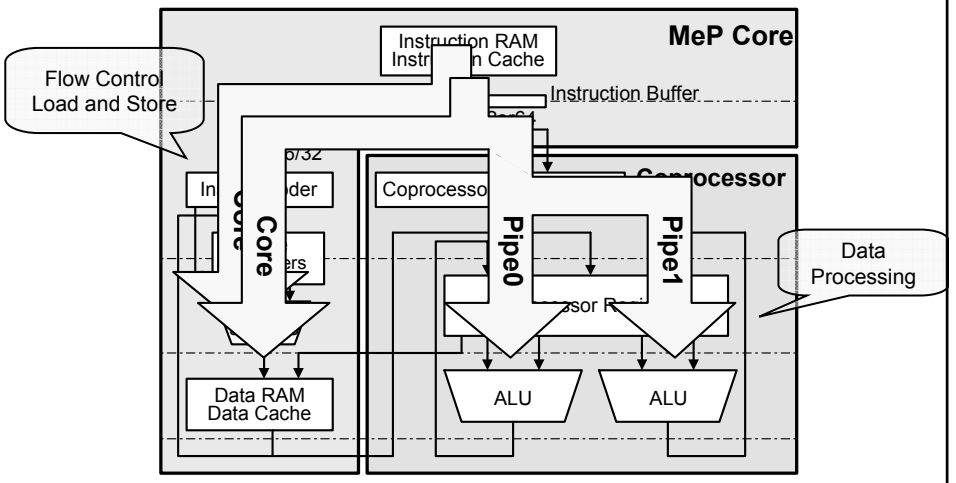



# Visconti: Image Recognition Processor (CICC 2003)



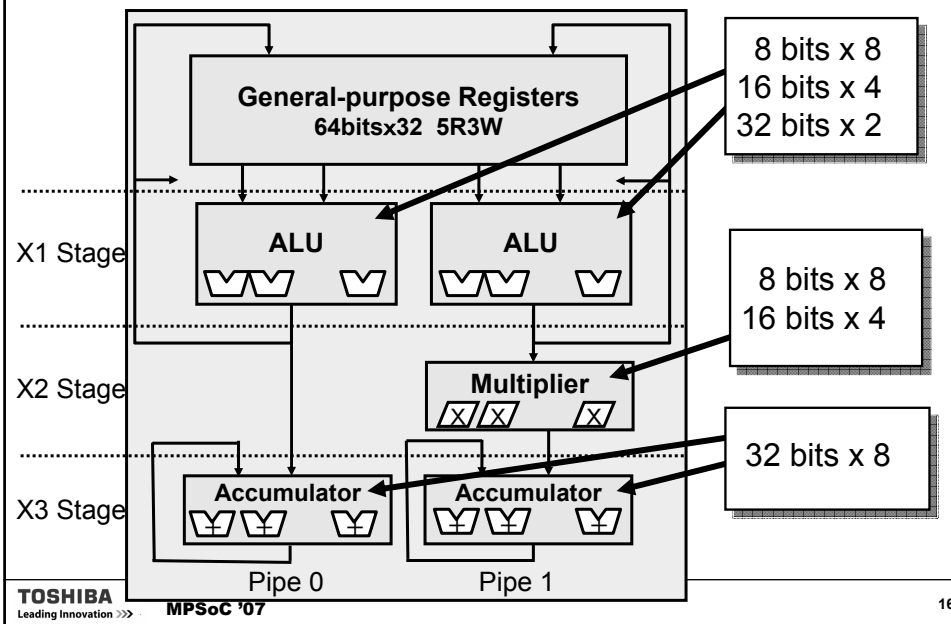
# 64-bit VLIW Coprocessor Extension

- **Core Mode**
  - 32-bit RISC processor
- **VLIW Mode**



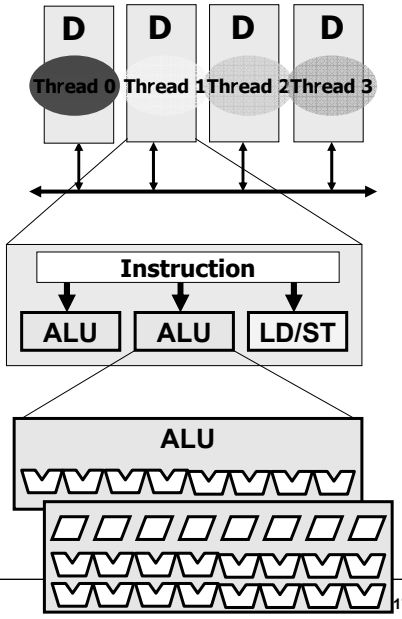



# 64-bit SIMD Datapath



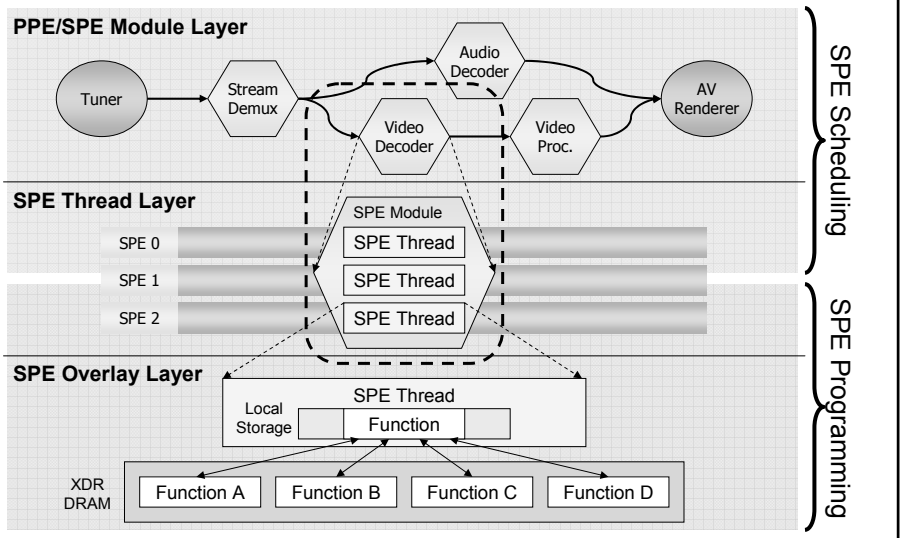
# Multi-grain Parallelism

- **TLP**
  **(Thread Level Parallelism)**
- **ILP**
  **(Instruction Level Parallelism)**
- **DLP (Data Level Parallelism)**
  **or Loop Level Parallelism**
  - SIMD instructions → Horizontal
  - Fused instructions → Vertical
  - Vector instructions



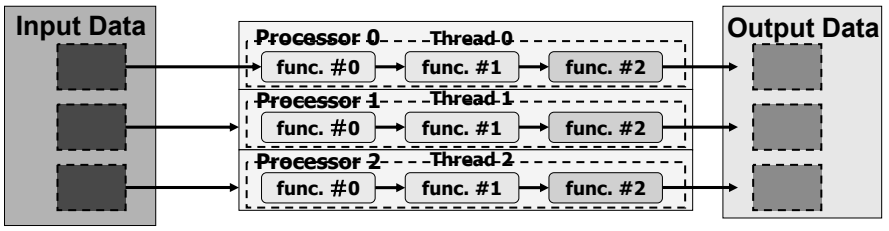



# Cell SPE Multi-layered Programming Model

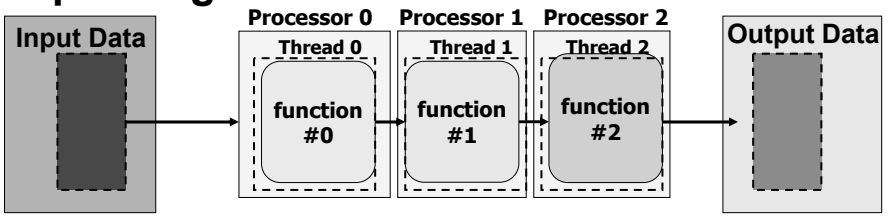


## Thread Parallelization Models

- **Data Parallel**

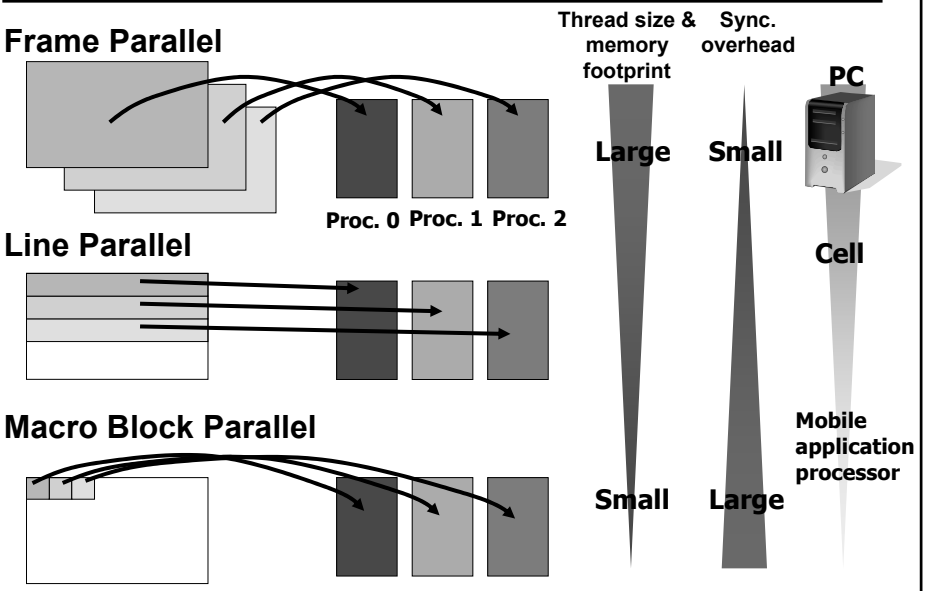



- **Pipelining**



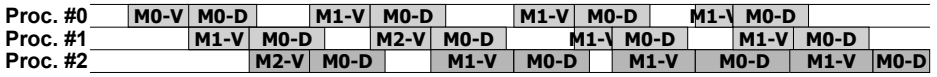



## Data Parallel Processing for Video CODEC



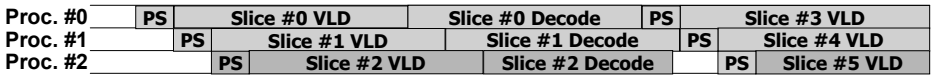
# Data Parallel Processing of MPEG-2 Decode

- **MB: Macro Block Parallel**




- **SL: Slice (Line) Parallel**

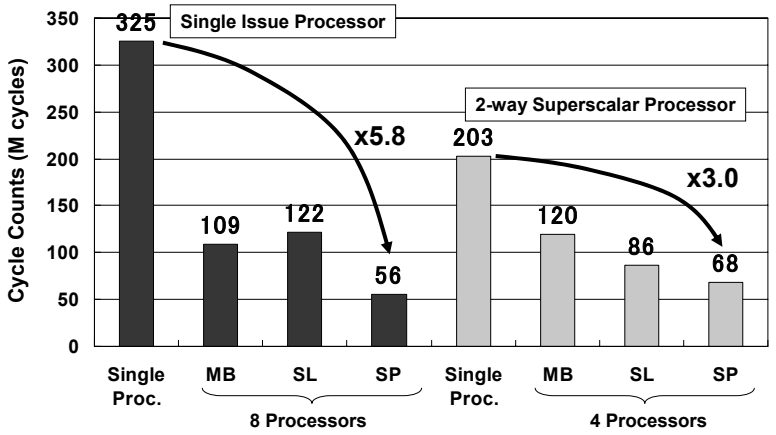

- **SP: Slice (Line) Parallel with Pre-scanning**





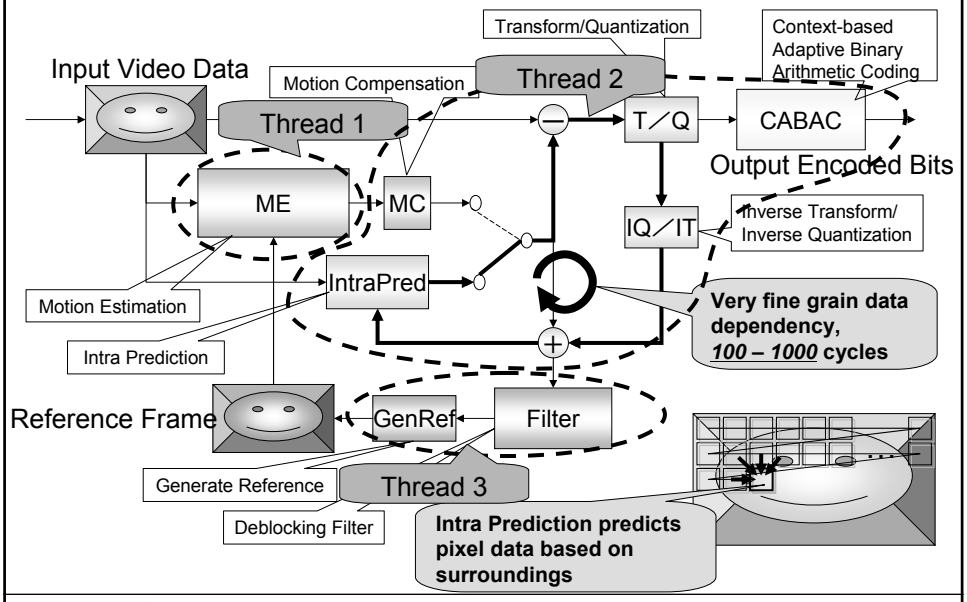

# Performance Comparison

**Parallel MPEG-2 Decoding, MP@ML 15 Frames**



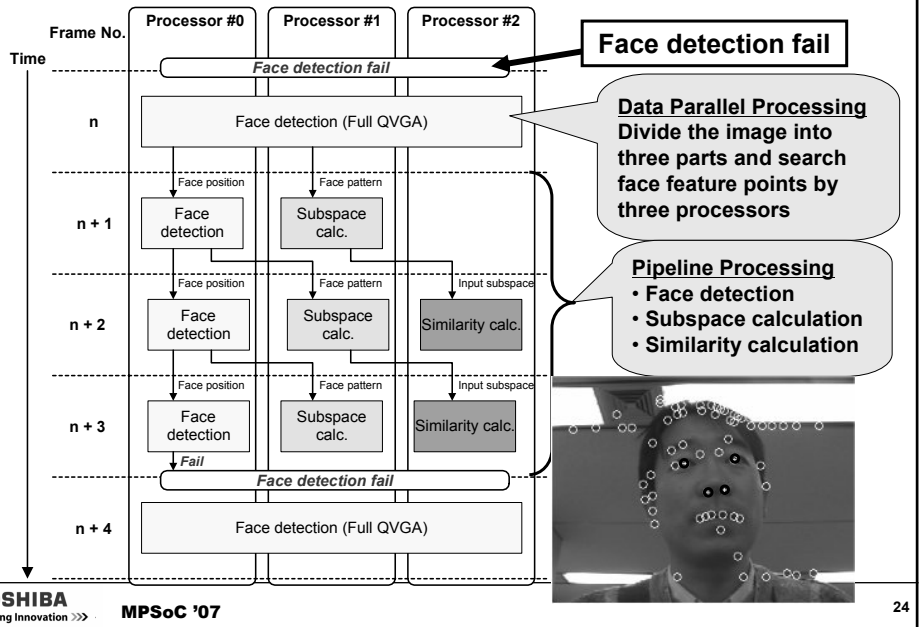

**Exploiting Coarse-Grain Parallelism in the MPEG-2 Algorithm**
**Eiji Iwata and Kunle Olukotun**
**Stanford University Computer Systems Lab Technical Report CSL-TR-98-771, September 1998.**

# H.264 Encode Thread Partitioning for Cell SPEs

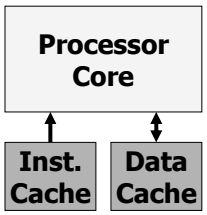
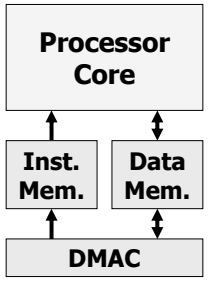





# Face Recognition Thread Partitioning for Visconti

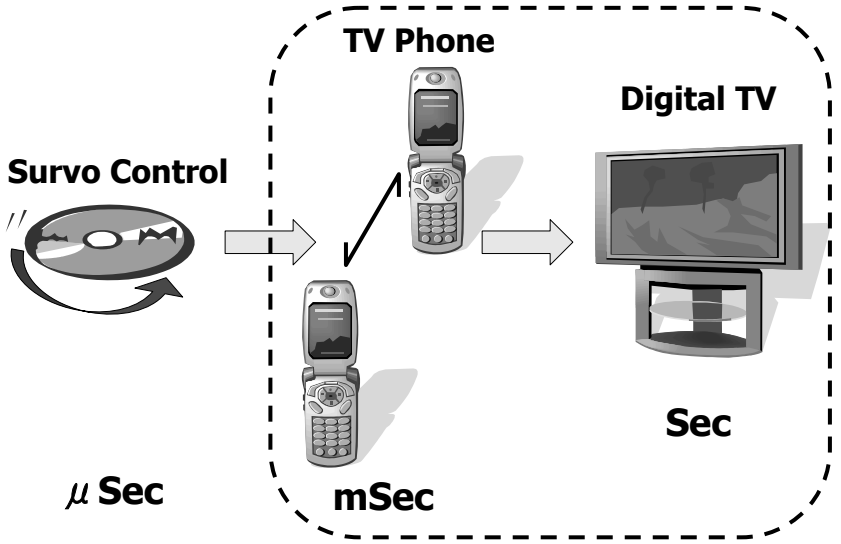


# Cache vs. Scratchpad Memory

| | Cache Memory | Scratchpad Memory |
|---|---|---|
| |  |  |
| Pros | + SW friendly<br>+ (Relatively) small area and power consumption | + Can be managed by program<br>→ good for real-time processing<br>+ Latency tolerant<br>+ Block transfer |
| Cons | - Pipeline stall due to cache miss | - Need overlay<br>→ Size of memory should be large! |

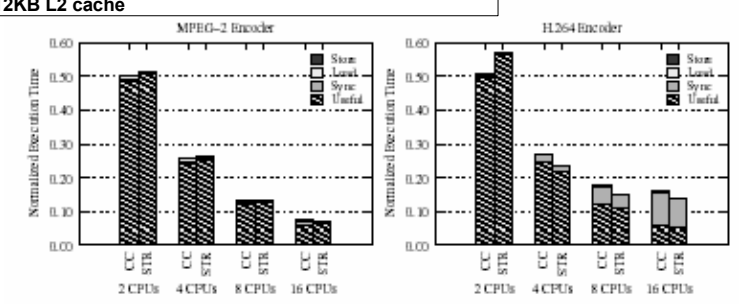


# Real-time Requirement for Multimedia Processing



## Comparing Memory Systems for Chip Multiprocessors
**(Stanford Univ., ISCA'07)**

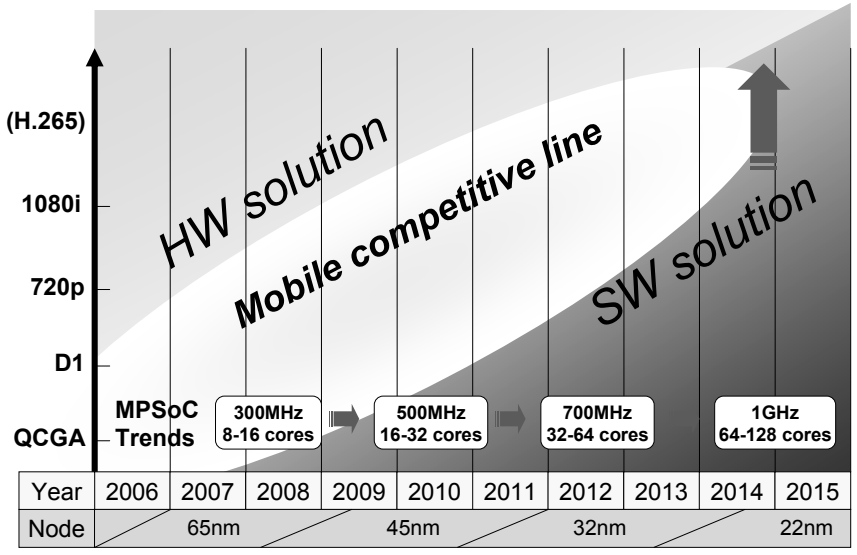
- **CC: Cache-Coherent Model**
  - 32KB 2-way assoc. cache
- **STR: Streaming Model**
  - 24KB local memory and 8KB 2-way assoc. cache
- **512KB L2 cache**



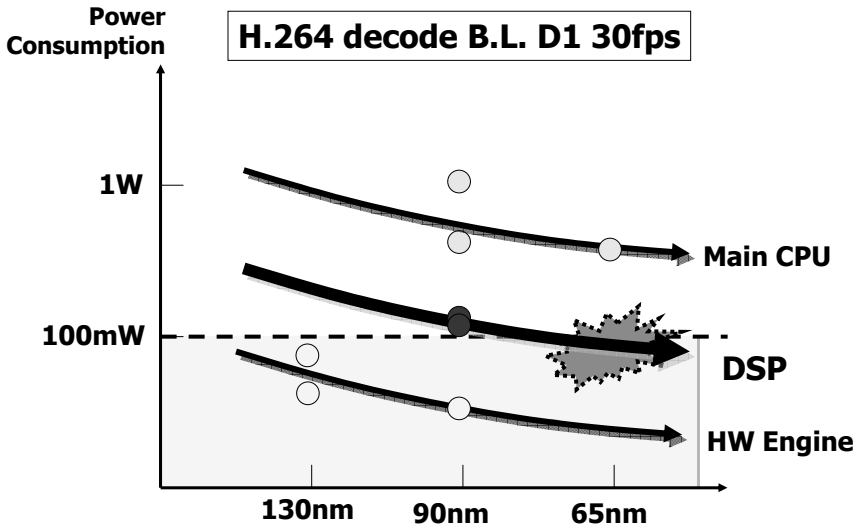

- **Both models perform and scale equally well.**
- **"Non-allocate store to cache" can reduce memory traffic.**
  - Ex. Prepare for Store (PFS) instruction of MIPS32
  - MPEG-2: Traffic due to write miss was reduced 56%.
- **Streaming programming model, such as blocking and locality-aware scheduling is efficient for cache model as well as streaming model.**



## Roadmap toward SW Solution

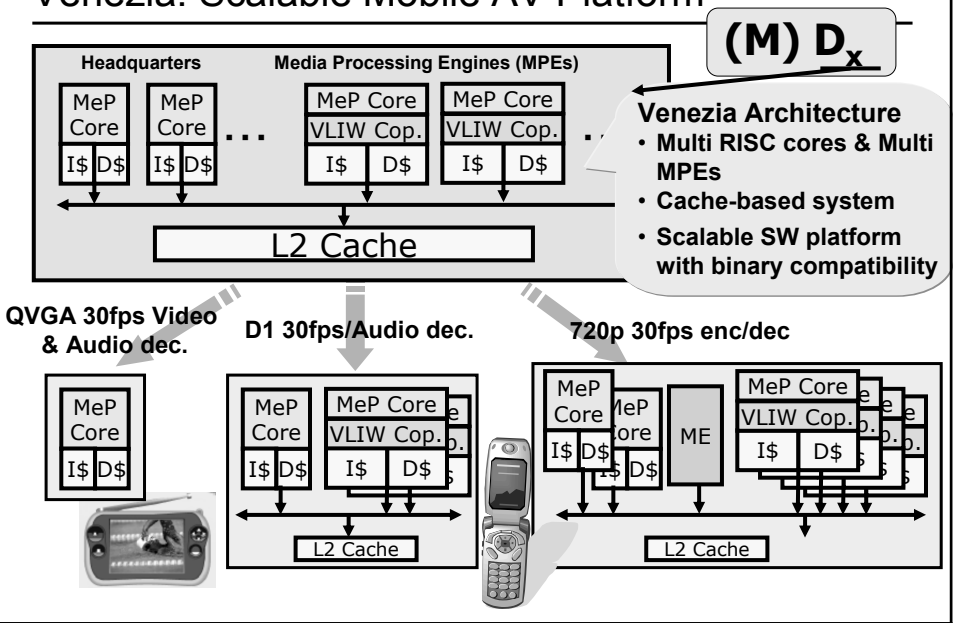


## HW Solution to SW Solution for Mobile Applications

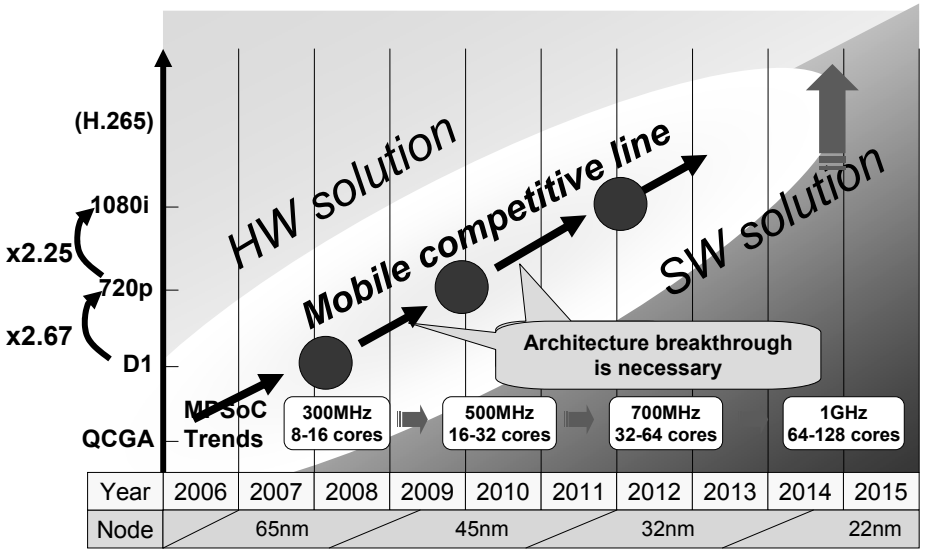





## Venezia: Scalable Mobile AV Platform

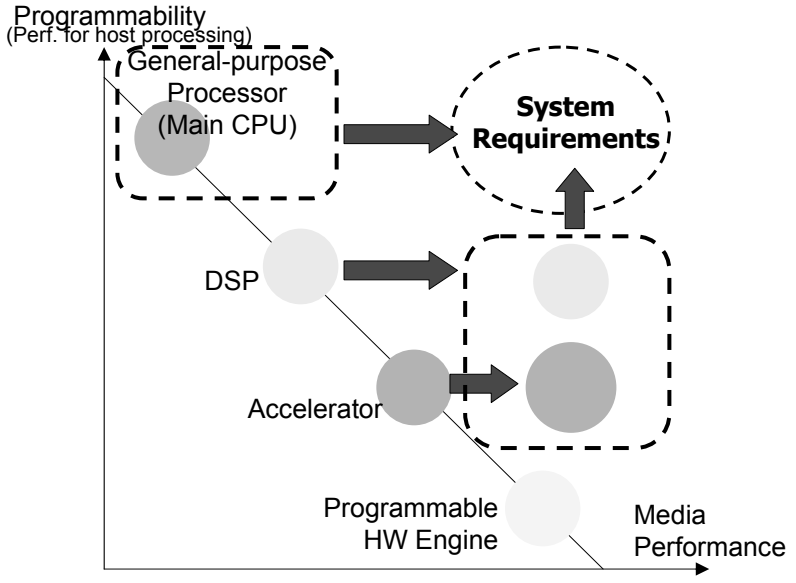


# Roadmap toward SW Solution

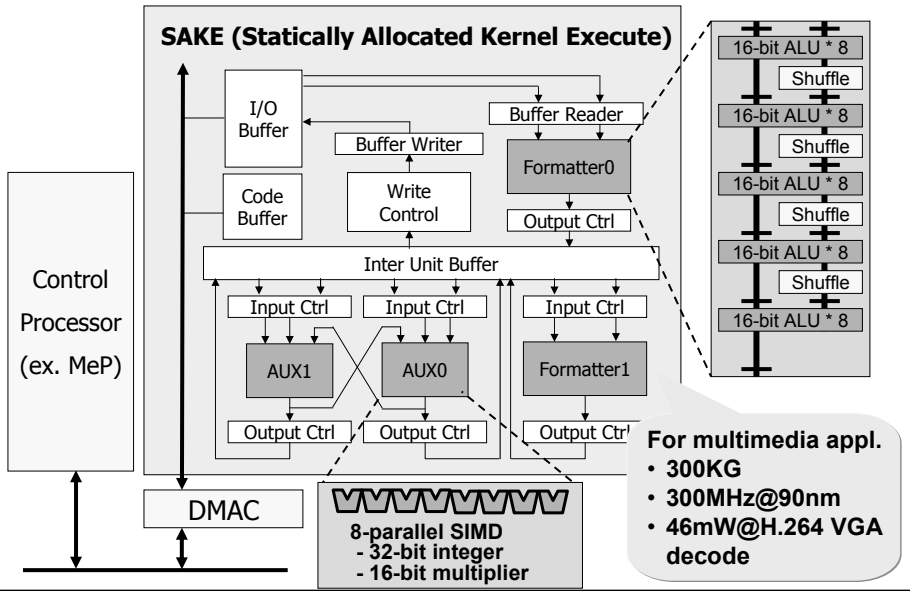





# SW Solution for Media Processing

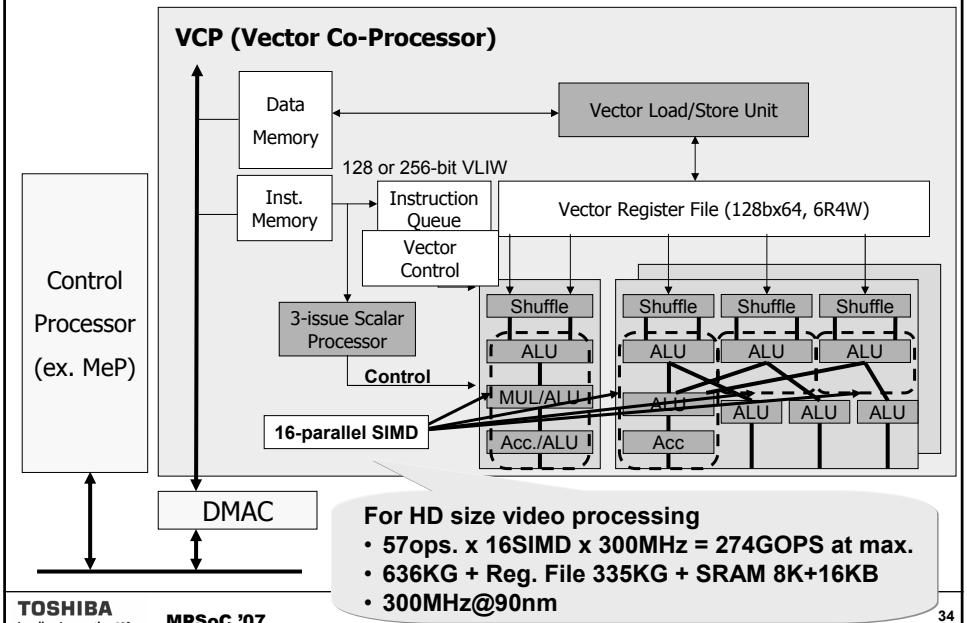


## Toshiba's Dynamically Reconfigurable Processor (Hot Chips '06)

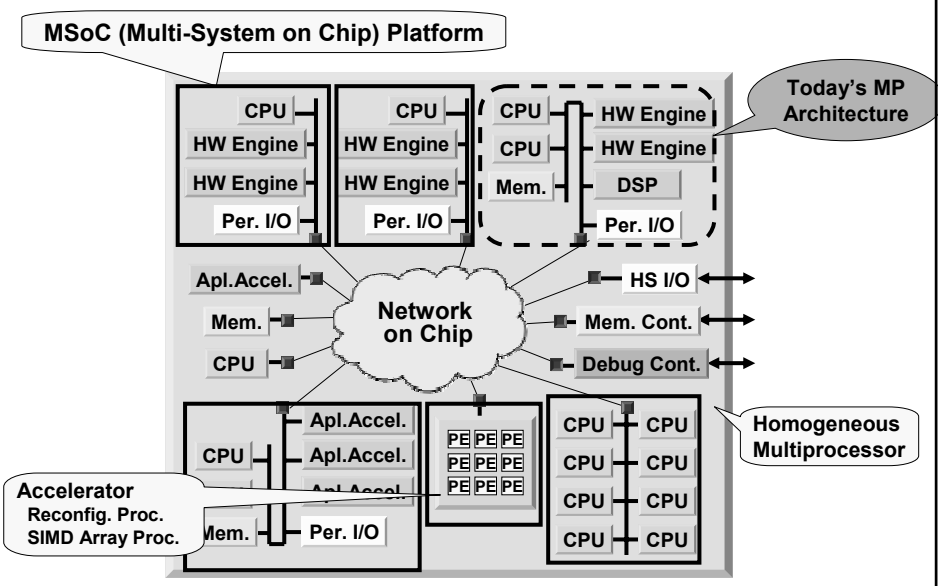





## Toshiba's Vector Processor: VCP



# Future MPSoC Architecture
## — More Than 1000 Processors on a Chip?






# Summary

- **Trend to SW solution for Video CODEC**
  - VGA, WVGA, D1 → HD
  - Scalable DSP platforms are required.
  - Multi-grain parallel execution
    - Thread parallelization is important. → • Compiler support • Thread scheduling method
- **Cache memory performs and scales well.**
  - SW friendly. Overlay is NOT needed.
  - (Or large scratchpad memory (ex. Cell SPE) )
- **Future MPSoC architecture for multimedia application**
  - Near future: Hybrid architecture of DSPs and **accelerators**.
  - Future: Homogeneous or Heterogeneous??