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Economics and Performance of Advanced SoC's

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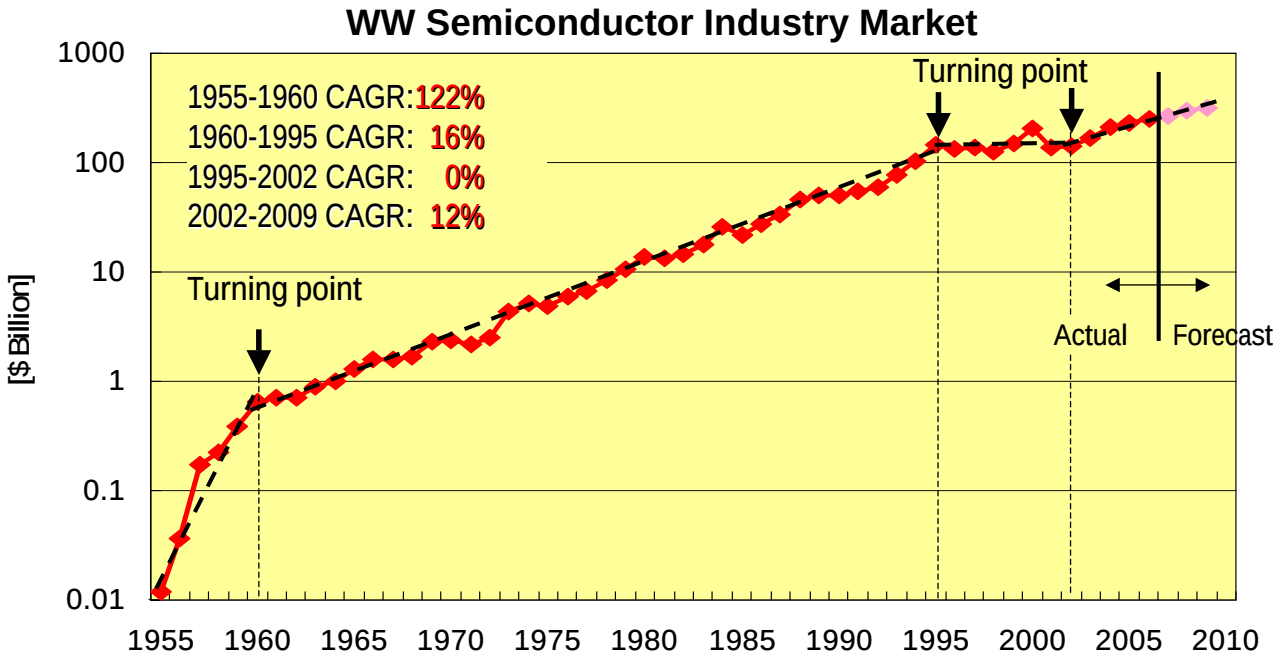
Outline

1. Improvements in economics and performance by scaling
2. Diminishing improvement rate in performance
3. Increased expenses for miniaturization and integration
4. Wafer production cost, process development cost, and design cost
5. Key to success - design cost reduction per chip -

Semiconductor Market Long-term Trend

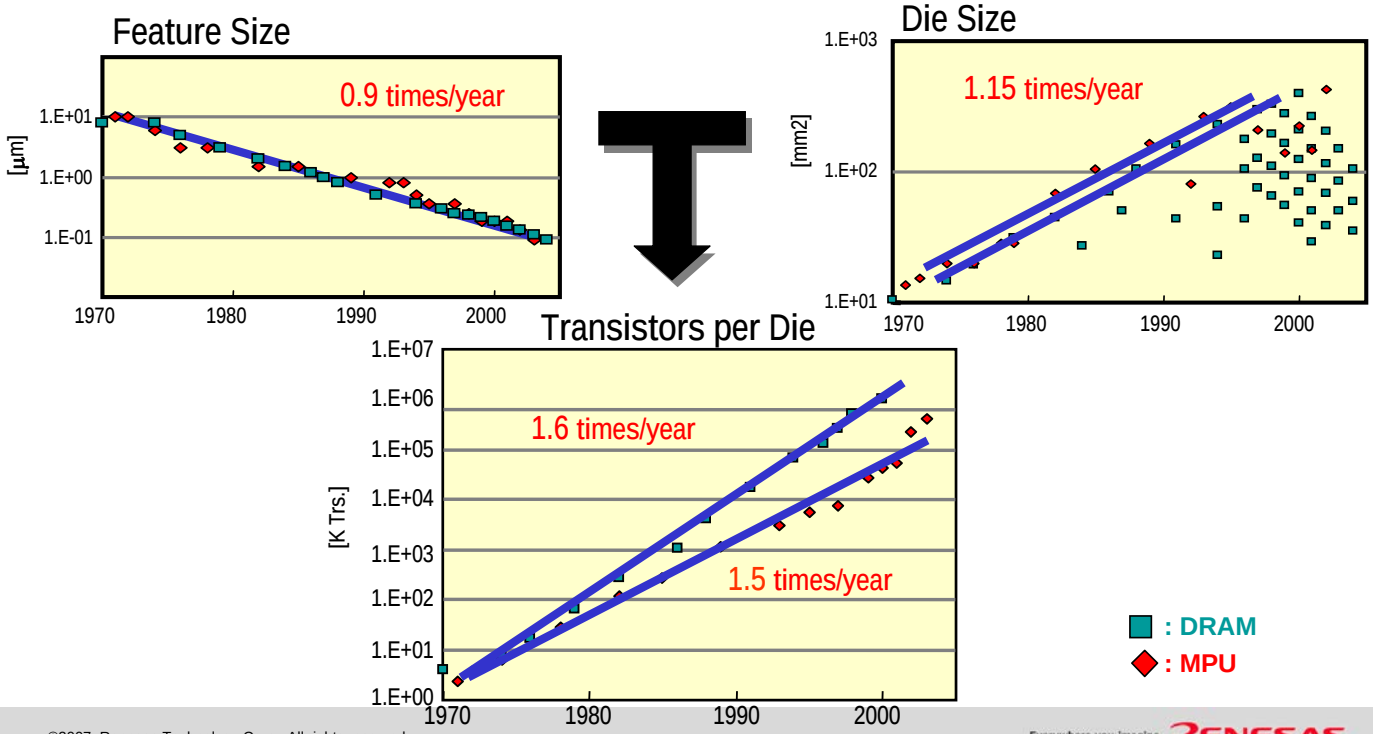
- Semiconductor Industry has expanded continuously from the 50's with the CAGR greater than 10% except from 1995 to 2002



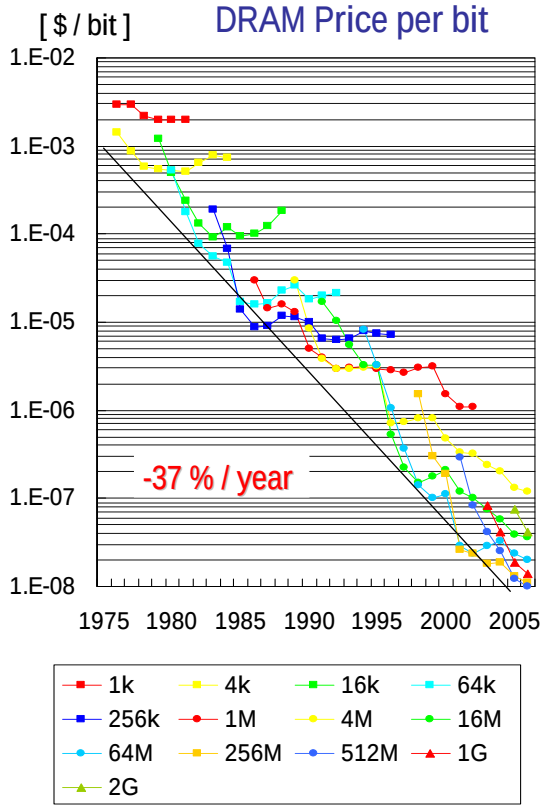
Source: SIA and WSTS

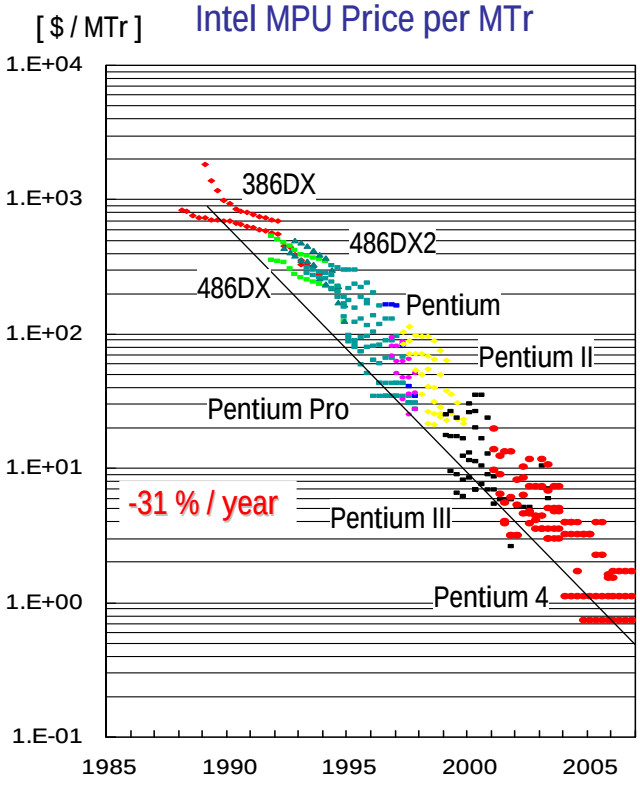
Integration Trends

- Exponential progress of "Transistors per Die" is caused by both "Feature Size" reduction and "Die Size" enlargement.



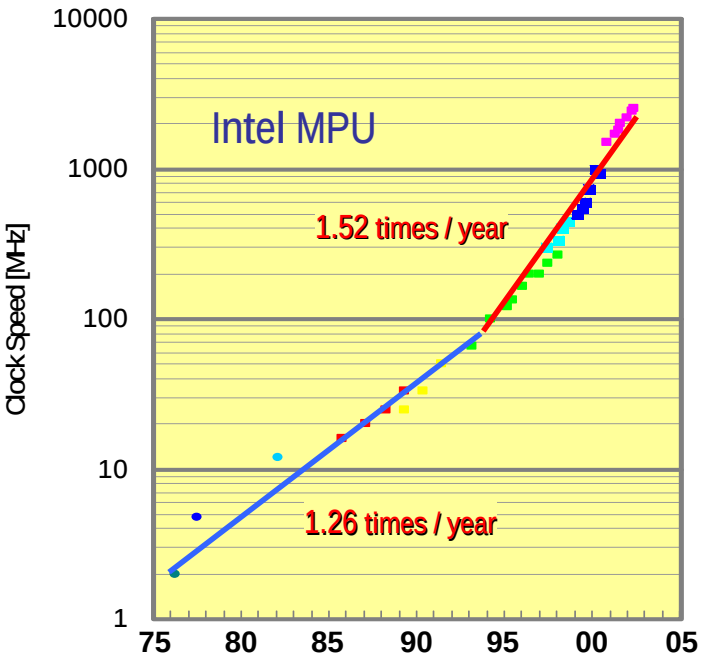
Improvement in Economics





Improvement in Performance

- Improvements in clock frequency has accelerated up to 2002.

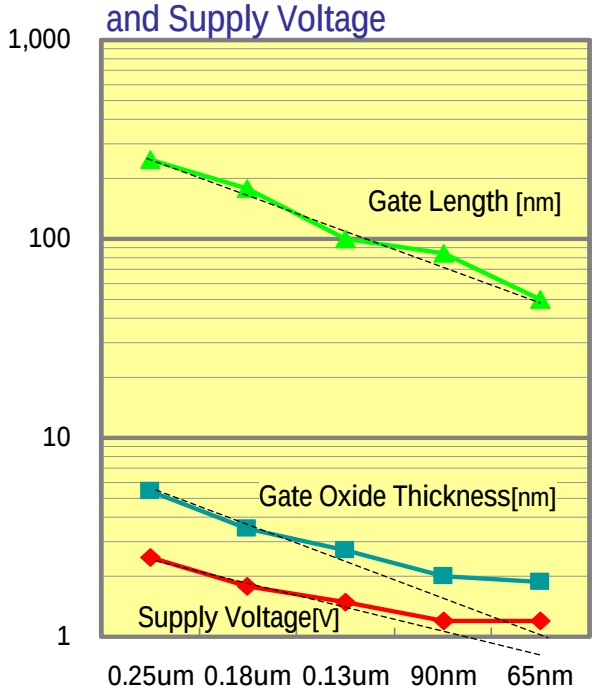


Source: Intel Publicized Company Information

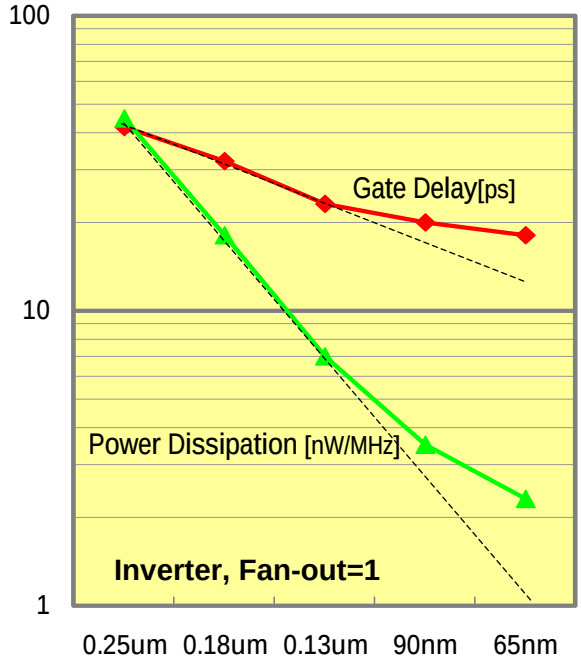
Diminishing Improvements in Performance

- Slowdown of improvement rate in performance from miniaturization

Trends in Transistor Dimensions and Supply Voltage

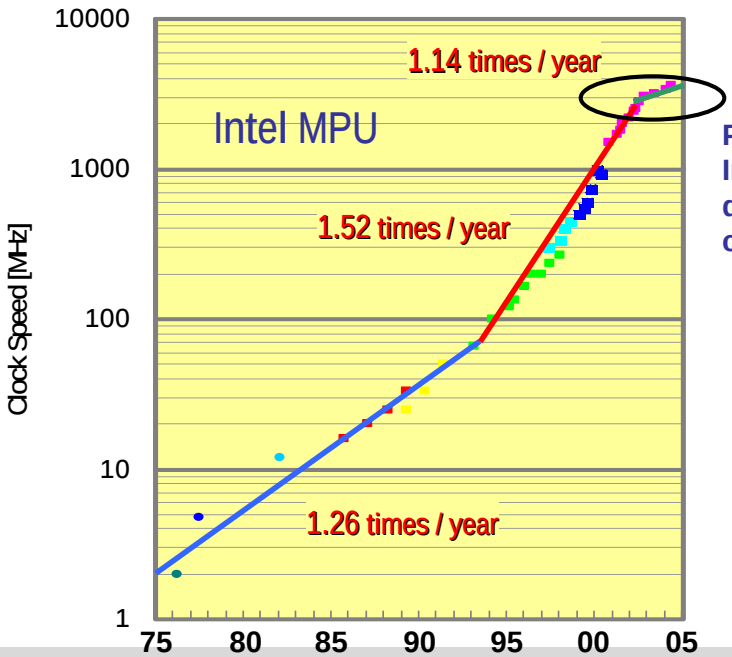


Trends in Transistor Performance



Diminishing Improvements in Clock Speed

- Improvements in clock frequency accelerated up to 2002.
- But, improvements diminished after 2002, and finally, ...



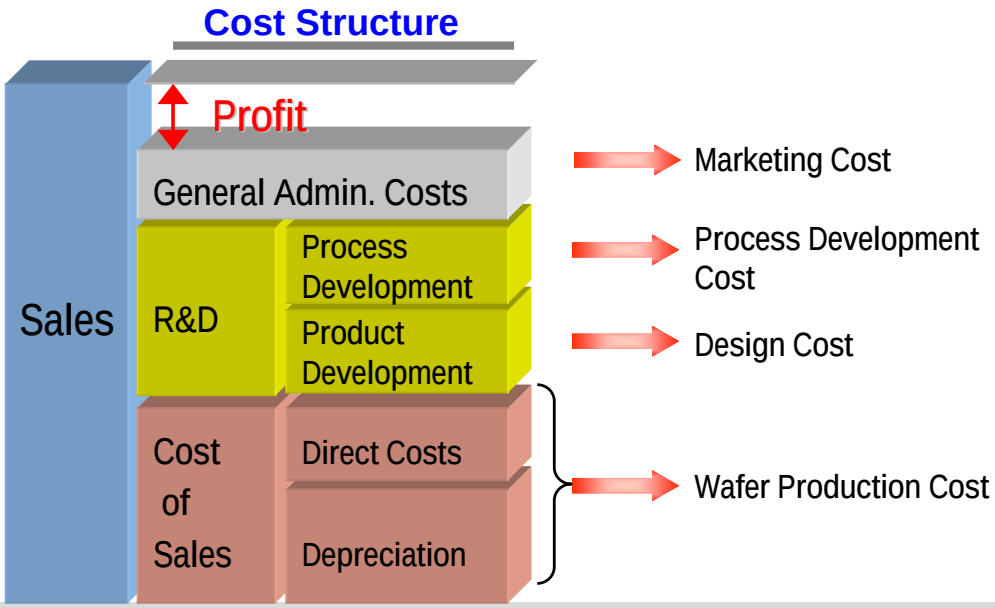
Diminishing Improvements

Public announcement from Intel that their 4GHz Pentium4 development has been cancelled (Nov., 2004)

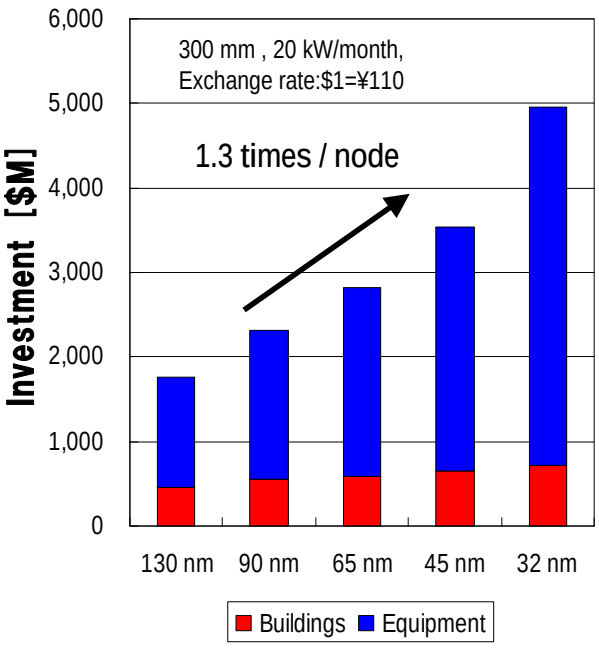
Source: Intel Publicized Company Information

Cost Structure of SoC's

- Increase in R&D and investment costs occurring simultaneously with increase in variety of product applications.
  - Made it a necessity for each firm to re-evaluate their business models reflecting their core competitiveness.



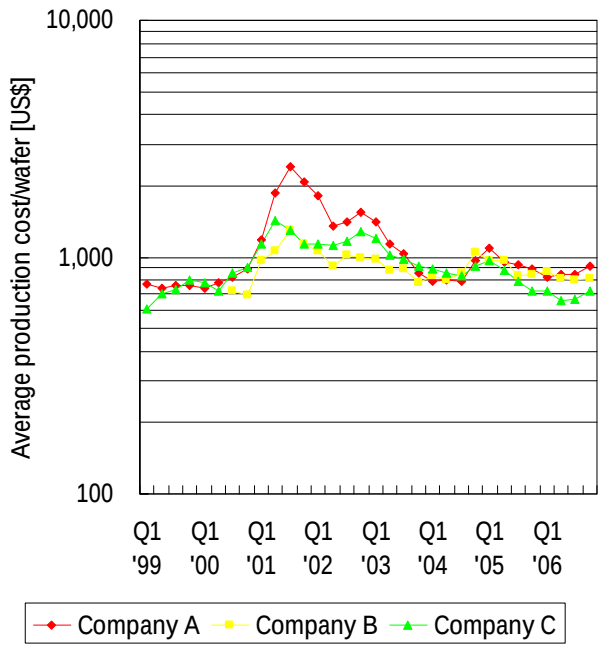
Investments in Fabrication Lines



- Investments in fabrication lines increase in terms of both buildings and equipment.
- Expense increases 1.3 times per technology node.

Source: SIRIJ

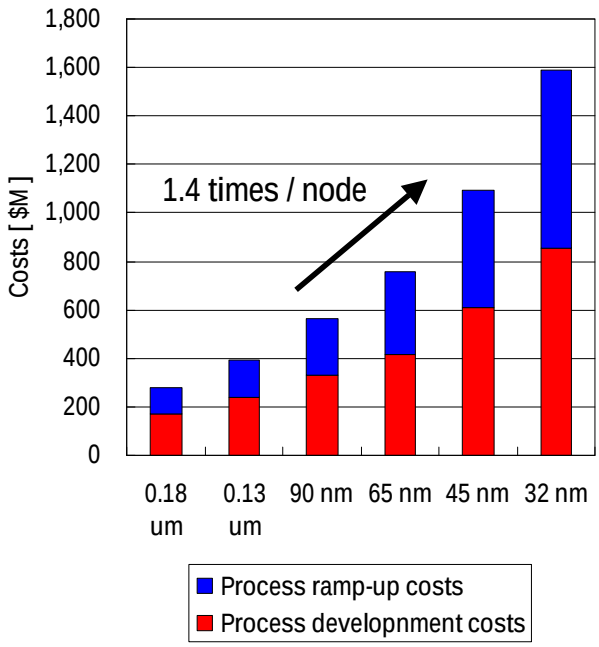
Average Wafer Production Cost
- 8 inch equivalent -



- Average production cost per wafer has been at the same level ($ 700 - $ 1300) for these past ten years though complexity of wafer production has increased.
  - Finer technology nodes
  - Increase in metal layers
- In order to keep the same cost, wafer fab capacities are enlarged year by year.

Source: Calculate from Financial Reports of Foundry Companies

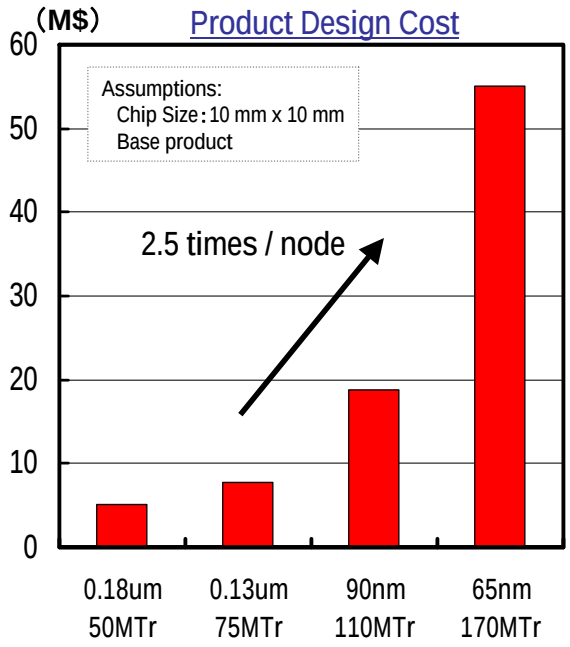
Wafer Process Development Cost



- Cost of developing wafer process technologies increases rapidly.
- Cost increases 1.4 times per technology node
- In order to reduce this cost, joint development is being done by several camps.

Source: IBS, April 2006

Design Cost



- Design costs increase as
  - Increase in the level of integration
  - Advanced process technology is used
  - Higher performance is required
- Cost increases 2.5 times per technology node

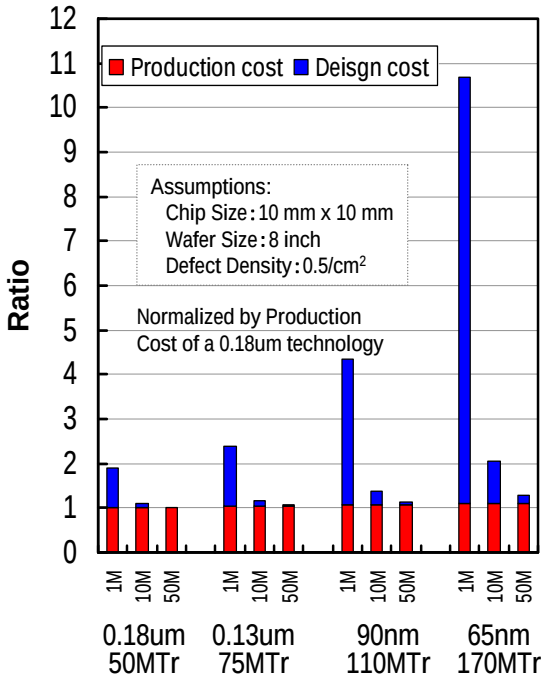
Source: IBS July 2005

Cost per Chip

- Wafer production cost per chip
  - Total fab expense (Ef) divided by total number of chips (Nf) which are fabricated by the fab.
- Wafer process development cost per chip
  - Process development expense (Ep) divided by number of chips (Np) which are fabricated by the process
- Design cost per chip
  - Design expense(Ed) divided by number of chips (Nd) which are fabricated by the design
- Value: Ef>Ep>Ed, Nf>Np>Nd,
- Increasing rate of expense from 0.18 um to 65 nm :
  - Increasing rate of Ef< Increasing rate of Ep< Increasing rate of Ed

Percentage of Design to Chip Cost

Manufacturing and Design Costs per Chip

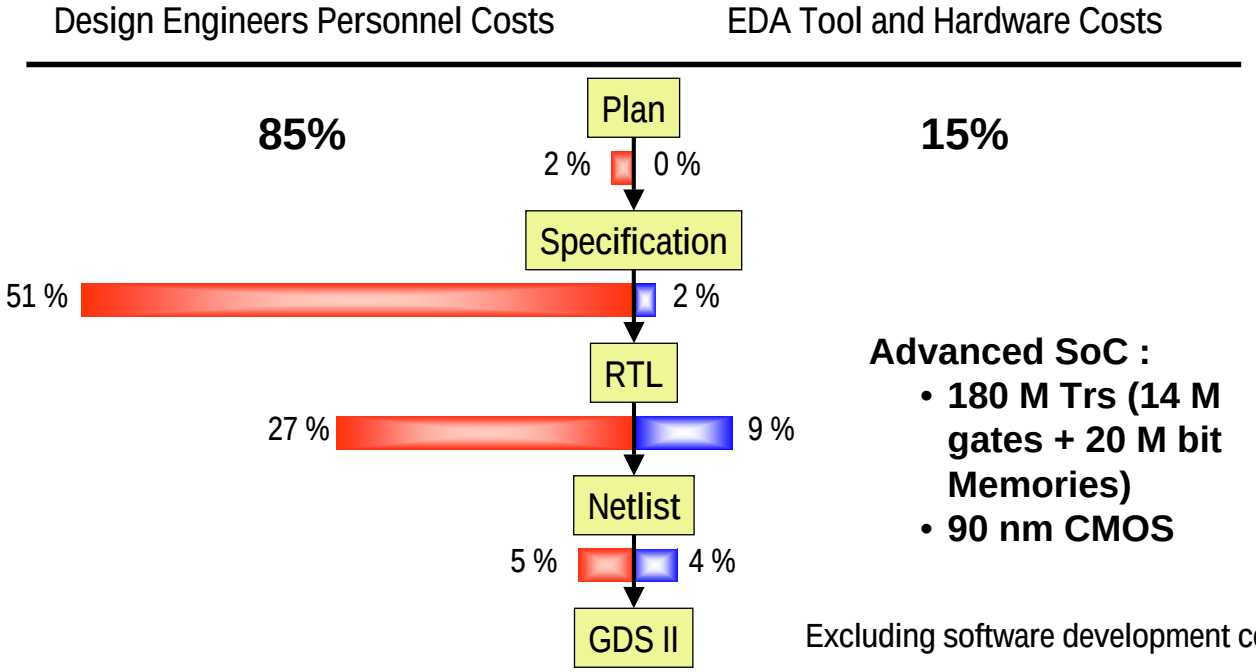


Source: Renesas Internal Estimation

- The percentage of design cost has increased compared to total cost, making it necessary to decrease this cost while increasing production/sales. Re-use of previously-designed IP is a necessity.
- To reduce total design cost
  - Key is to reduce system level design engineer personnel expenses.
- To enlarge sales volume
  - It is important to generalize hardware design and to increase production volume per design.

Breakdown of Advanced SoC Design Cost

- Design cost consists of design engineer personnel costs, EDA software expenses, and computing hardware expenses.



Advanced SoC :

- **180 M Trs (14 M gates + 20 M bit Memories)**
- **90 nm CMOS**

Excluding software development costs

Summary

- Miniaturization and integration have brought improvements of performance and economics of LSI's and tremendous growth in the semiconductor industry.
- However, miniaturization and integration cause result in increase in
  - Process development cost,
  - Wafer production cost, and
  - Design cost
- Percentage of design cost per chip will increase and the key to success for the SoC business is to reduce this design cost.
- Reduction of system level design cost is a major challenge for advanced SoC's

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