Is SDR Mature For Mobile Baseband Solutions ?

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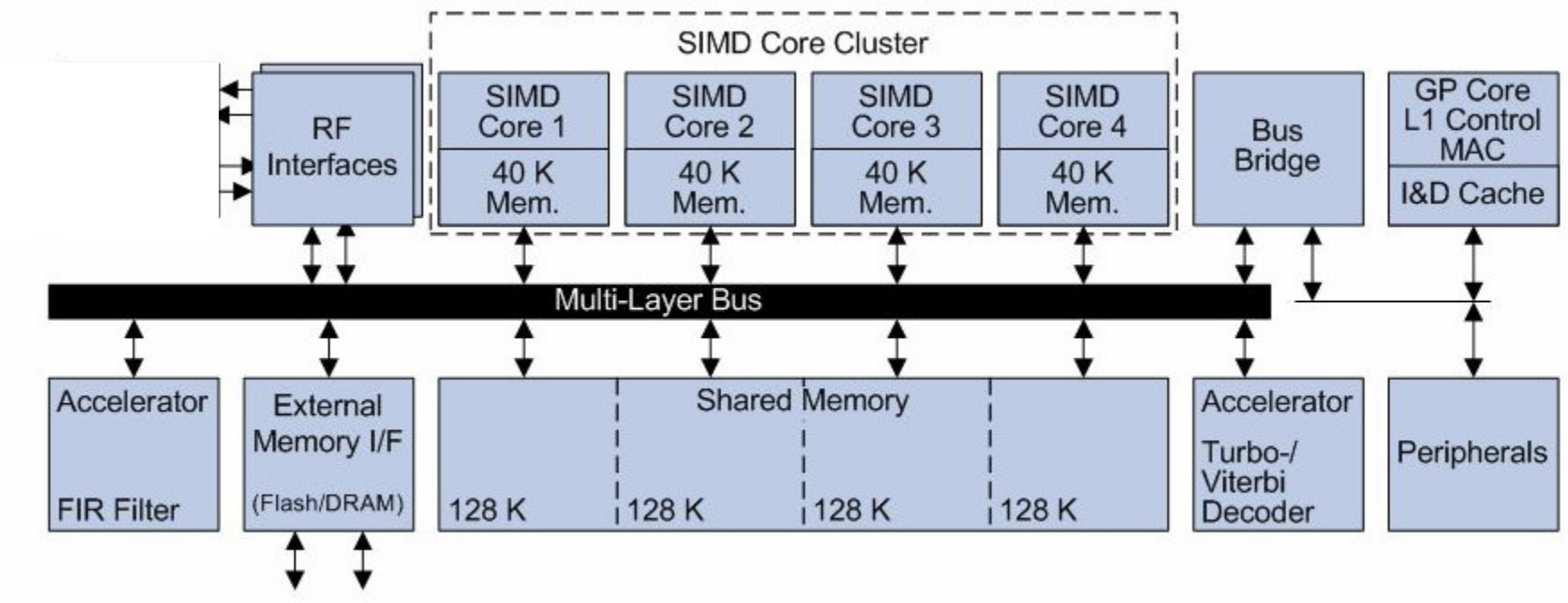
COM IN

Never stop thinking

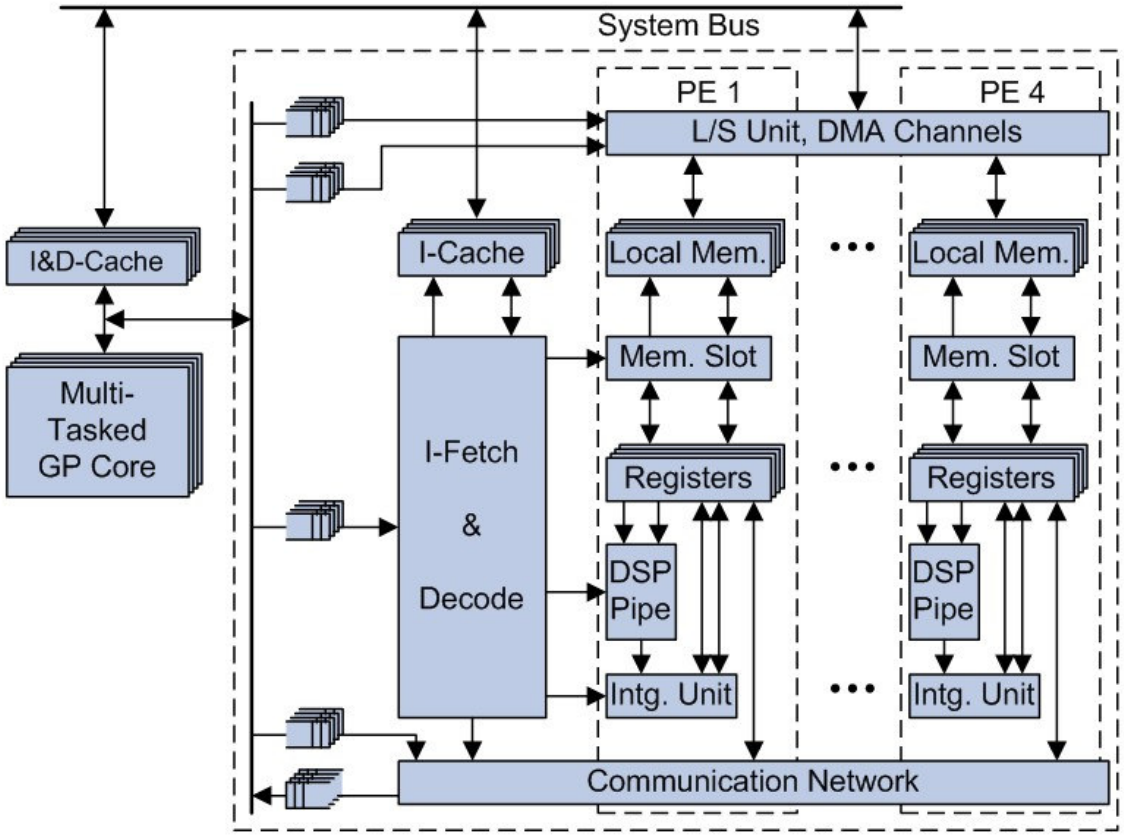
Our solution : Baseband Processor MuSIC



- 3-Level Memory Hierarchy
  - external DRAM/Flash
  - Shared Memory
  - Local Memories
- GP Core for L1 Ctrl & MAC
- reconf. accelerators for FIR and Channel Encoding/Decoding

Concept of Multi-Tasked SIMD Core

- 4 SIMD Execution Units
- Long Instruction Word
  - Computation Slot (DSP Pipe & IU)
  - Memory Slot
  - Communication Slot
- 4 Interleaved Threads
- Multi-tasked GP core to control the SIMD core
- Local Data Memories instead of L1 Cache



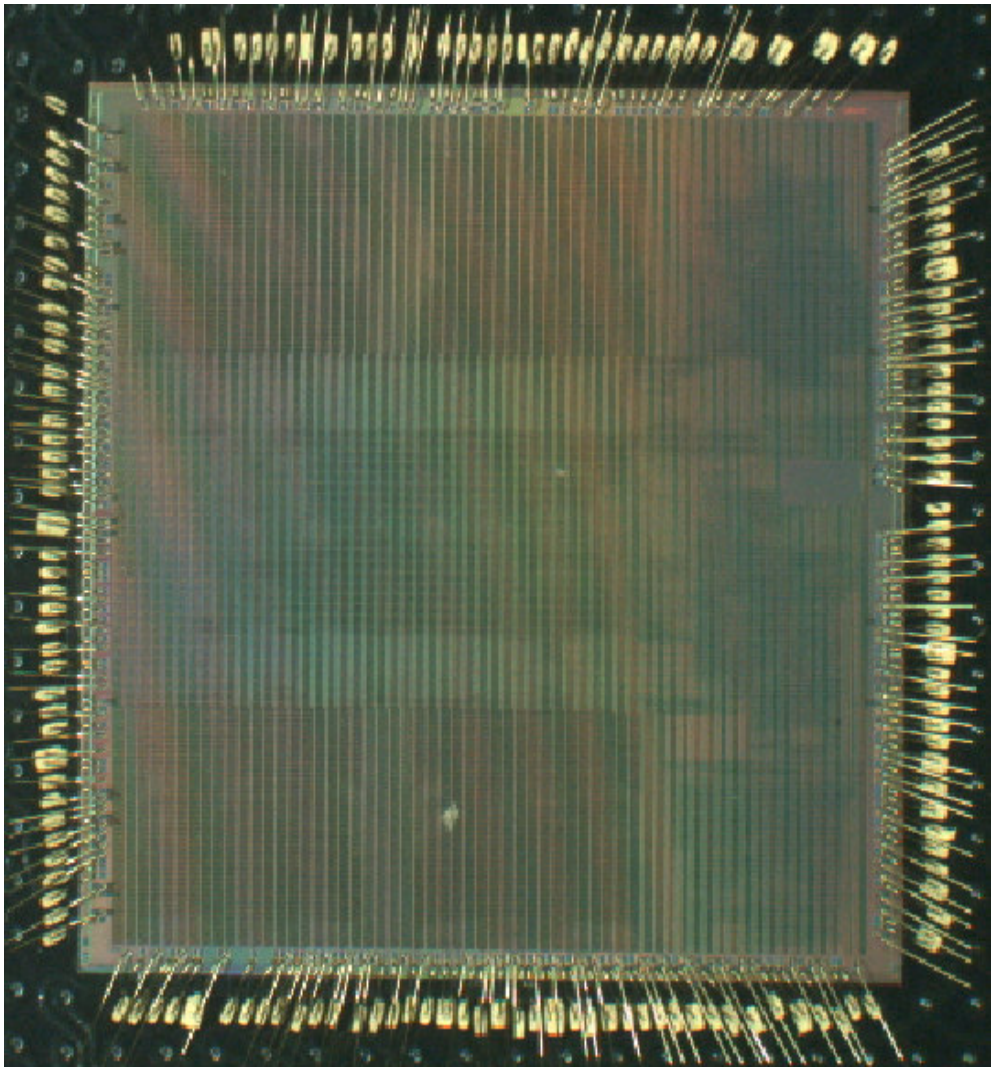
PE memory slot: **82 load/store instructions**
DSP Pipe: **25 instructions**
Integer Unit: **122 instructions**
Inter-PE Communication: **27 instructions**
RC1632: **230 instructions (159 in 16bits, 71 in 32 bits)**

MuSIC-1 Silicon in Dec. 2006

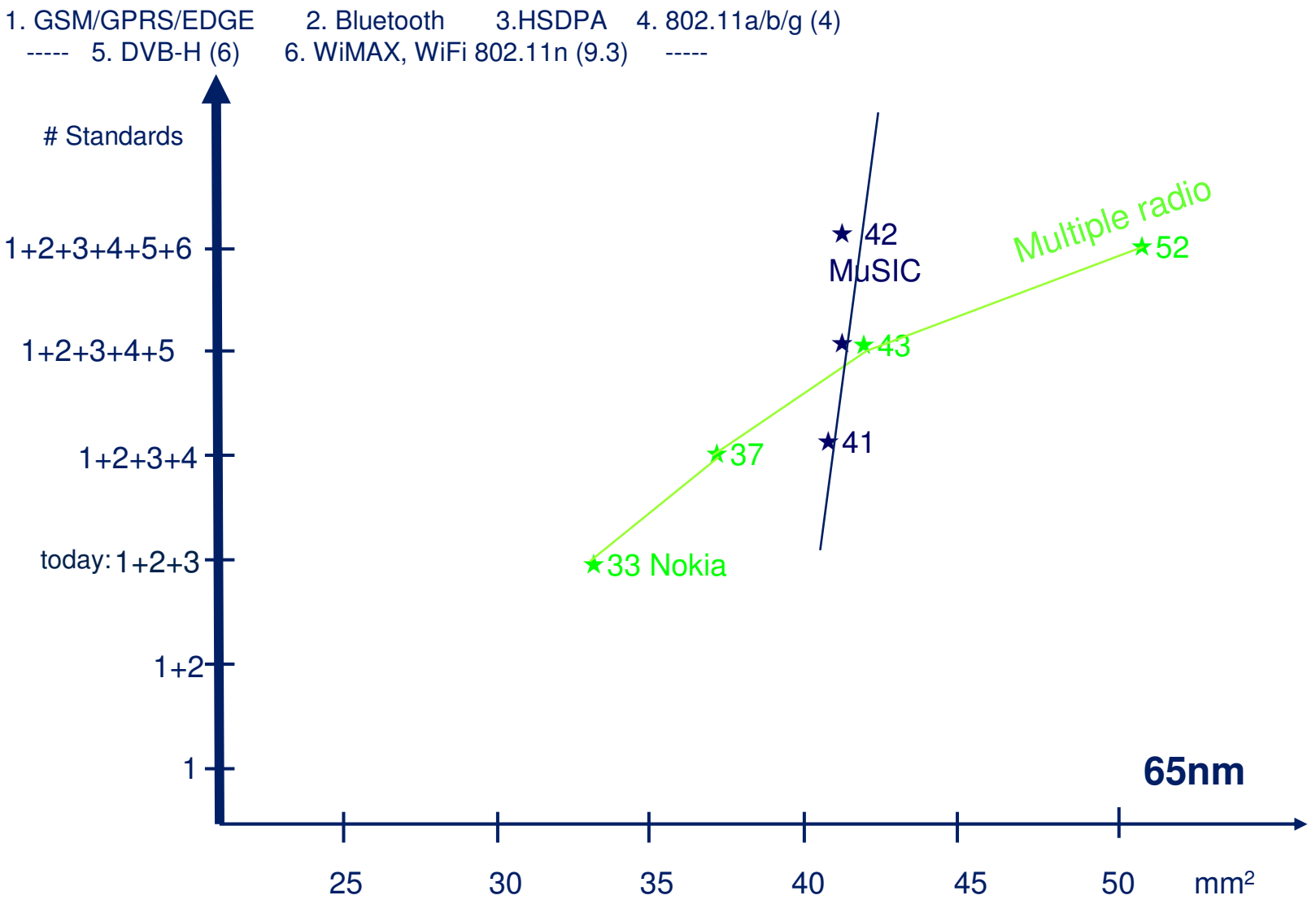
Technology:
90 nm CMOS

28 million trs for logic
+
768KB for memory

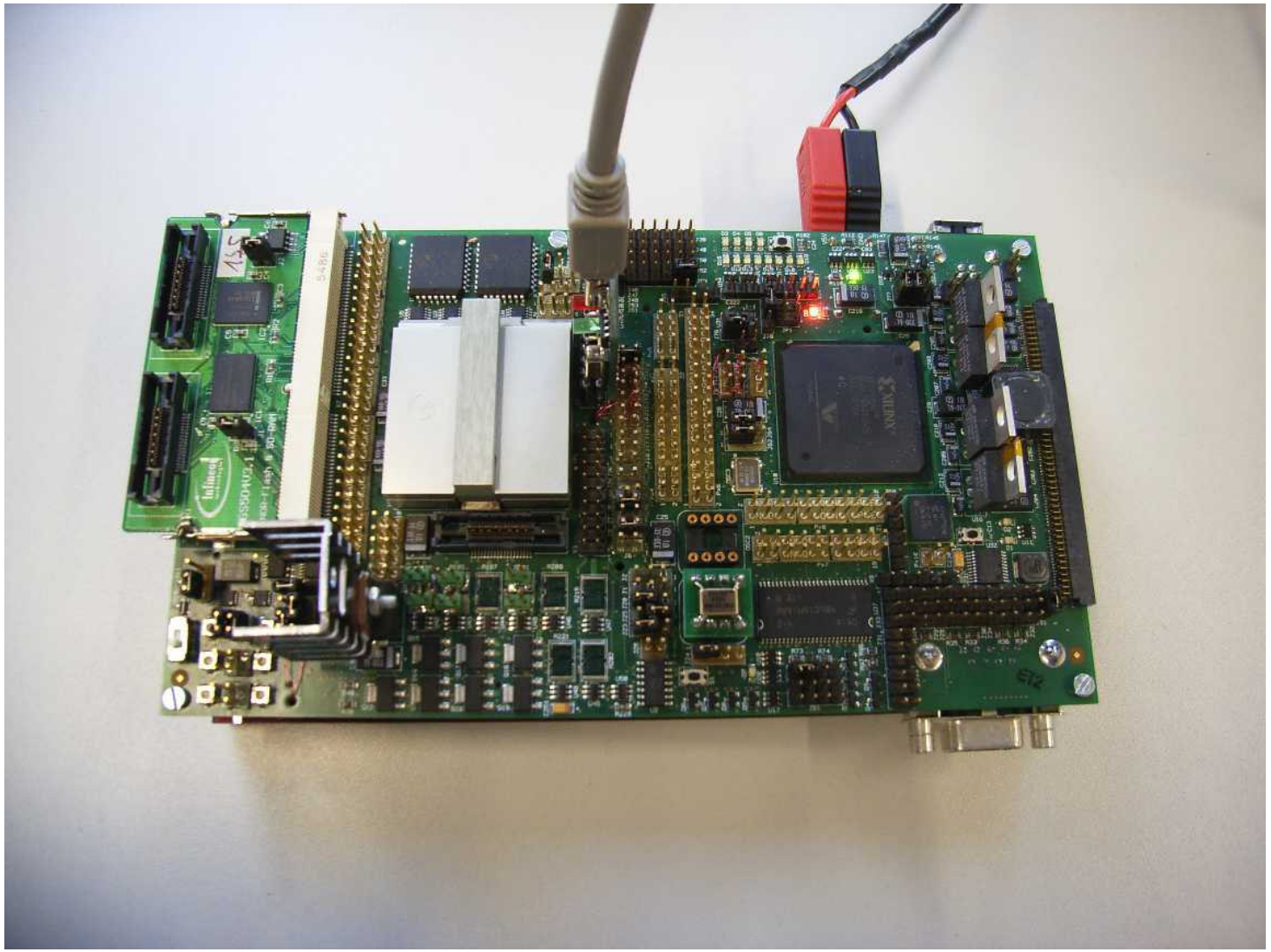
Area:
57 mm^2



Dilemma of Classical Solutions

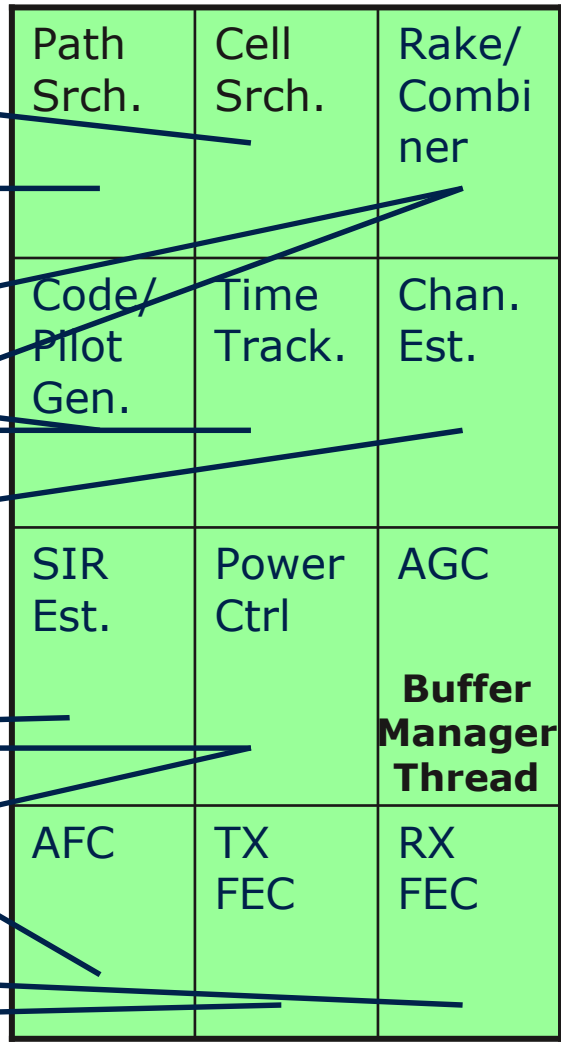


MuSIC-1 Evaluation Board



WCDMA function – thread mapping

- Cell Searcher
  - Slot boundary detection
  - Frame boundary detection
  - Scrambling code identification
- Path Searcher
  - Delay Profile Measurement
  - Finger Assignment
- Rake Code Generation
  - Scrambling/OVSF-Code Generation (for each channel/base)
- Rake Processing (rake finger)
  - Despreading of CPICH and one other channel (e.g. BCH, DCH)
  - Time Tracking
- Maximum Ratio Combiner (MRC)
  - Combing of rake finger outputs (one for each channel/base)
  - Channel Estimation
  - AFC Measurement and Ctrl
- TPC/SIR
  - Extraction of power Ctrl Bits
  - Signal/Interference measurement
  - (Power Ctrl)
- Outer Receiver
  - Deinterleaving, Demapping, Decoding (RX FEC), TFCI proc.
- Transmitter
  - Encoding (TX FEC), Interleaving, Mapping, Spreading
  - Power Ctrl
- Add. threads: Phy-Ctrl, Buffer Manager (incl. RSSI, AGC), FE/FIR-Ctrl, T/V-Ctrl



Total baseband power incl. ARM and Accelerators

WCDMA
3 basest.
8 fingers

300 MHz	90nm	65nm
4 simd cores	268	159
fir acc	57	33
tv acc	49	27
arm subsystem	40	24
bus & mem & sync & rfif	63	37
MuSIC total	**477**	**280**

- Worst case savings
- Further power saving measures:

  Use of low, regular, and high V_t for minimal active power as well as leakage

  Use of 8 metal layers instead of 6

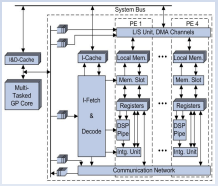
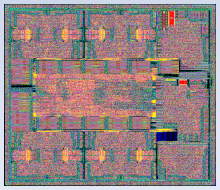
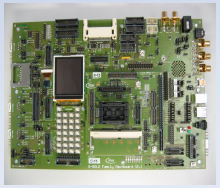
  Area and power shrinkage by full custom design

  Multiple voltage domains instead of a single one

MuSIC VC Performance in 65nm

	Coding Perfomance	Format	SIMDCores	Power Consumption
H.264 Decode	8000 Macro Blocks / (s x SIMDCore)	CIF/15fps	1	11 mW
		CIF/30fps	1+1RC	22 mW
H.264 Encode	4000 Macro Blocks / (s x SIMDCore)	CIF/15fps	1+1RC	22 mW
		CIF/30fps	1+2RC	45 mW
MPEG-4 Decode	13000 Macro Blocks / (s x SIMDCore)	CIF/15fps	1	7 mW
		CIF/30fps	1	13 mW
		VGA/30fps	1+2RC	40 mW
MPEG-4 Encode	6500 Macro Blocks / (s x SIMDCore)	CIF/15fps	1	13 mW
		CIF/30fps	1+1RC	25 mW
		VGA/30fps	2+4RC	75 mW

Decision: Commercialize SDR Mobile Platforms

	Phase	Milestones & Achievements
✓	**Innovation**	**Innovation Project:** ■ Multi-processors architecture (SIMD cores) ■ Asynchronous control → flexibility & power ■ Virtual Prototyping of entire SDR Core 
✓	**Test Chip**	**Innovation Project:** ■ MuSIC-1 Test chip in 90nm CMOS technology ■ 4 SIMD Cores @ 300MHz, ARM9 @ 200MHz ■ Proof-of-Concept of chip architecture / area 
✓	**Proof of Concept**	**Innovation Project:** ■ MuSIC-1 Evaluation Board ■ Proof-of-Concept of SDR architecture / Power ■ Demo of multi-standard / LTE development kit 
→	**Product**	**SDR Mobile Platforms Business:** ■ Commercialize SDR: SDR Core IP up to Full Platform business models ■ MuSIC-2: 8 SIMD, 2 ASIP, ARM11, and MM @ 65nm technology ■ Development kit for full system integration (incl. RF) / field tests ■ SW Development & Debug tools / multi-standards mapping

BB Summary

- **Multiple standards become the standard for mobile radios**
- **The multiple radios solutions of today will be replaced by programmable multi-processor solutions**
- **SW programmable multi-processor solution in 2010 latest**
  - competitive area+power
  - High re-use in HW&SW because of superior flexibility