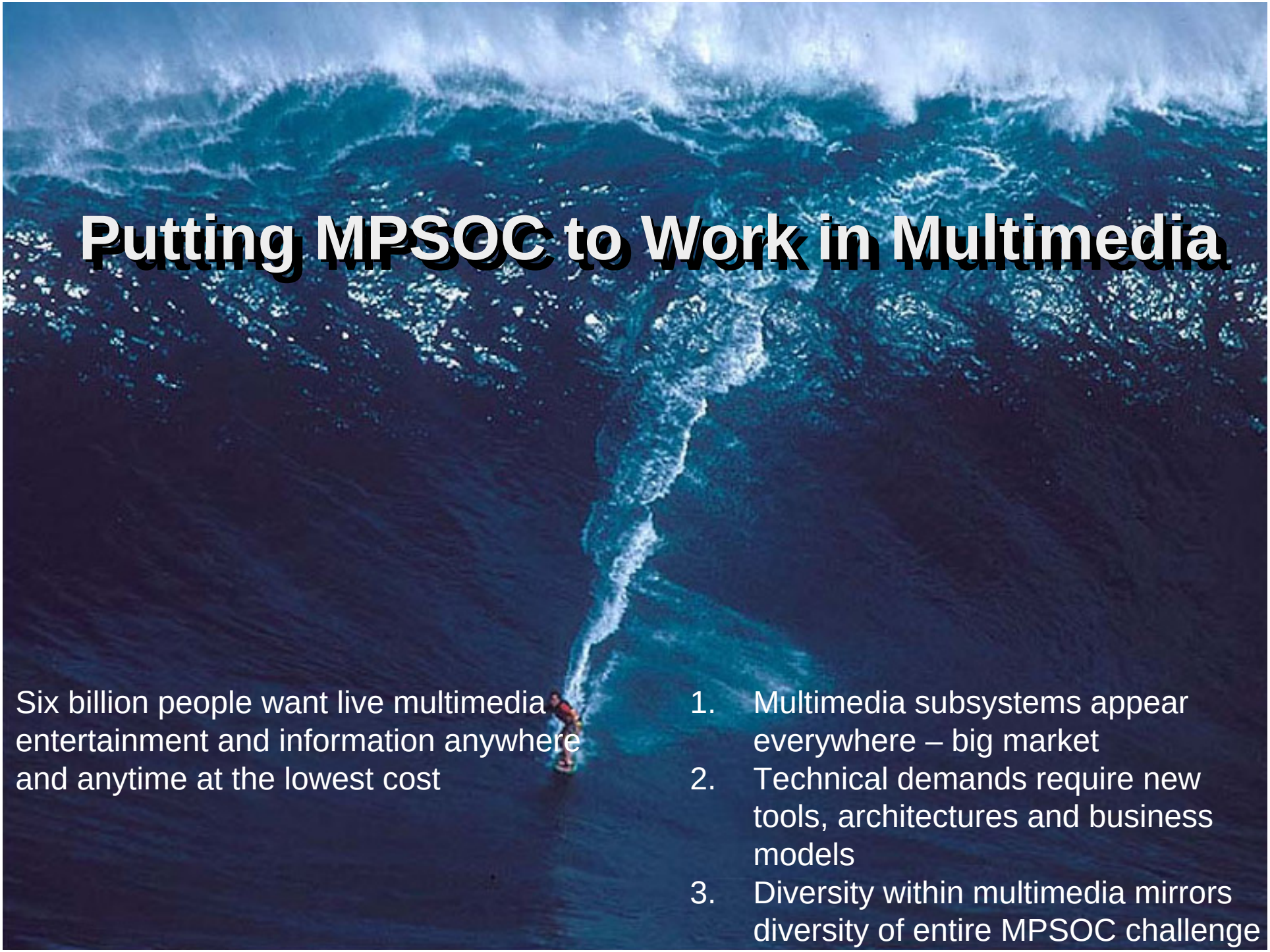


Putting MPSOC to Work in Multimedia

Six billion people want live multimedia entertainment and information anywhere and anytime at the lowest cost

1. Multimedia subsystems appear everywhere – big market
2. Technical demands require new tools, architectures and business models
3. Diversity within multimedia mirrors diversity of entire MPSOC challenge

MPSOC Becomes Mainstream Style

The Transformation of the Modern Mobile Device

Key complementary processing functions of mobile devices covered by Tensilica configurable processors

Mobile WiFi

Camera Image Processing

User Authentication

HD Radio

Satellite Radio

Audio Codec

Video Codec

Noise Cancellation

DTV Reception

Baseband DSP

Bluetooth

GPS

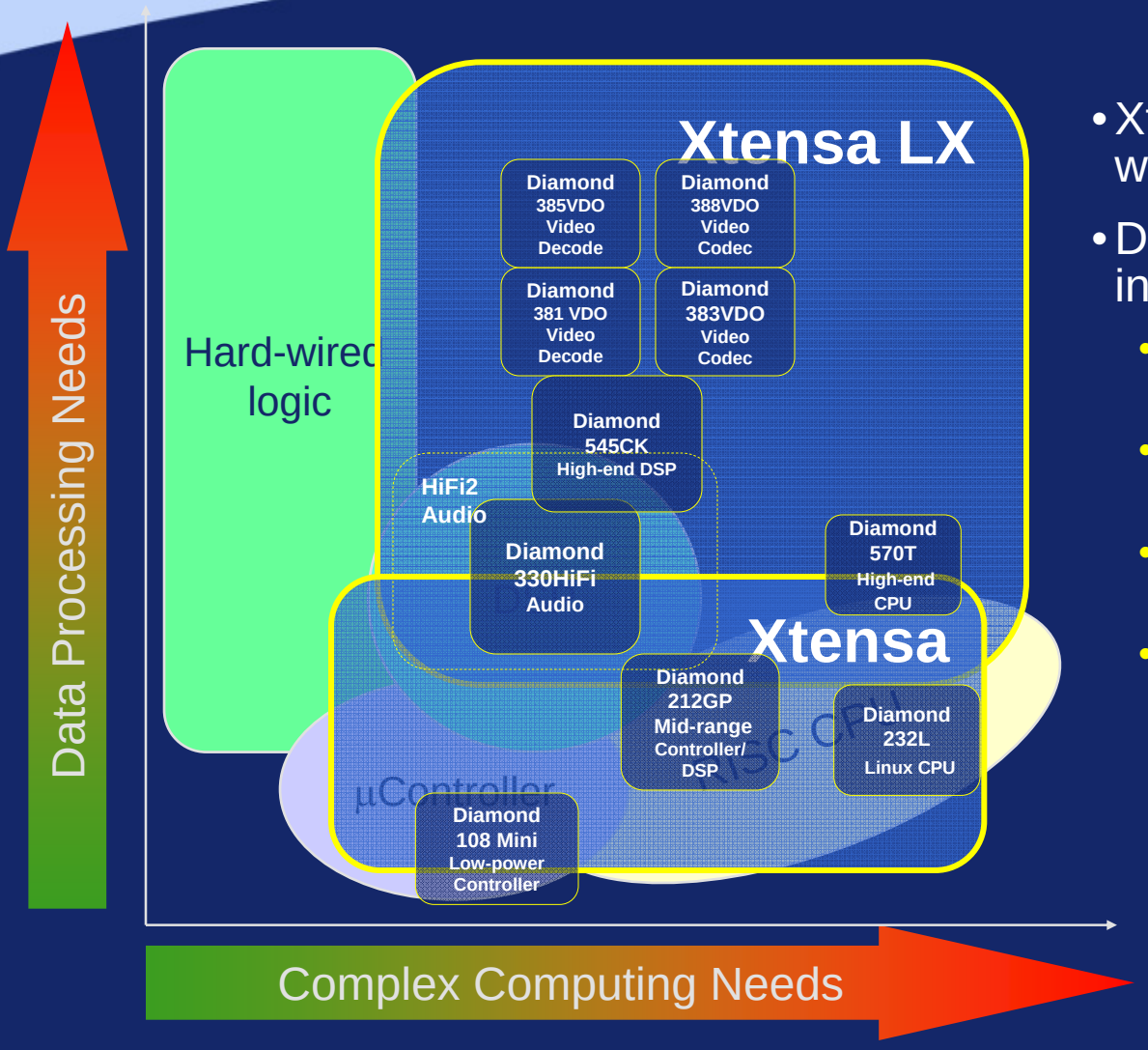
Software Rules

Network of Partners and Customers Defines Strength

AFA TECHNOLOGY

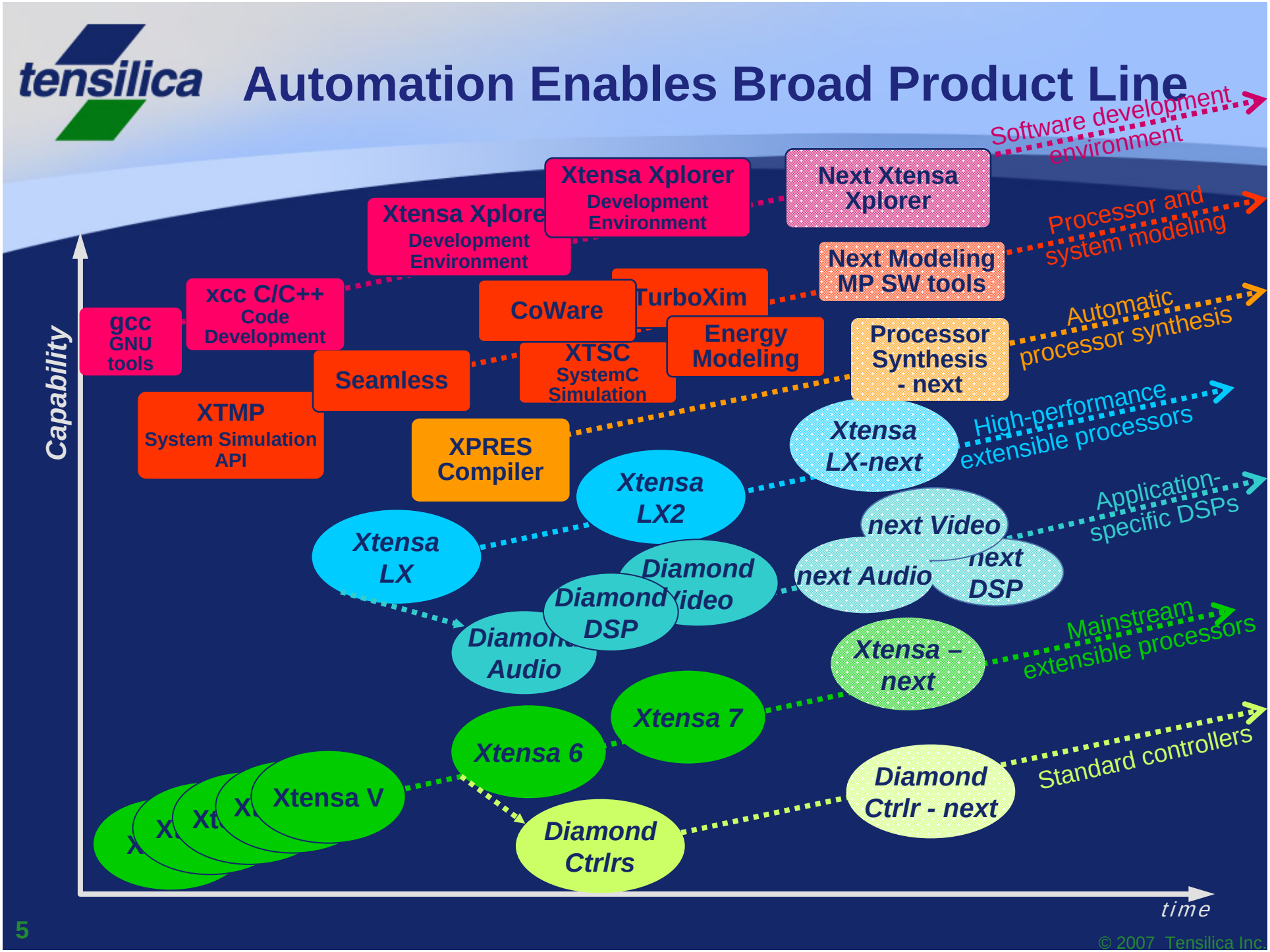
Design Teams Need Different Entry Points

Key Question: Who Specifies Processor?



- Xtensa configurable processors widely used in multimedia
- Diamond Standard cores introduced February 2006:
  - Broad line of compatible controller, CPU and DSP cores
  - High performance general-purpose DSP
  - Complete low-power HiFi2 audio solution
  - Diamond Video spans wide range of mobile media needs

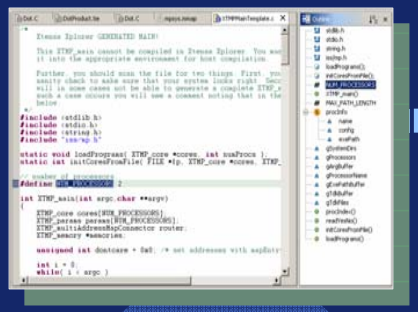
Automation Enables Broad Product Line

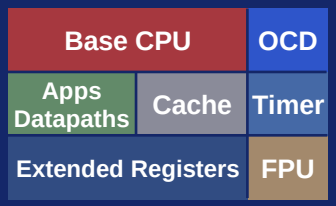


Multimedia Design is Energy-Based Design

Example: Xenergy Energy Explorer

Processor Description





Application Code

```
int main( ) {
 int i;
 short c[100];
 for (i=0;i<N/2;i++)
 {
```

Xtensa xcc
C/C++ compiler

Xenergy Energy Estimator

Tune processor instruction set and memories

Complete Dynamic Energy/Power Profile
Processor + Memory

Tune software algorithms and coding

Application-Specific Processors
Example: HiFi 2 Audio Engine

- **Pre-configured VLIW audio DSP with dual 24-bit MACs for higher quality audio**
- **Already in use in dozens of chip designs, licensed by many top semiconductor suppliers**
- **Available 2 ways:**
  - Xtensa HiFi 2 Audio Engine for further customization
  - Diamond Standard 330HiFi audio core
- **Delivers both low power and scalability**
- **<75K gates for full-feature processor**
- **Example: MP3 decode at 5.7 MHz (core + memory <0.75mW in 65nm)**
- **Emerging trend:** multiple instances of HiFi2 on same chip, tuned for different mW vs. MHz

Sample of HiFi2 Audio Software

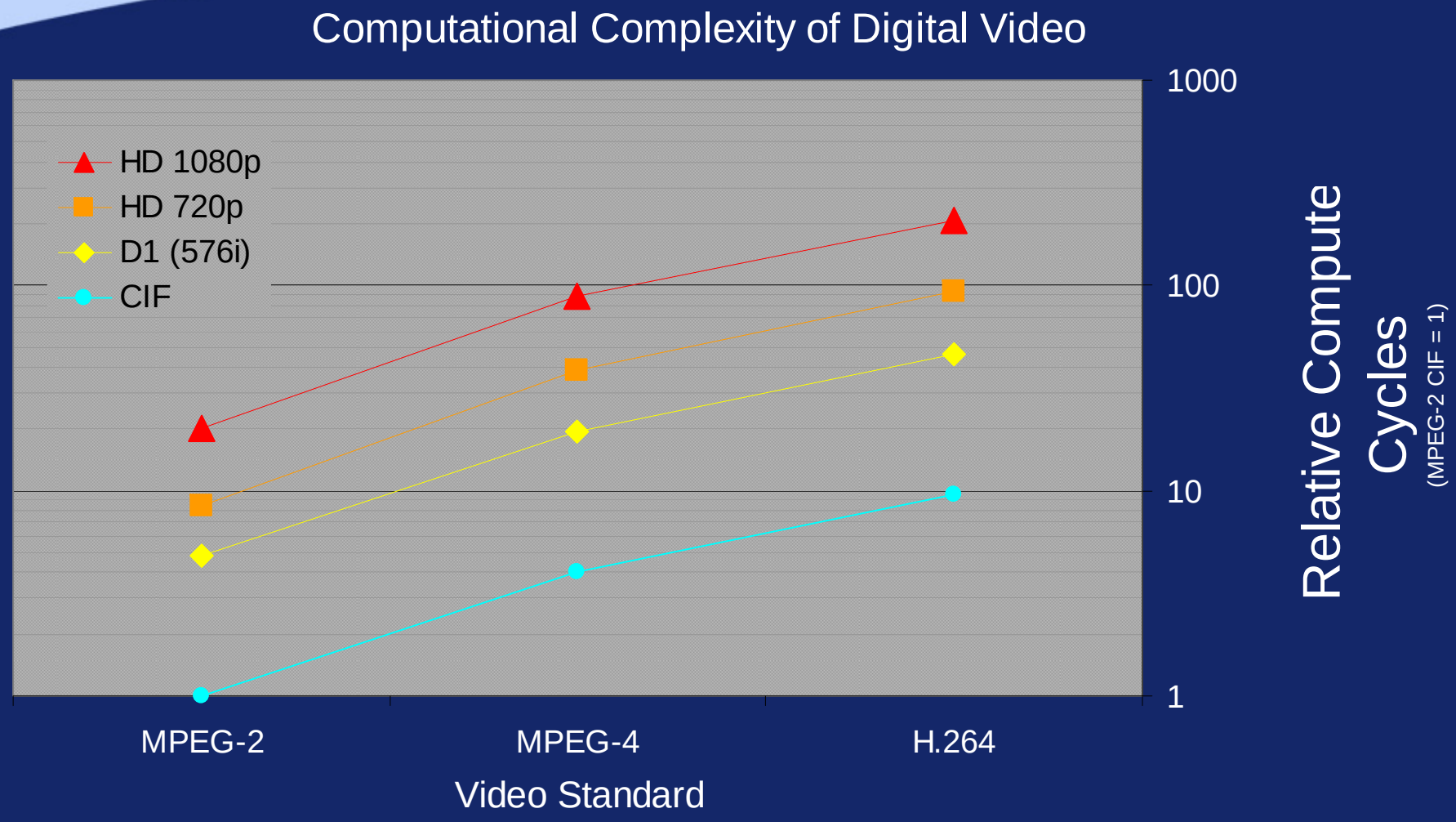
Currently available:

- MP3 decode
- MP3 encode
- WMA decode
- WMA encode
- AAC-LC decode
- AAC-LC encode
- aacPlus v2 decode
- aacPlus v2 encode
- aacPlus v1 decode
- aacPlus v1 encode
- Ogg Vorbis Decoder
- Dolby AC-3 5.1 ch decode
- Dolby AC-3 2 ch encode
- Dolby Digital Plus 5.1 ch decode
- Dolby Digital Plus 7.1 ch decode
- AM3D Diesel 3D
- AM3D Zirene effects
- QSound microQ MIDI, 3D, effects
- SONiVOX AudioiNSIDE MIDI
- SRS WOW XT audio expansion
- SRS Xspace 3D
- SRS TruSurround HD
- AMR NB codec
- AMR WB codec

Schedule for release:

- BSAC decoder
- Dolby TrueHD
- Dolby Digital Prologic II / IIx
- Dolby Digital Consumer Encoder 2 channel encoder
- Dolby Digital Compatible Output 5.1 channel encoder
- aacPlus 5.1/7.1 channel decode
- SBC Bluetooth stereo codec
- AMR-WB+G.711 codec
- G.723.1 codec
- G.726 codec
- DTMF
- aacPlus 5.1/7.1 channel decode
- Dolby TrueHD Dolby Digital Prologic II / IIx
- G.167 (AEC)
- G.168 (LEC)
- WMA 10 Pro Decoder

Growth in Video Resolution and Complexity

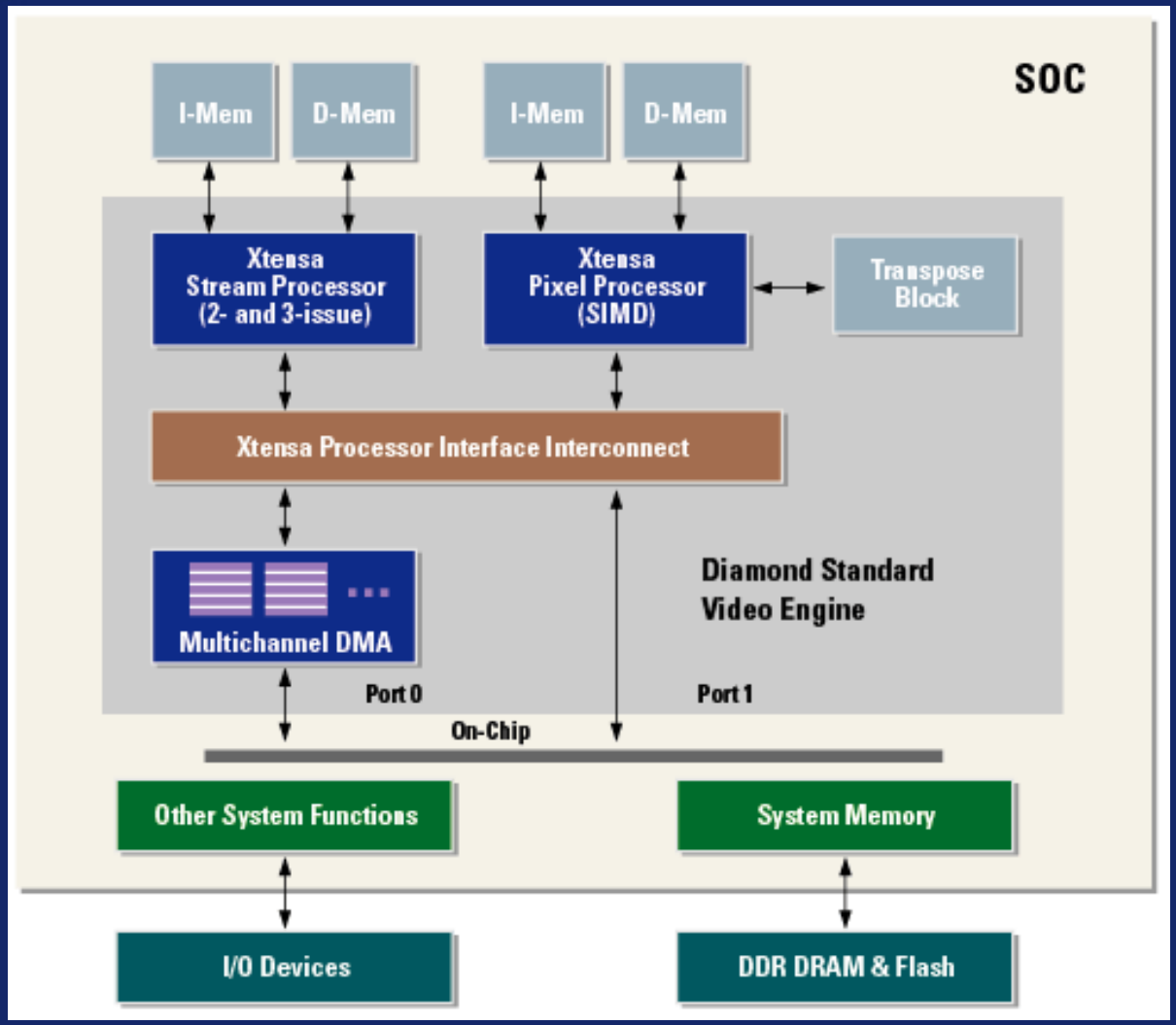


Source: "A Performance Characterization of High Definition Digital Video Decoding using H.264/AVC", scaled for CIF

Diamond VDO Design Goals

- **Video encode & decode up to**
  - 720 x 480 @30 fps (NTSC)
  - 720 x 576 @25 fps (PAL)
- **Support multiple coding standards @ main profile**
  - H.264 main profile @ L3 decoder
  - MPEG-4 ASP [no GMC] @ L5 decoder
  - MPEG-2 MP @ ML decoder
  - WMV9/VC1 main profile decoder
  - MPEG-4 ASP encoder
- **Programmable solution**
- **Less than 100MB/s memory decode bandwidth requirement**
- **Operating frequency <200Mhz**
  - Can be implemented in 130nm G technology
- **Compatible subsets for decode only and Base Profile only**

Top Level Block Diagram



Diamond VDO Product Family

Tensilica Engine	Decoders	Encoder
Baseline Profiles – D1		
Diamond 381VDO	H.264 Baseline Profile MPEG-4 Simple Profile VC-1/WMV9 Simple Profile MPEG-2 Main Profile	None
Diamond 383VDO	H.264 Baseline Profile MPEG-4 Simple Profile VC-1/WMV9 Simple Profile MPEG-2 Main Profile	MPEG-4 Simple Profile
Main / Advanced Profiles – D1		
Diamond 385VDO	H.264 Main Profile MPEG-4 Advanced Simple Profile VC-1/WMV9 Main Profile MPEG-2 Main Profile	None
Diamond 388VDO	H.264 Main Profile MPEG-4 Advanced Simple Profile VC-1/WMV9 Main Profile MPEG-2 Main Profile	MPEG-4 Advanced Simple Profile

Standard	Resolution	Frames-per-Second	Max. Required Clock Rate
H.264 Main Profile Decode	D1	30	172 MHz
MPEG-4 Advanced Simple Profile Decode	D1	30	156 MHz
VC-1/WMV9 Main Profile Decode	D1	30	189 MHz
MPEG-2 Main Profile Decode	D1	30	150 MHz
MPEG-4 Advanced Simple Profile Encode	D1	30	185 MHz

Optimizing Energy
ISA Extension Example: CABAC

- **Context-adaptive binary arithmetic coding (CABAC) achieves higher compression in H.264**
  - **Required for Main Profile H.264 decoding**
  - **Our solution: Xtensa ISA extensions**
  - **Peak decode performance is one bin per cycle**

	Millions of cycles per second in unaugmented core	Millions of cycles per second in ISA extended core
CABAC decode cycles	**710**	**13**

Area cost: 20K gates for CABAC ISA extensions

Energy for 1 second	**164mJ**	**5mJ**

Unaugmented core assumes base core plus 16b MUL, LOOP ops, debug, PIF at max MHz

Optimizing Energy

Example: Motion Estimation for MPEG4 Encode

	Millions of cycles required on unaugmented core	Millions of cycles required on ISA extended core
16x16 SAD	527	16.3
Diamond	735	8.4
Half Pel	1143	10.7
8pt SAD	1659	14.2
Control	204	26.6
Motion Estimation	**4268**	**76.2**

Area Cost: Less than 40Kgates for all Motion Estimation extensions

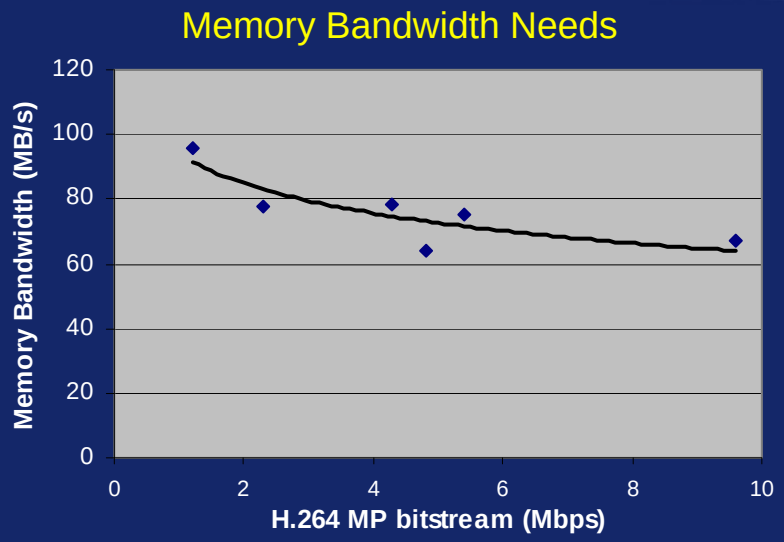
Energy for 1 second	**988mJ**	**29mJ**

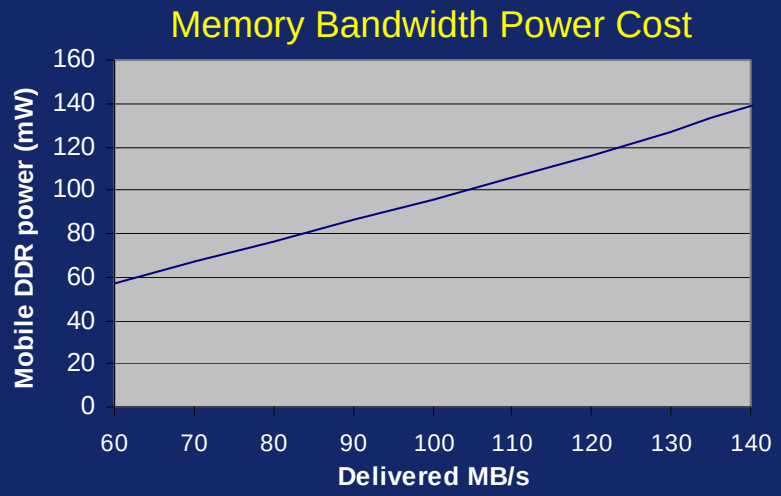
Unaugmented core assumes base core plus 16b MUL, LOOP ops, debug, PIF at max MHz

System Issues in Mobile Video

Example: Decode Memory Bandwidth Drives Power

- **Off-chip power is a major component of solution power**
- **Early, accurate modeling gives insight and enables novel optimization**
- **Non-trivial interactions:**
  - Core power **increases** with bit stream data rate
  - Memory power **decreases** with bit stream data rate
- **Design of video architecture, DMA and software reduces bandwidth by about one-third (saves 30mW)**
- **Additional power savings in on-chip interconnect and memory controller**

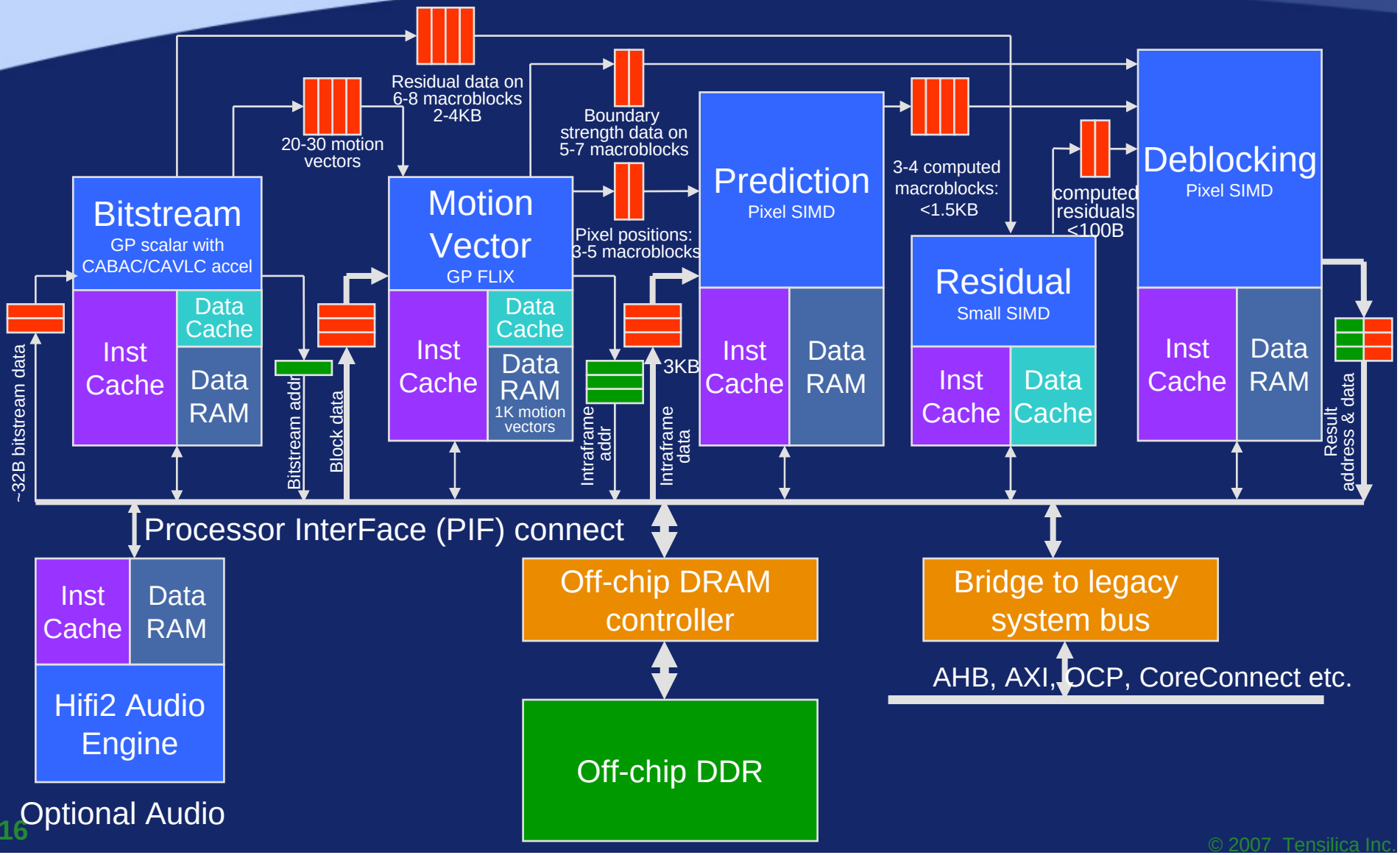




Estimated power for Micron MT46H16M16LF Mobile DDR at 133MHz: 50% 16B block read, 50% 16B writes

Move Up to Fully Programmable HD

Approach: five small video task engines + audio

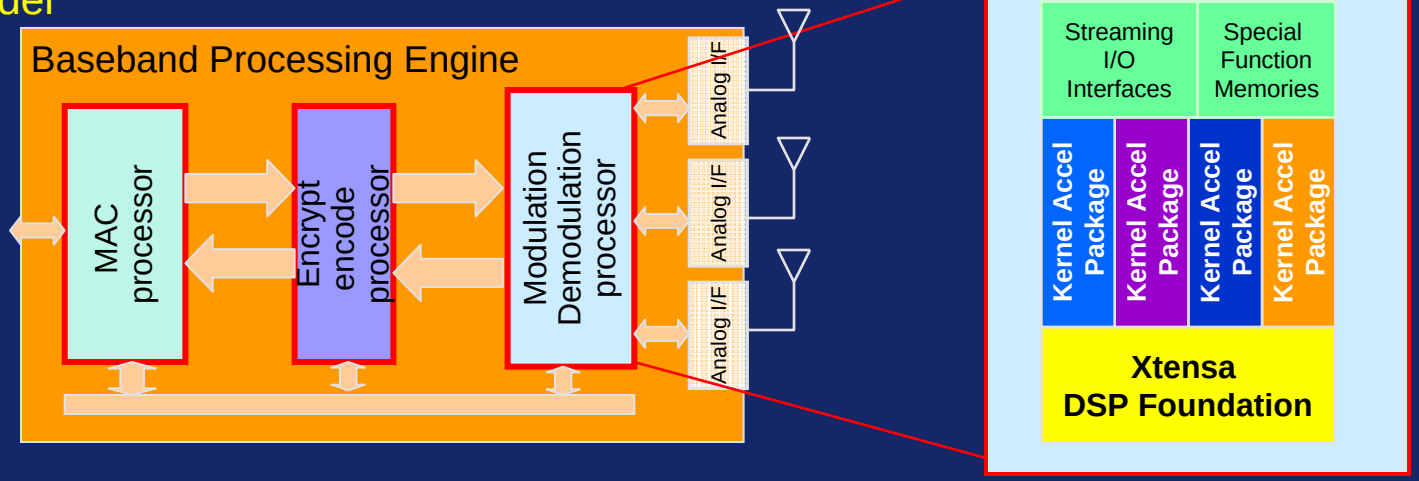


Baseband DSP Needs Extensible Processors

Optimized baseband architecture with DSP-optimized task-engines

- Explosion of standards and multiple radios dictates agile-but-efficient baseband design
- Each processor extensible to handle specific algorithm kernels with RTL-like power and throughput
- Easy composition of engines into efficient pipeline
- Unified hardware and software development model

Domain	Function	Versus	Efficiency (cycle reduction)
Modulation (e.g. OFDM)	FIR	TI C64x	**4x**
	FFT	TI C64x	**3x**
Error Coding	Viterbi	TI C64x	**3x**
	Turbo decoding	TI C62x	**18x**
	LDPC	TI C64x	**~100x**
Security	3-DES	RISC	**43x**
	AES	RISC	**300x**
	SSL	RISC	**4x**
Upper layer processing		RISC	**2x**

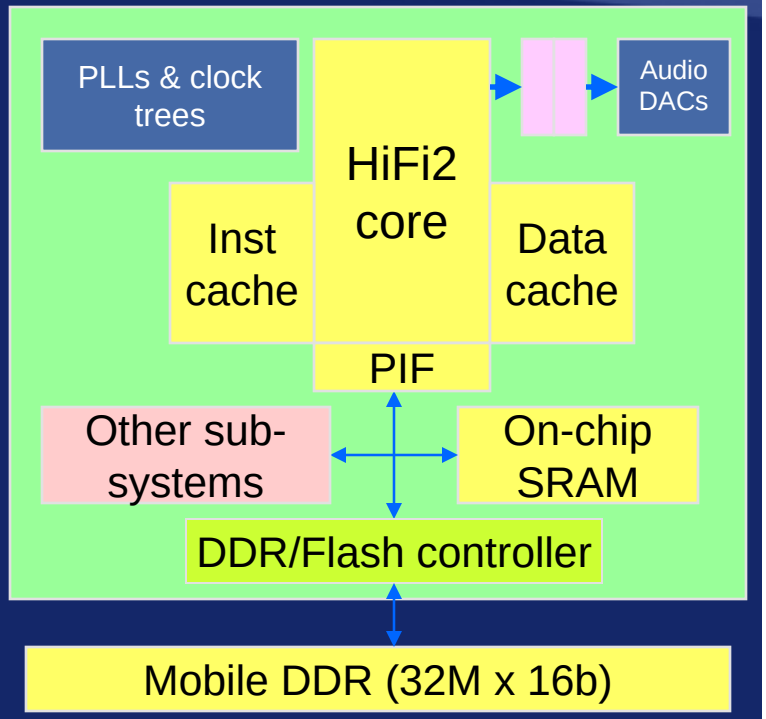


System Level Design Matters

Example: Audio System Optimization

System-level design tools make a big difference

- Tensilica supports wealth of system modeling: ISS, TurboXim, XTMP C modeling, XTSC System C modeling, CoWare, Seamless
- Tensilica Xenergy Energy Estimator provides rapid, accurate configuration-specific application power analysis
- Example: Audio system organization analysis:



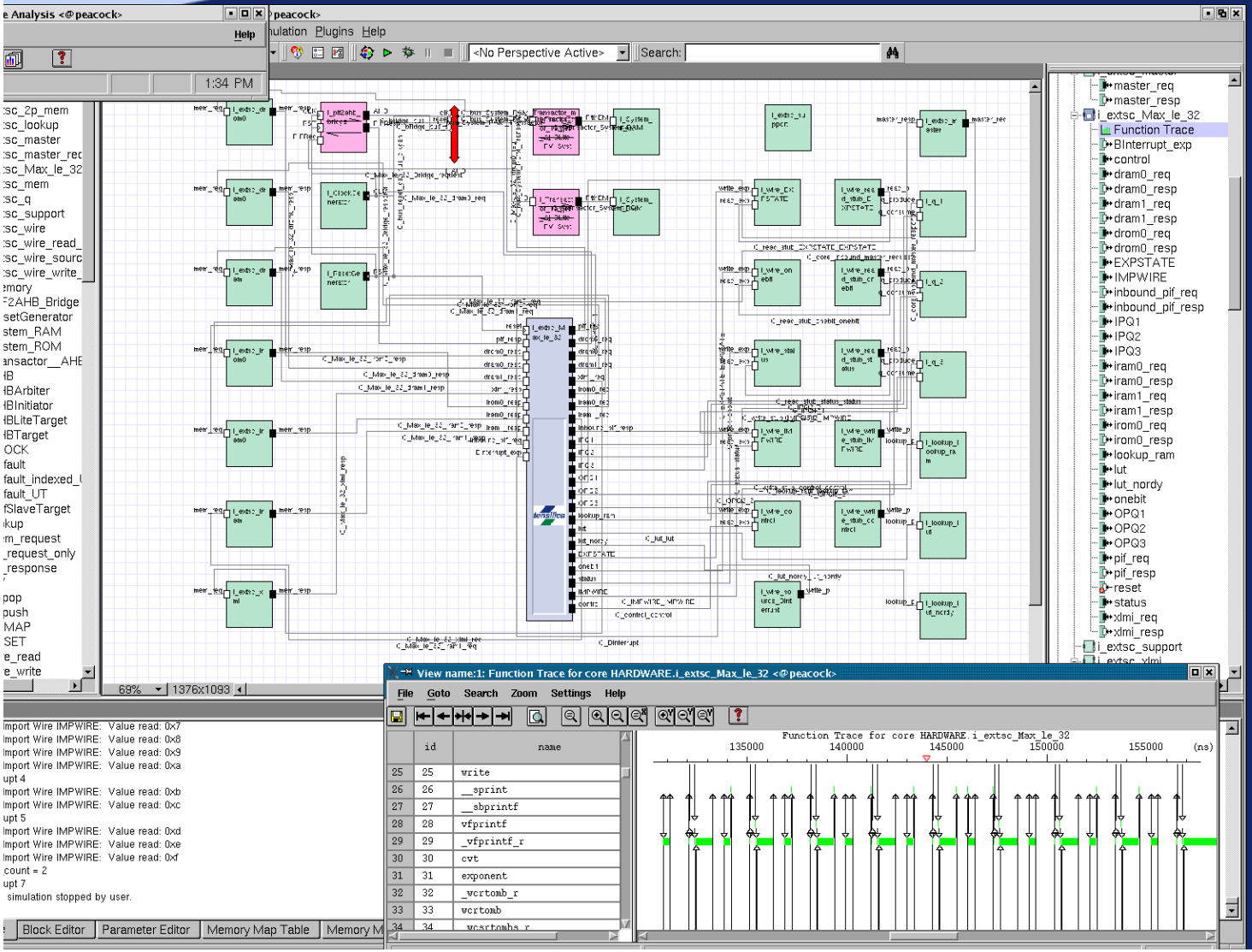
Relative power

System Organization	90G	90G high-vt
4K/8K DM + DDR	1.00	0.94
4K/8K DM + 192K on-chip	0.65	0.16
16K/32K DM + DDR	0.36	0.25
16K/32K DM + 192K on-chip	0.65	0.15
16K/32K + 128K on-chip + DDR	0.56	0.19

- Power includes dynamic and static at minimum WMA decode MHz
- Power includes HiFi2 core, I cache, D cache, On-chip SRAM, DDR (no refresh)
- I/O through queues

MPSOC System Design is Collaborative

Example: Xtensa in CoWare Platform Architect



Configured subsystems with rich interfaces:

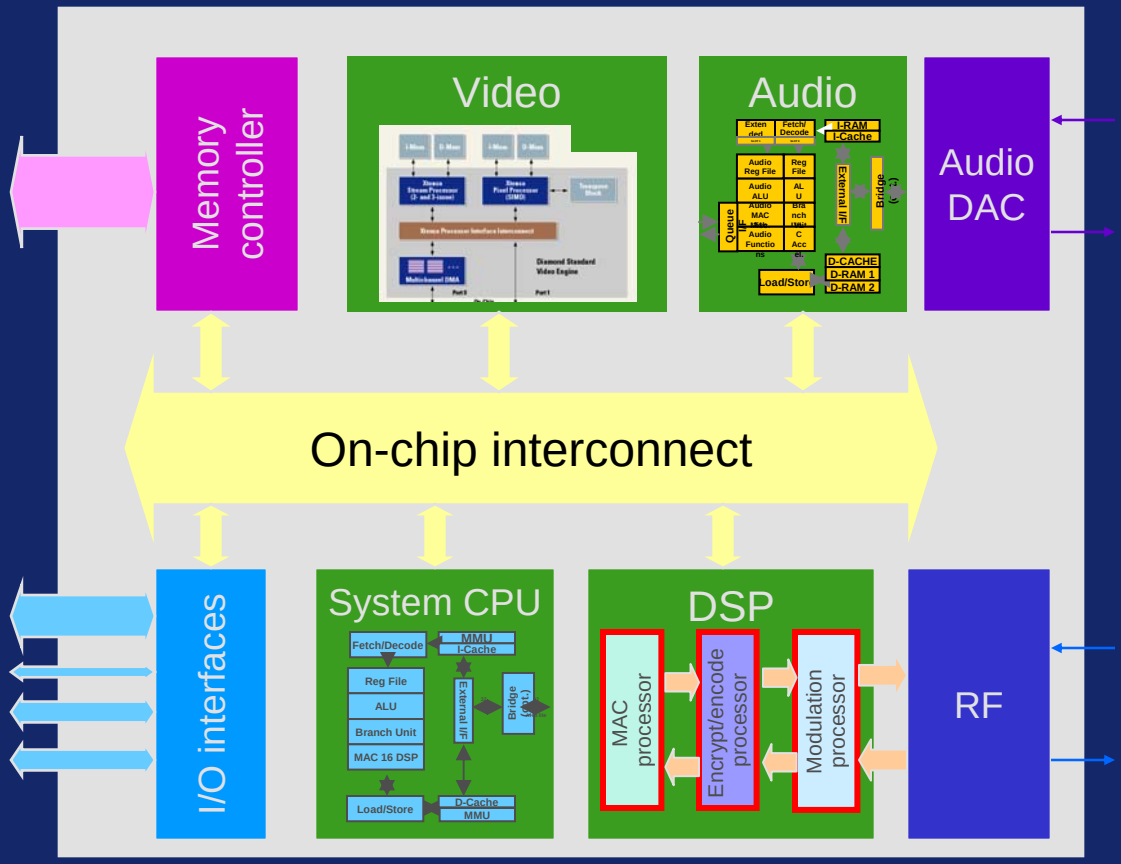
- AMBA bus
- Local memories
- Caches
- Special lookup memories
- Input queues
- Output queues
- Input wires
- Exported state wires
- Interrupts

- **Wrapper automatically generated from processor configuration**

Putting It Together

The principles

- Multimedia SOC is not “rocket science”: hundreds of designs underway around the world
- Pay attention to best practices:
  1. Leverage existing design standards, tools, interconnect and subsystem IP
  2. Model early and often. Cost, performance, power largely set in architectural phase
  3. Application standards explode. Build in programmability everywhere
  4. Look at total bandwidth and total power, especially in off-chip communications
- Differentiation, time-to-market and high efficiency are compatible!




Thank you!